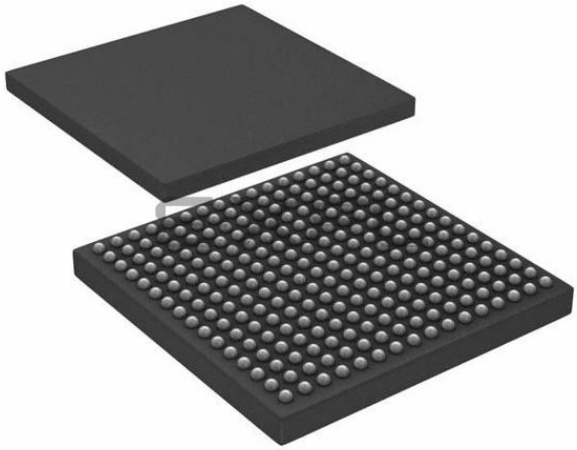
Lattice Semiconductor Corporation - LAXP2-17E-5FTN256E Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

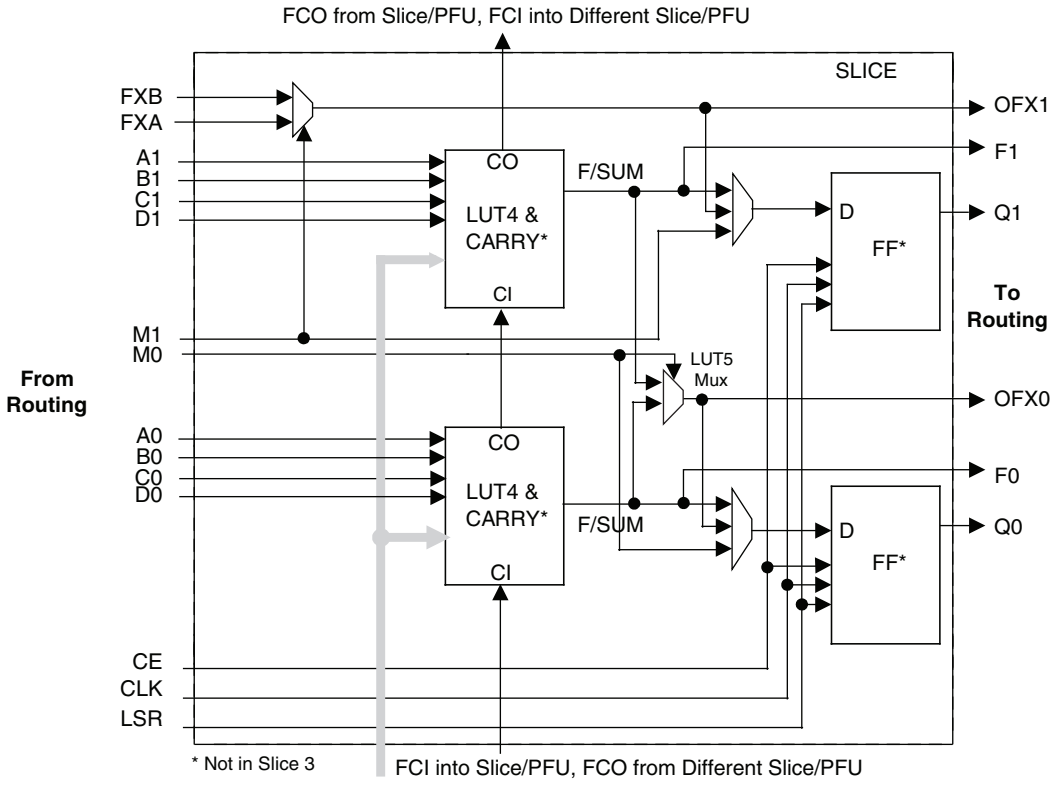
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-17e-5ftn256e

Figure 2-3. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from Slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four-input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LA-LatticeXP2 devices, see TN1137, LatticeXP2 Memory Usage Guide.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

EBR memory supports two forms of write behavior for single port or dual port operation:

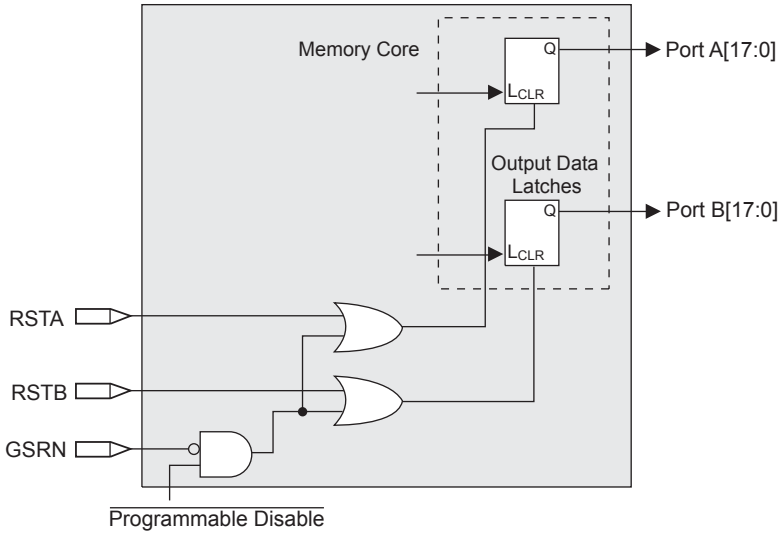
1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset

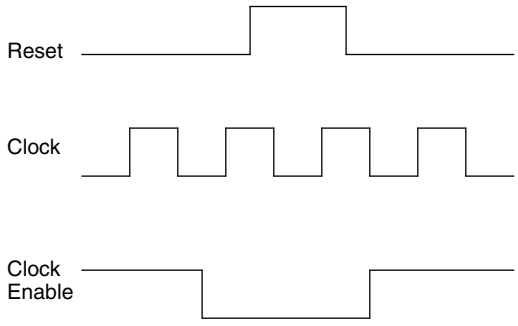


For further information on the sysMEM EBR block, see TN1137, LatticeXP2 Memory Usage Guide.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.

Figure 2-18. EBR Asynchronous Reset (Including GSR) Timing Diagram



mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be con•gured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-6 shows the capabilities of the block.

Table 2-6. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	4	2	—
MULTADDSUBSUM	2	1	—

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting ‘dynamic operation’ the following operations are possible:

- In the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle.
- In the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

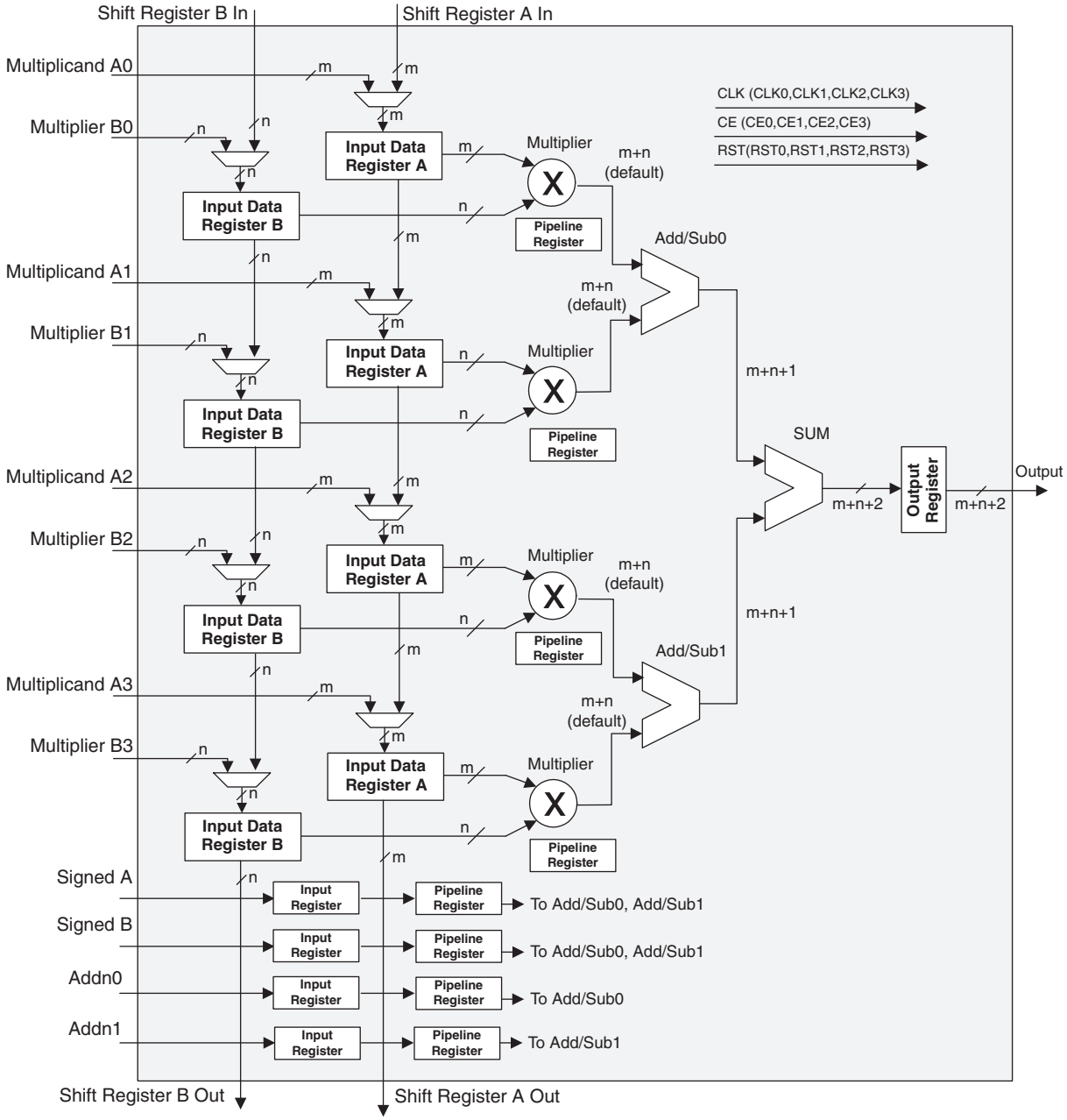
MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM

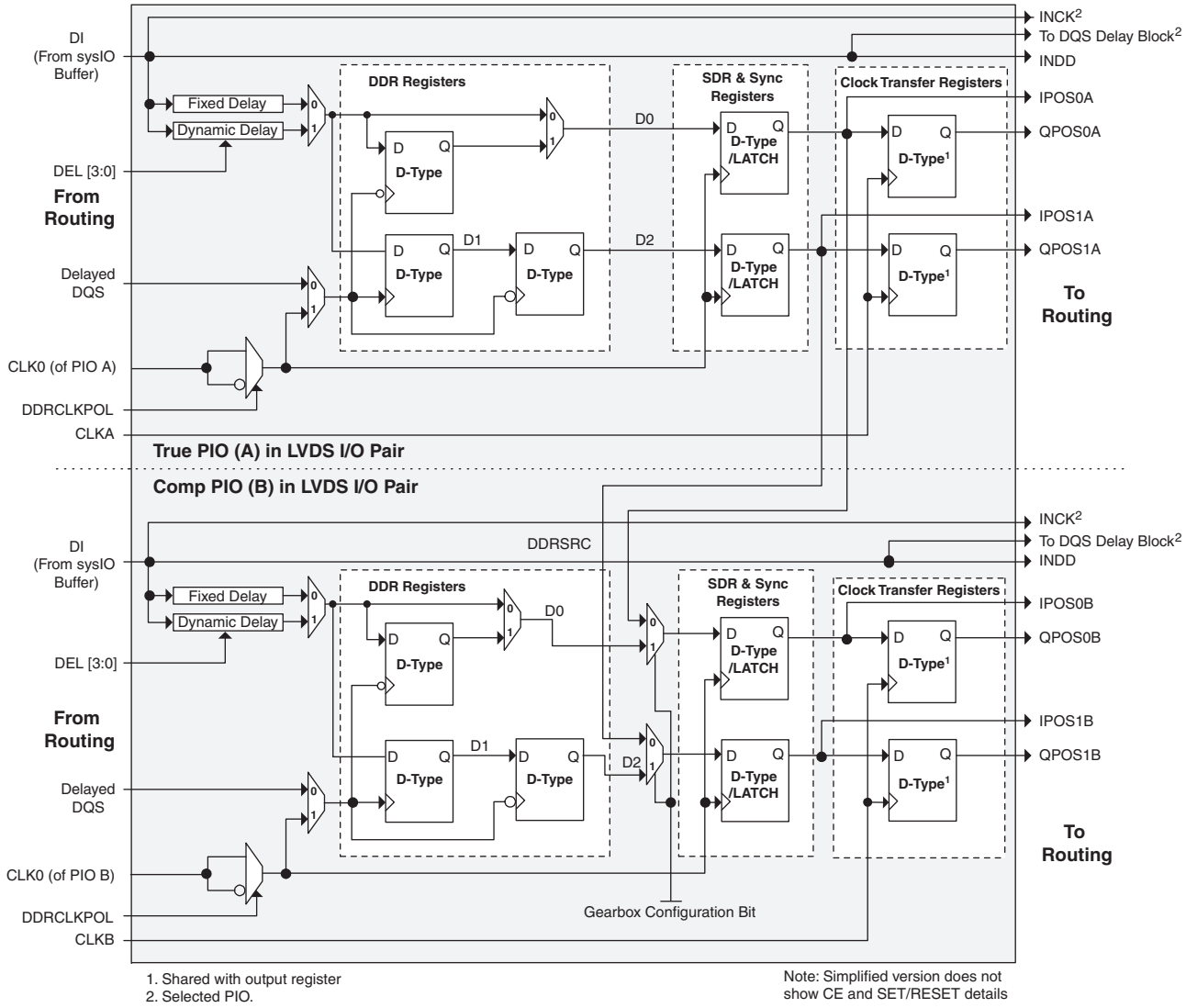


Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Block



1. Shared with output register
2. Selected PIO.

Note: Simplified version does not show CE and SET/RESET details

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

DQSXFER

LA-LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a •exible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

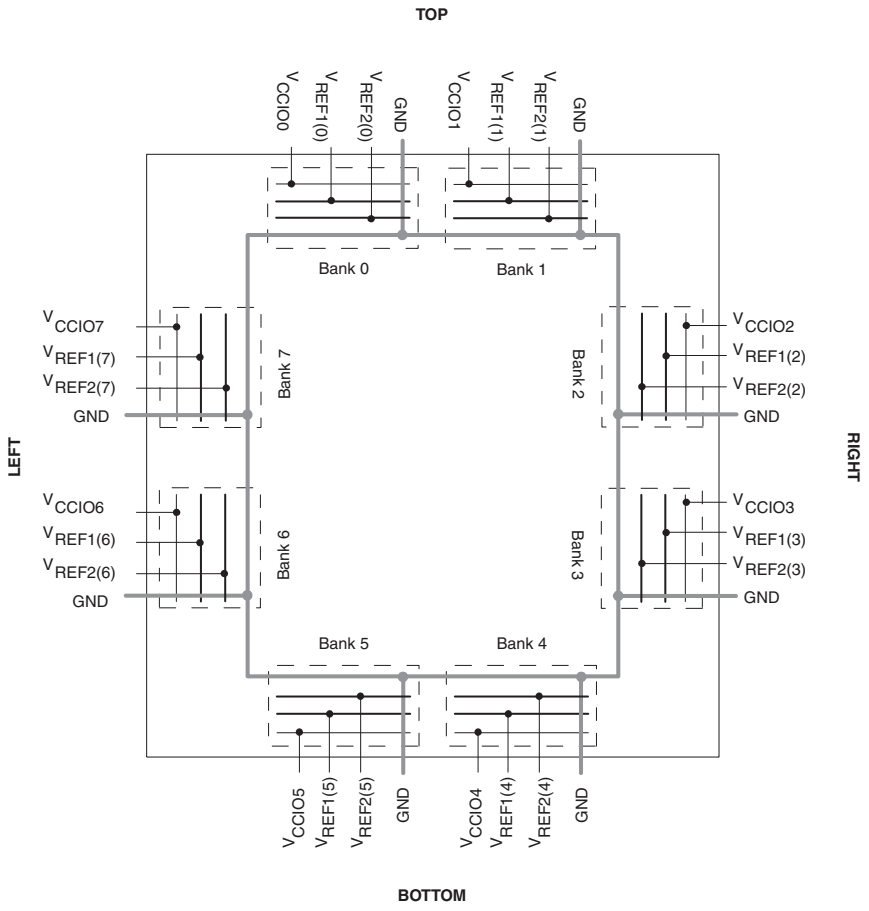
sysIO Buffer Banks

LA-LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2}, that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LA-LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-32. LA-LatticeXP2 Banks



LA-LatticeXP2 devices contain two types of sysIO buffer pairs.

1. **Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. **Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, LatticeXP2 sysIO Usage Guide for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LA-LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Table 2-12 and Table 2-13 show the I/O standards (together with their supply and reference voltages) supported by LA-LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards, see TN1136, LatticeXP2 sysIO Usage Guide.

Table 2-13. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	3.3
LVCMOS33	4 mA, 8 mA, 12 mA 16 mA, 20 mA	3.3
LVCMOS25	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	2.5
LVCMOS18	4 mA, 8 mA, 12 mA, 16 mA	1.8
LVCMOS15	4 mA, 8 mA	1.5
LVCMOS12	2 mA, 6 mA	1.2
LVCMOS33, Open Drain	4 mA, 8 mA, 12 mA 16 mA, 20 mA	—
LVCMOS25, Open Drain	4 mA, 8 mA, 12 mA 16 mA, 20 mA	—
LVCMOS18, Open Drain	4 mA, 8 mA, 12 mA 16 mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL33 Class I, II	N/A	3.3
SSTL25 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL33, Class I, II	N/A	3.3
Differential SSTL25, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS[1, 2]	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5
LVCMOS33D[1]	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	3.3

1. Emulated with external resistors. For more detail, see TN1138, LatticeXP2 High Speed I/O Interface.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LA-LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LA-LatticeXP2 ideal for many multiple power supply and hot-swap applications.

IEEE 1149.1-Compliant Boundary Scan Testability

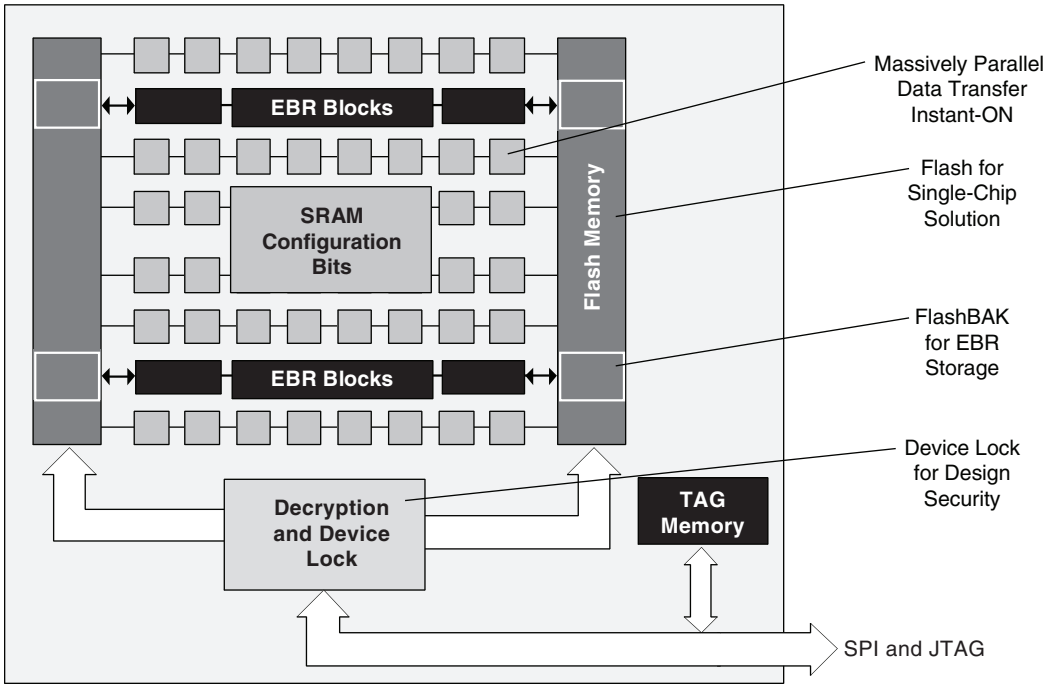
All LA-LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to

be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for veri•cation. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LA-LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.

Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LA-LatticeXP2 Devices



At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:

sysIO Recommended Operating Conditions

Over Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18_I[2], SSTL18_II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I[2], SSTL25_II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I[2], SSTL33_II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I[2], HSTL18_II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], SSTL18D_II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], SSTL25D_II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], SSTL33D_ II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], HSTL18D_ II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

Typical Building Block Function Performance[1]

Over Recommended Operating Conditions

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	5.7	ns
32-bit Decoder	6.9	ns
64-bit Decoder	7.7	ns
4:1 MUX	4.8	ns
8:1 MUX	5.1	ns
16:1 MUX	5.6	ns
32:1 MUX	5.8	ns

Register-to-Register Performance

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	354	MHz
32-bit Decoder	318	MHz
64-bit Decoder	280	MHz
4:1 MUX	493	MHz
8:1 MUX	458	MHz
16:1 MUX	424	MHz
32:1 MUX	364	MHz
8-bit Adder	326	MHz
16-bit Adder	306	MHz
64-bit Adder	178	MHz
16-bit Counter	312	MHz
32-bit Counter	257	MHz
64-bit Counter	191	MHz
64-bit Accumulator	161	MHz
Embedded Memory Functions		
512 x 36 Single Port RAM, EBR Output Registers	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	173	MHz
Distributed Memory Functions		
16 x 4 Pseudo-Dual Port RAM (One PFU)	508	MHz
32 x 2 Pseudo-Dual Port RAM	313	MHz
64 x 1 Pseudo-Dual Port RAM	235	MHz
DSP Functions		
18 x 18 Multiplier (All Registers)	276	MHz
9 x 9 Multiplier (All Registers)	276	MHz
36 x 36 Multiply (All Registers)	244	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	176	MHz
18 x 18 Multiply-Add/Sub-Sum (All Registers)	235	MHz

LA-LatticeXP2 Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	–5		Units
		Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.217	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.178	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	–0.131	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchronous)	—	1.544	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	–0.159	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.209	—	ns
t_{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.351	—	ns
t_{RST_EBR}	Asynchronous reset time for EBR	—	1.544	ns
PLL Parameters				
$t_{RSTKREC\_PLL}$	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.012	—	ns
t_{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only[2])	1.012	—	ns
DSP Block Timing				
t_{SUI_DSP}	Input Register Setup Time	0.168	—	ns
t_{HI_DSP}	Input Register Hold Time	–0.031	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	3.101	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	–1.006	—	ns
t_{SUO_DSP}	Output Register Setup Time	6.002	—	ns
t_{HO_DSP}	Output Register Hold Time	–1.791	—	ns
t_{COI_DSP}[3]	Input Register Clock to Output Time	—	5.447	ns
t_{COP_DSP}[3]	Pipeline Register Clock to Output Time	—	2.420	ns
t_{COO_DSP}[3]	Output Register Clock to Output Time	—	0.639	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	–0.331	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.375	—	ns

1. Internal parameters are characterized, but not tested on every device.
2. RST resets VCO and all counters in PLL.
3. These parameters include the Adder Subtractor block in the path.

Timing v. A 0.12

LA-LatticeXP2 Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
Input Adjusters			
LVDS25	LVDS	0.05	ns
BLVDS25	BLVDS	0.05	ns
MLVDS	LVDS	0.05	ns
RSDS	RSDS	0.05	ns
LVPECL33	LVPECL	0.05	ns
HSTL18_I	HSTL_18 class I	0.07	ns
HSTL18_II	HSTL_18 class II	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	0.02	ns
HSTL15_I	HSTL_15 class I	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	ns
SSTL33_I	SSTL_3 class I	0.12	ns
SSTL33_II	SSTL_3 class II	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	0.04	ns
SSTL25_I	SSTL_2 class I	0.10	ns
SSTL25_II	SSTL_2 class II	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	0.03	ns
SSTL18_I	SSTL_18 class I	0.07	ns
SSTL18_II	SSTL_18 class II	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	0.02	ns
LVTTL33	LVTTL	0.19	ns
LVCMOS33	LVCMOS 3.3	0.19	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.17	ns
LVCMOS12	LVCMOS 1.2	-0.04	ns
PCI33	3.3V PCI	0.19	ns
Output Adjusters			
LVDS25E	LVDS 2.5 E[4]	0.32	ns
LVDS25	LVDS 2.5	0.32	ns
BLVDS25	BLVDS 2.5	0.29	ns
MLVDS	MLVDS 2.5[4]	0.29	ns
RSDS	RSDS 2.5[4]	0.32	ns
LVPECL33	LVPECL 3.3[4]	0.19	ns
HSTL18_I	HSTL_18 class I 8mA drive	0.45	ns
HSTL18_II	HSTL_18 class II	0.31	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	0.45	ns
HSTL18D_II	Differential HSTL 18 class II	0.31	ns

LA-LatticeXP2 Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	1.60	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.40	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.63	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.41	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.84	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.52	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.32	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.55	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	1.79	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	0.01	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	1.73	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.02	ns
PCI33	3.3V PCI	0.27	ns

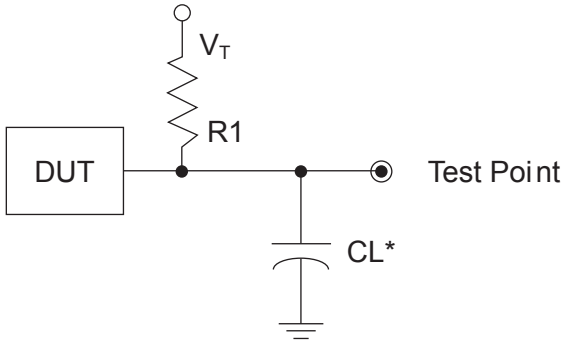
1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.

Timing v. A 0.12

Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The speci•c values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary (Continued)

Pin Type		LA-XP2-5				LA-XP2-8				LA-XP2-17	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA
DDR Banks Bonding Out per I/O Bank[1]	Bank0	1	1	1	1	1	1	1	1	1	1
	Bank1	0	0	1	1	0	0	1	1	1	1
	Bank2	1	1	1	1	1	1	1	1	1	1
	Bank3	0	0	1	1	0	0	1	1	1	1
	Bank4	0	0	1	1	0	0	1	1	1	1
	Bank5	1	1	1	1	1	1	1	1	1	1
	Bank6	0	0	1	1	0	0	1	1	1	1
	Bank7	1	1	1	1	1	1	1	1	1	1
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28
	Bank1	4	6	18	18	4	6	18	22	18	22
	Bank2	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26
	Bank5	14	18	20	24	14	18	20	24	20	24
	Bank6	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found on the LatticeXP2 product pages on the Lattice website at www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package-specific thermal values.

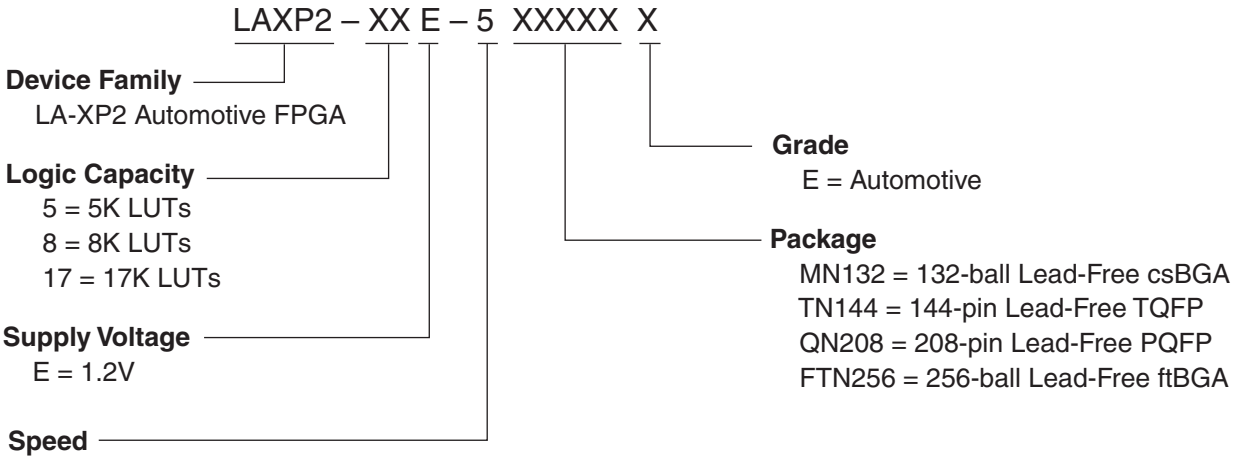
For Further Information

- TN1139 - Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool included with Lattice Diamond design software or as a standalone download from www.latticesemi.com/software

LA-LatticeXP2 Family Data Sheet Ordering Information

August 2014 Data Sheet DS1024

Part Number Description



Ordering Information

The LA-LatticeXP2 devices are marked with a single automotive temperature grade, as shown below.

Automotive Disclaimer

Products are not designed, intended or warranted to be fail-safe and are not designed, intended or warranted for use in applications related to the deployment of airbags. Further, products are not intended to be used, designed or warranted for use in applications that affect the control of the vehicle unless there is a fail-safe or redundancy feature and also a warning signal to the operator of the vehicle upon failure. Use of products in such applications is fully at the risk of the customer, subject to applicable laws and regulations governing limitations on product liability.

Lead-Free Packaging

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-5E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	5
LAXP2-5E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	5
LAXP2-5E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	5
LAXP2-5E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-8E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	8
LAXP2-8E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	8
LAXP2-8E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	8
LAXP2-8E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-17E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	17
LAXP2-17E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	17

LA-LatticeXP2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LA-LatticeXP2 FPGA family are available on the Lattice website.

- TN1136, LatticeXP2 sysIO Usage Guide
- TN1137, LatticeXP2 Memory Usage Guide
- TN1138, LatticeXP2 High Speed I/O Interface
- TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide
- TN1139, Power Estimation and Management for LatticeXP2 Devices
- TN1140, LatticeXP2 sysDSP Usage Guide
- TN1141, LatticeXP2 sysCONFIG Usage Guide
- TN1142, LatticeXP2 Configuration Encryption and Security Usage Guide
- TN1143, LatticeXP2 TransFR I/O
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- TN1220, LatticeXP2 Dual Boot Feature
- TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com