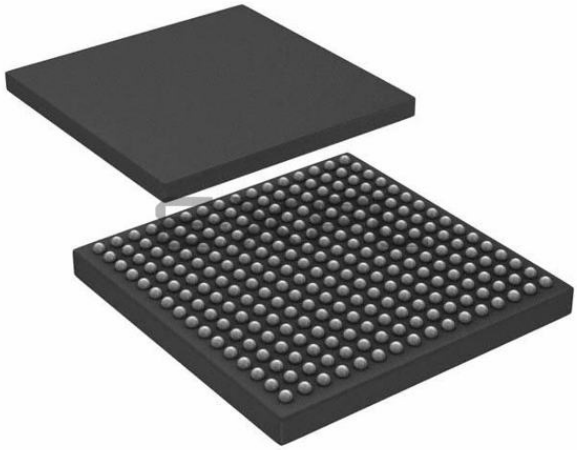
Lattice Semiconductor Corporation - LAXP2-5E-5FTN256E Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	172
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-5e-5ftn256e

LA-LatticeXP2 Family Data Sheet Introduction

February 2015 Data Sheet DS1024

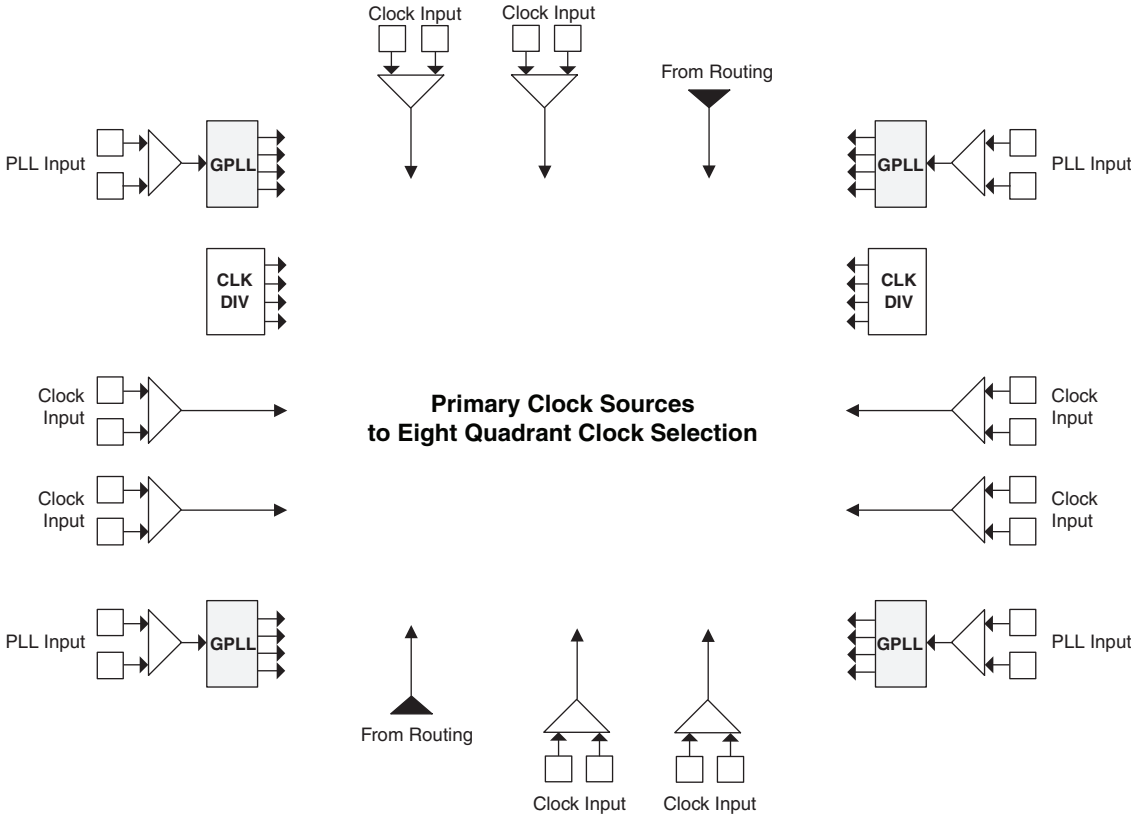
Features

- **flexiFLASH™ Architecture**
  - Instant-on
  - Infinitely reconfigurable
  - Single chip
  - FlashBAK™ technology
  - Serial TAG memory
  - Design security
- **AEC-Q100 Tested and Qualified**
- **Live Update Technology**
  - TransFR™ technology
  - Secure updates with 128 bit AES encryption
  - Dual-boot with external SPI
- **sysDSP™ Block**
  - Three to five blocks for high performance Multiply and Accumulate
  - 12 to 20 18 x 18 multipliers
  - Each block supports one 36 x 36 multiplier or four 18 x 18 or eight 9 x 9 multipliers
- **Embedded and Distributed Memory**
  - Up to 276 kbits sysMEM™ EBR
  - Up to 35 kbits Distributed RAM
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **Flexible I/O Buffer**
  - sysIO™ buffer supports:
    - LVCMOS 33/25/18/15/12; LVTTL
    - SSTL 33/25/18 class I, II
    - HSTL15 class I; HSTL18 class I, II
    - PCI
    - LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- **Pre-engineered Source Synchronous Interfaces**
  - DDR / DDR2 interfaces up to 200 MHz
  - 7:1 LVDS interfaces support display applications
  - XGMII
- **Density And Package Options**
  - 5k to 17k LUT4s, 86 to 358 I/Os
  - csBGA, ftBGA, TQFP and PQFP packages
  - Density migration supported
- **Flexible Device Configuration**
  - SPI (master and slave) Boot Flash Interface
  - Dual Boot Image supported
  - Soft Error Detect (SED) macro embedded
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 Compliant
  - On-chip oscillator for initialization & general use
  - Devices operate with 1.2 V power supply

Table 1-1. LA-LatticeXP2 Family Selection Guide

Device	LA-XP2-5	LA-XP2-8	LA-XP2-17
LUTs (K)	5	8	17
Distributed RAM (kbits)	10	18	35
EBR SRAM (kbits)	166	221	276
EBR SRAM Blocks	9	12	15
sysDSP Blocks	3	4	5
18 x 18 Multipliers	12	16	20
V_{CC} Voltage	1.2	1.2	1.2
GPLL	2	2	4
Max Available I/O	172	201	201
Packages and I/O Combinations			
132-Ball csBGA (8 x 8 mm)	86	86	
144-Pin TQFP (20 x 20 mm)	100	100	
208-Pin PQFP (28 x 28 mm)	146	146	146
256-Ball ftBGA (17 x17 mm)	172	201	201

Figure 2-6. Primary Clock Sources for LatticeXP2-17

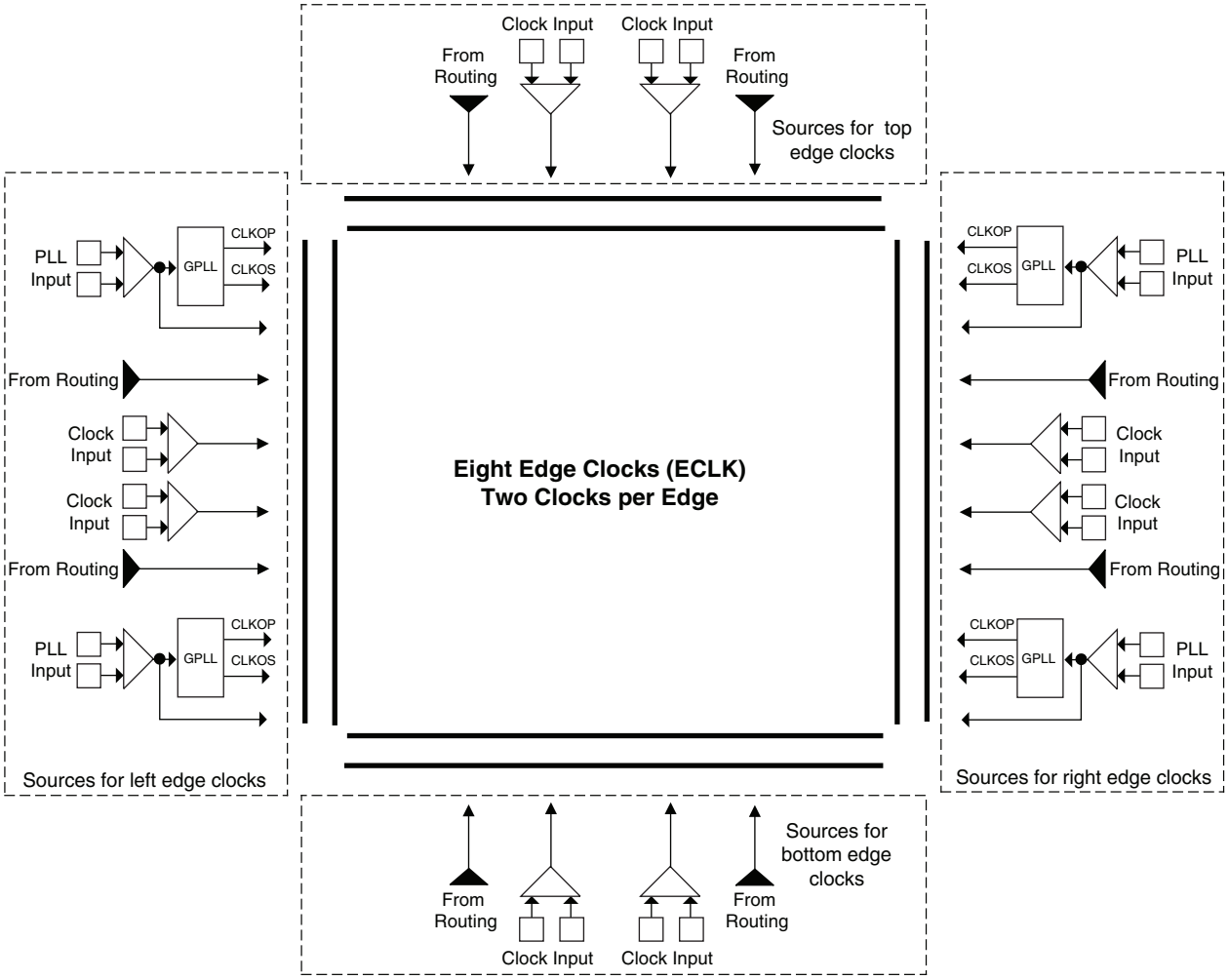


Note: This diagram shows sources for the LA-LatticeXP2-17 device. Smaller LA-LatticeXP2 devices have two GPLLs.

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs and clock dividers as shown in Figure 2-8.

Figure 2-8. Edge Clock Sources



Note: This diagram shows sources for the LA-LatticeXP2-17 device. Smaller LA-LatticeXP2 devices have two GPLLs.

EBR memory supports two forms of write behavior for single port or dual port operation:

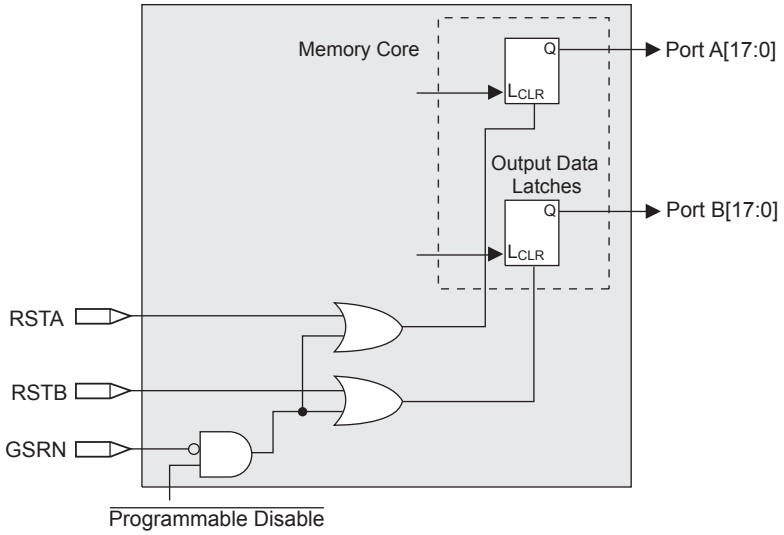
1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset

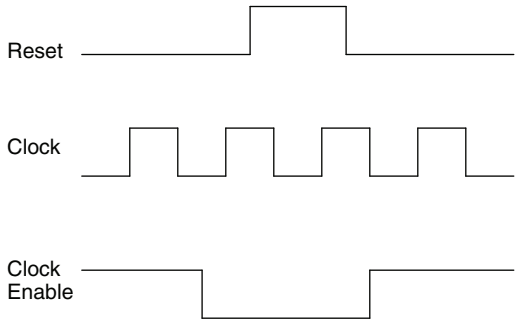


For further information on the sysMEM EBR block, see TN1137, LatticeXP2 Memory Usage Guide.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.

Figure 2-18. EBR Asynchronous Reset (Including GSR) Timing Diagram



IPexpress™

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LA-LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LA-LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LA-LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LA-LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-8. Maximum Number of DSP Blocks in the LA-LatticeXP2 Family

Device	DSP Block	9 x 9 Multiplier	18 x 18 Multiplier	36 x 36 Multiplier
LA-XP2-5	3	24	12	3
LA-XP2-8	4	32	16	4
LA-XP2-17	5	40	20	5

Table 2-9. Embedded SRAM/TAG Memory in the LA-LatticeXP2 Family

Device	EBR SRAM Block	Total EBR SRAM (kbits)	TAG Memory (Bits)
LA-XP2-5	9	166	632
LA-XP2-8	12	221	768
LA-XP2-17	15	276	2184

LA-LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LA-LatticeXP2 family.

Table 2-10. DSP Performance

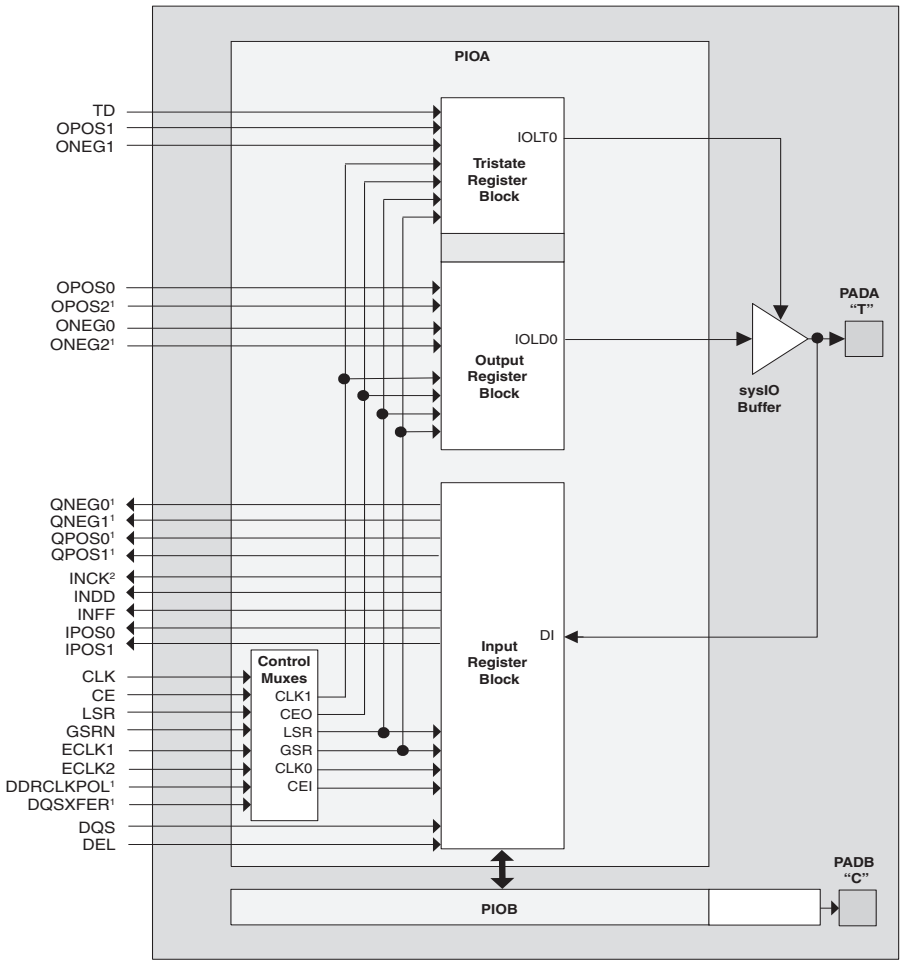
Device	DSP Block	DSP Performance MMAC
LA-XP2-5	3	3,900
LA-XP2-8	4	5,200
LA-XP2-17	5	6,500

For further information on the sysDSP block, see TN1140, LatticeXP2 sysDSP Usage Guide.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Table 2-11. PIO Signal List

Name	Type	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK[2]	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0[1], QPOS1[1]	Input to the core	Gearbox pipelined inputs to the core
QNEG0[1], QNEG1[1]	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.
2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.

DQSXFER

LA-LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a •exible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

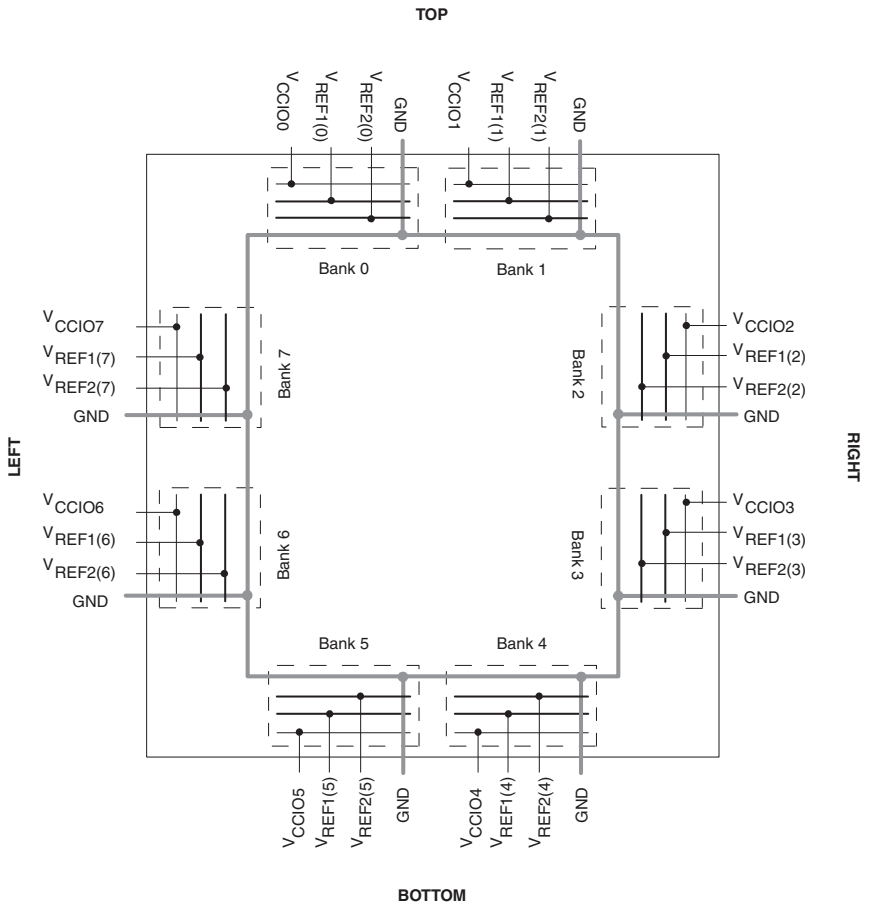
sysIO Buffer Banks

LA-LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2}, that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LA-LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-32. LA-LatticeXP2 Banks



Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/–1	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.

ESD Performance

Please refer to the LatticeXP2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
		$V_{CCIO} \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{CCIO}$	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin con•gured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.

Initialization Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25 °C, Max. Supply)[6]	Units
I_{CC}	Core Power Supply Current	LA-XP2-5	20	mA
		LA-XP2-8	21	mA
		LA-XP2-17	44	mA
I_{CCAUX}	Auxiliary Power Supply Current[7]	LA-XP2-5	67	mA
		LA-XP2-8	74	mA
		LA-XP2-17	112	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
I_{CCJ}	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are con•gured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Does not include additional current from bypass or decoupling capacitor across the supply.
5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
6. T_J = 25 °C, power supplies at nominal voltage.
7. In fpBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and $I_{CCPLL.}$ For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25 °C, Max. Supply)[6]	Units
I_{CC}	Core Power Supply Current	LA-XP2-5	17	mA
		LA-XP2-8	21	mA
		LA-XP2-17	28	mA
I_{CCAUX}	Auxiliary Power Supply Current[7]	LA-XP2-5	64	mA
		LA-XP2-8	66	mA
		LA-XP2-17	83	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I_{CCJ}	V_{CCJ} Power Supply Current[8]		14	mA

1. For further information on supply current, see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are con•gured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz (excludes dynamic power from FPGA operation).
4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
5. Bypass or decoupling capacitor across the supply.
6. T_J = 25 °C, power supplies at nominal voltage.
7. In fpBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
8. When programming via JTAG.

LVPECL

The LA-LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

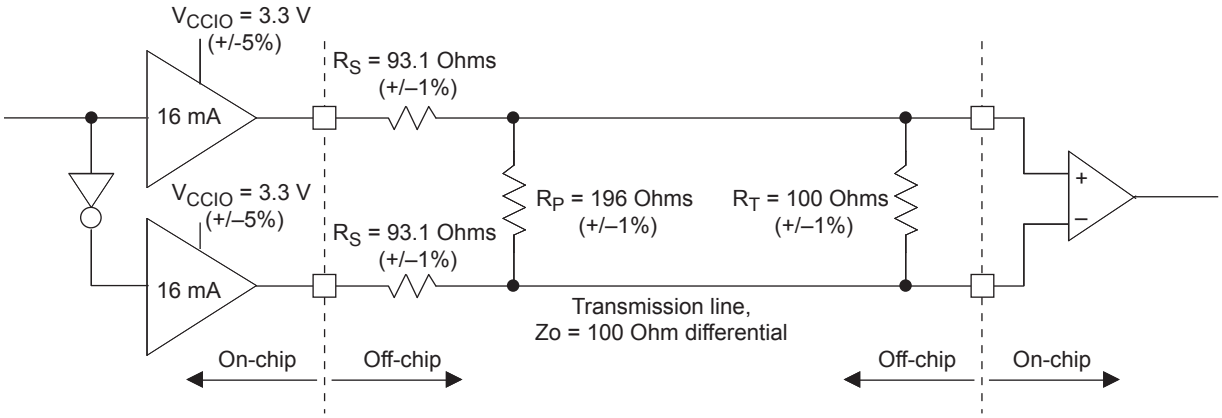


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/–1%)	93	Ω
R_P	Driver Parallel Resistor (+/–1%)	196	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage (After R_P)	2.05	V
V_{OL}	Output Low Voltage (After R_P)	1.25	V
V_{OD}	Output Differential Voltage (After R_P)	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance[1]

Over Recommended Operating Conditions

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	5.7	ns
32-bit Decoder	6.9	ns
64-bit Decoder	7.7	ns
4:1 MUX	4.8	ns
8:1 MUX	5.1	ns
16:1 MUX	5.6	ns
32:1 MUX	5.8	ns

Register-to-Register Performance

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	354	MHz
32-bit Decoder	318	MHz
64-bit Decoder	280	MHz
4:1 MUX	493	MHz
8:1 MUX	458	MHz
16:1 MUX	424	MHz
32:1 MUX	364	MHz
8-bit Adder	326	MHz
16-bit Adder	306	MHz
64-bit Adder	178	MHz
16-bit Counter	312	MHz
32-bit Counter	257	MHz
64-bit Counter	191	MHz
64-bit Accumulator	161	MHz
Embedded Memory Functions		
512 x 36 Single Port RAM, EBR Output Registers	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	173	MHz
Distributed Memory Functions		
16 x 4 Pseudo-Dual Port RAM (One PFU)	508	MHz
32 x 2 Pseudo-Dual Port RAM	313	MHz
64 x 1 Pseudo-Dual Port RAM	235	MHz
DSP Functions		
18 x 18 Multiplier (All Registers)	276	MHz
9 x 9 Multiplier (All Registers)	276	MHz
36 x 36 Multiply (All Registers)	244	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	176	MHz
18 x 18 Multiply-Add/Sub-Sum (All Registers)	235	MHz

LA-LatticeXP2 External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	–5		Units
			Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[1]					
t_{CO}	Clock to Output - PIO Output Register	LA-XP2-5	—	4.77	ns
		LA-XP2-8	—	4.77	ns
		LA-XP2-17	—	4.78	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LA-XP2-5	-0.06	—	ns
		LA-XP2-8	-0.06	—	ns
		LA-XP2-17	-0.06	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.98	—	ns
		LA-XP2-8	1.99	—	ns
		LA-XP2-17	1.99	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	1.87	—	ns
		LA-XP2-8	1.87	—	ns
		LA-XP2-17	1.86	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.06	—	ns
		LA-XP2-8	0.06	—	ns
		LA-XP2-17	0.07	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LA-XP2	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)[1]					
t_{COE}	Clock to Output - PIO Output Register	LA-XP2-5	—	4.00	ns
		LA-XP2-8	—	4.00	ns
		LA-XP2-17	—	4.00	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.62	—	ns
		LA-XP2-8	1.62	—	ns
		LA-XP2-17	1.62	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	1.62	—	ns
		LA-XP2-8	1.62	—	ns
		LA-XP2-17	1.62	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	LA-XP2	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]					
t_{COPLL}	Clock to Output - PIO Output Register	LA-XP2-5	—	3.80	ns
		LA-XP2-8	—	3.80	ns
		LA-XP2-17	—	3.80	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LA-XP2-5	1.25	—	ns
		LA-XP2-8	1.27	—	ns
		LA-XP2-17	1.23	—	ns

LA-LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	–5		Units
			Min.	Max.	
t_{HPLL}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.32	—	ns
		LA-XP2-8	1.32	—	ns
		LA-XP2-17	1.32	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	2.16	—	ns
		LA-XP2-8	2.18	—	ns
		LA-XP2-17	2.14	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
DDR[2] and DDR2[3] I/O Pin Parameters					
t_{DVADQ}	Data Valid After DQS (DDR Read)	LA-XP2	—	0.29	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	LA-XP2	0.71	—	UI
t_{DQVBS}	Data Valid Before DQS	LA-XP2	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	LA-XP2	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	LA-XP2	95	133	MHz
f_{MAX_DDR2}	DDR Clock Frequency	LA-XP2	133	166	MHz
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	LA-XP2	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	LA-XP2	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	LA-XP2	—	160	ps
Edge Clock (ECLK1 and ECLK2)					
f_{MAX_ECLK}	Frequency for Edge Clock	LA-XP2	—	311	MHz
t_{W_ECLK}	Clock Pulse Width for Edge Clock	LA-XP2	1	—	ns
t_{SKEW_ECLK}	Edge Clock Skew Within an Edge of the Device	LA-XP2	—	130	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25.
3. DDR2 timing numbers based on SSTL18.

Timing v. A 0.12

LA-LatticeXP2 Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
Input Adjusters			
LVDS25	LVDS	0.05	ns
BLVDS25	BLVDS	0.05	ns
MLVDS	LVDS	0.05	ns
RSDS	RSDS	0.05	ns
LVPECL33	LVPECL	0.05	ns
HSTL18_I	HSTL_18 class I	0.07	ns
HSTL18_II	HSTL_18 class II	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	0.02	ns
HSTL15_I	HSTL_15 class I	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	ns
SSTL33_I	SSTL_3 class I	0.12	ns
SSTL33_II	SSTL_3 class II	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	0.04	ns
SSTL25_I	SSTL_2 class I	0.10	ns
SSTL25_II	SSTL_2 class II	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	0.03	ns
SSTL18_I	SSTL_18 class I	0.07	ns
SSTL18_II	SSTL_18 class II	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	0.02	ns
LVTTL33	LVTTL	0.19	ns
LVCMOS33	LVCMOS 3.3	0.19	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.17	ns
LVCMOS12	LVCMOS 1.2	-0.04	ns
PCI33	3.3V PCI	0.19	ns
Output Adjusters			
LVDS25E	LVDS 2.5 E[4]	0.32	ns
LVDS25	LVDS 2.5	0.32	ns
BLVDS25	BLVDS 2.5	0.29	ns
MLVDS	MLVDS 2.5[4]	0.29	ns
RSDS	RSDS 2.5[4]	0.32	ns
LVPECL33	LVPECL 3.3[4]	0.19	ns
HSTL18_I	HSTL_18 class I 8mA drive	0.45	ns
HSTL18_II	HSTL_18 class II	0.31	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	0.45	ns
HSTL18D_II	Differential HSTL 18 class II	0.31	ns

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCPLL}	—	PLL supply pins. csBGA, PQFP and TQFP packages only.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V_{CCPLL}	—	Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.

Signal Descriptions (Continued)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN[1]	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI[2]	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI[2]	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN[2]	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10k ohms is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

Pin Information Summary (Continued)

Pin Type		LA-XP2-5				LA-XP2-8				LA-XP2-17	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA
DDR Banks Bonding Out per I/O Bank[1]	Bank0	1	1	1	1	1	1	1	1	1	1
	Bank1	0	0	1	1	0	0	1	1	1	1
	Bank2	1	1	1	1	1	1	1	1	1	1
	Bank3	0	0	1	1	0	0	1	1	1	1
	Bank4	0	0	1	1	0	0	1	1	1	1
	Bank5	1	1	1	1	1	1	1	1	1	1
	Bank6	0	0	1	1	0	0	1	1	1	1
	Bank7	1	1	1	1	1	1	1	1	1	1
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28
	Bank1	4	6	18	18	4	6	18	22	18	22
	Bank2	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26
	Bank5	14	18	20	24	14	18	20	24	20	24
	Bank6	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found on the LatticeXP2 product pages on the Lattice website at www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package-specific thermal values.

For Further Information

- TN1139 - Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool included with Lattice Diamond design software or as a standalone download from www.latticesemi.com/software

Lead-Free Packaging

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-5E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	5
LAXP2-5E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	5
LAXP2-5E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	5
LAXP2-5E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-8E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	8
LAXP2-8E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	8
LAXP2-8E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	8
LAXP2-8E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-17E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	17
LAXP2-17E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	17