Lattice Semiconductor Corporation - LAXP2-5E-5TN144E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

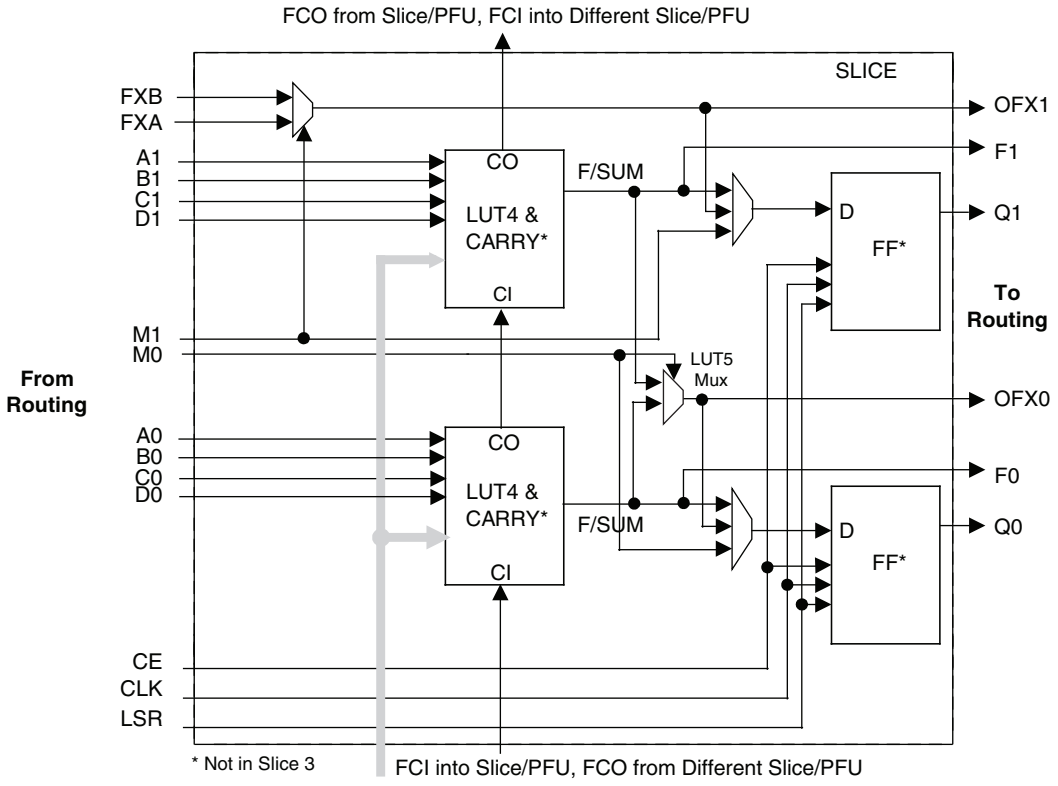
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-5e-5tn144e

Figure 2-3. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from Slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four-input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LA-LatticeXP2 devices, see TN1137, LatticeXP2 Memory Usage Guide.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LA-LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LA-LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LA-LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.

Figure 2-4. General Purpose PLL (GPLL) Diagram

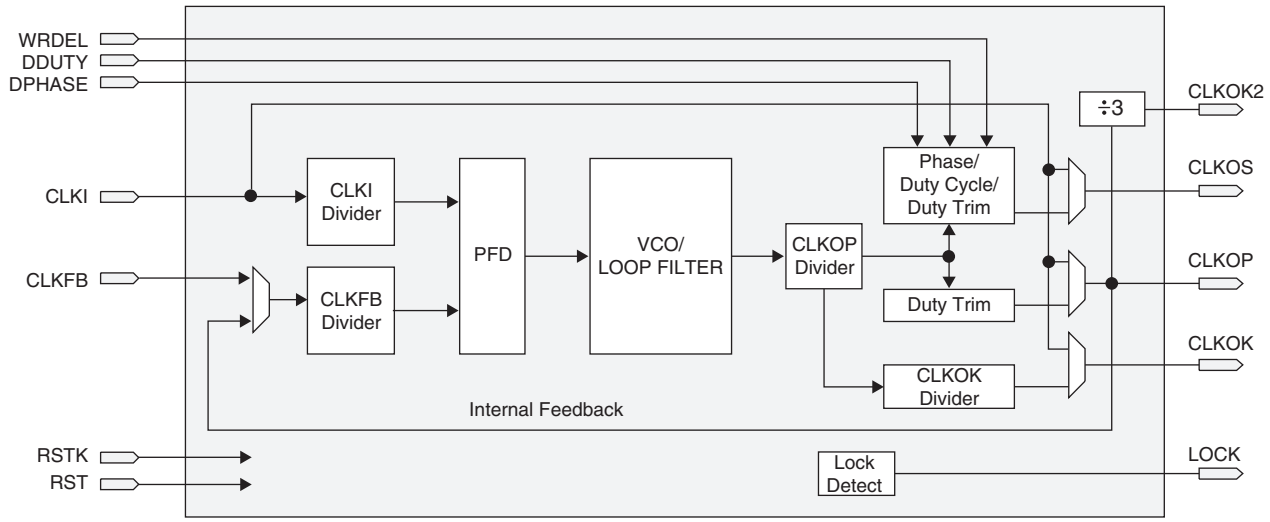


Table 2-4 provides a description of the signals in the GPLL blocks.

Table 2-4. GPLL Block Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

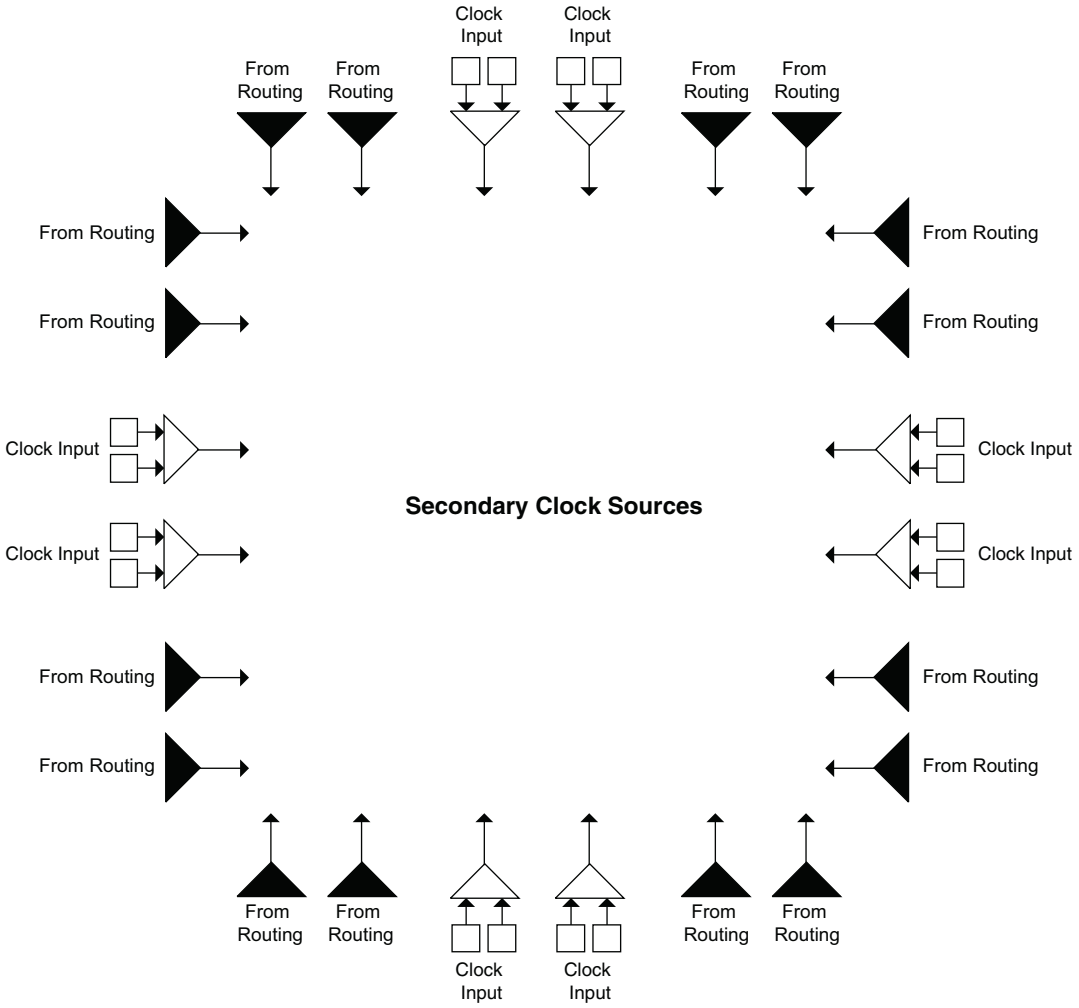
Clock Dividers

LA-LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.

Secondary Clock/Control Sources

LA-LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

Figure 2-7. Secondary Clock Sources



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice 0 through Slice 2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice 0 through Slice 2 Clock Selection

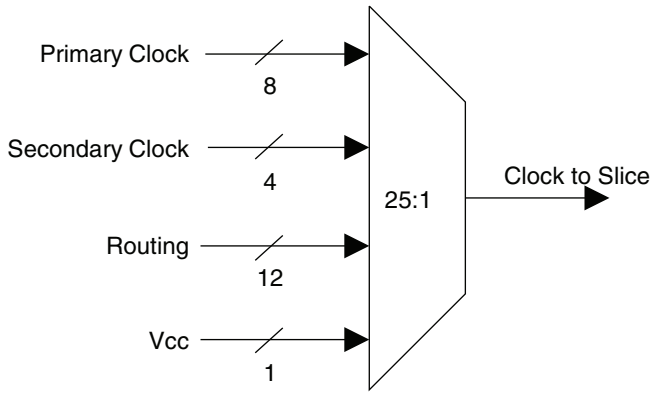
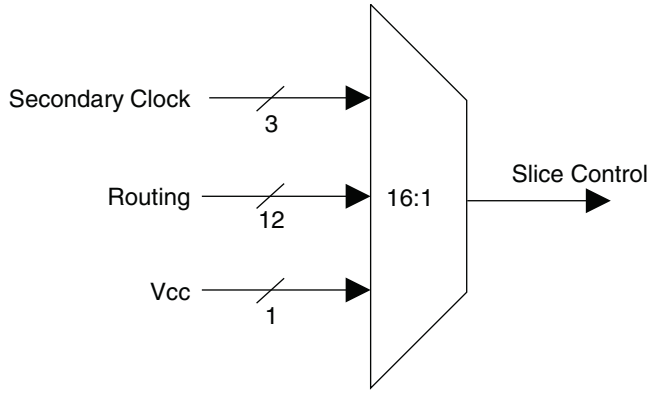


Figure 2-14. Slice 0 through Slice 2 Control Selection



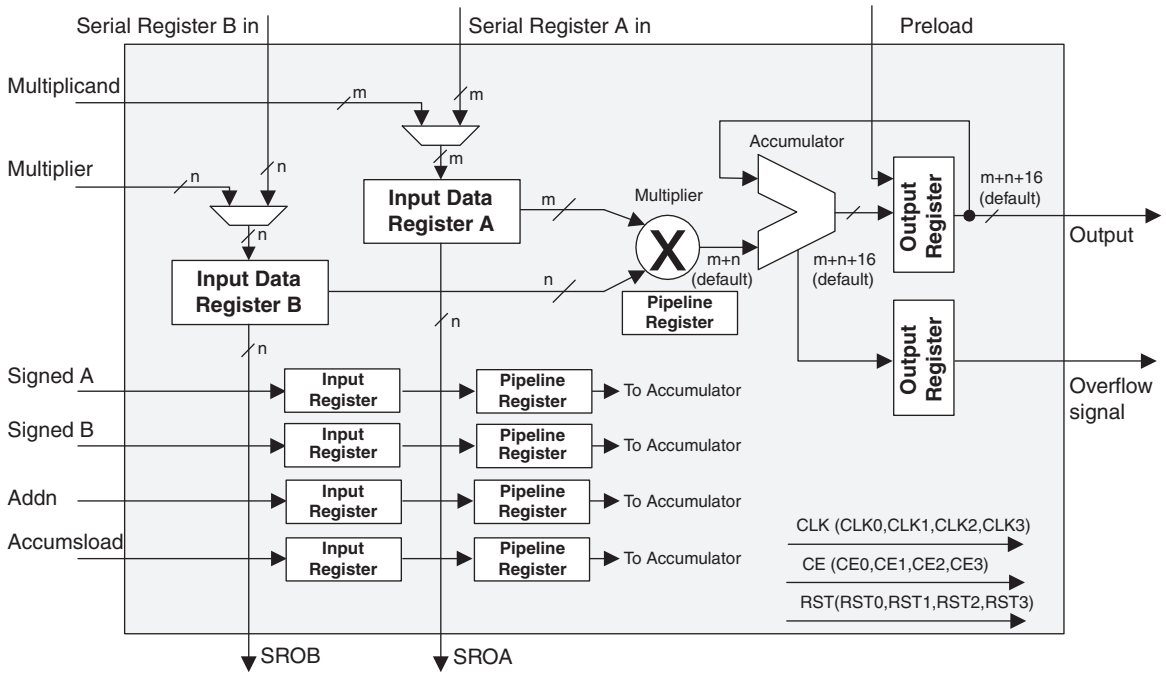
Edge Clock Routing

LA-LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2-15 shows the selection muxes for these clocks.

MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LA-LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The over• ow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

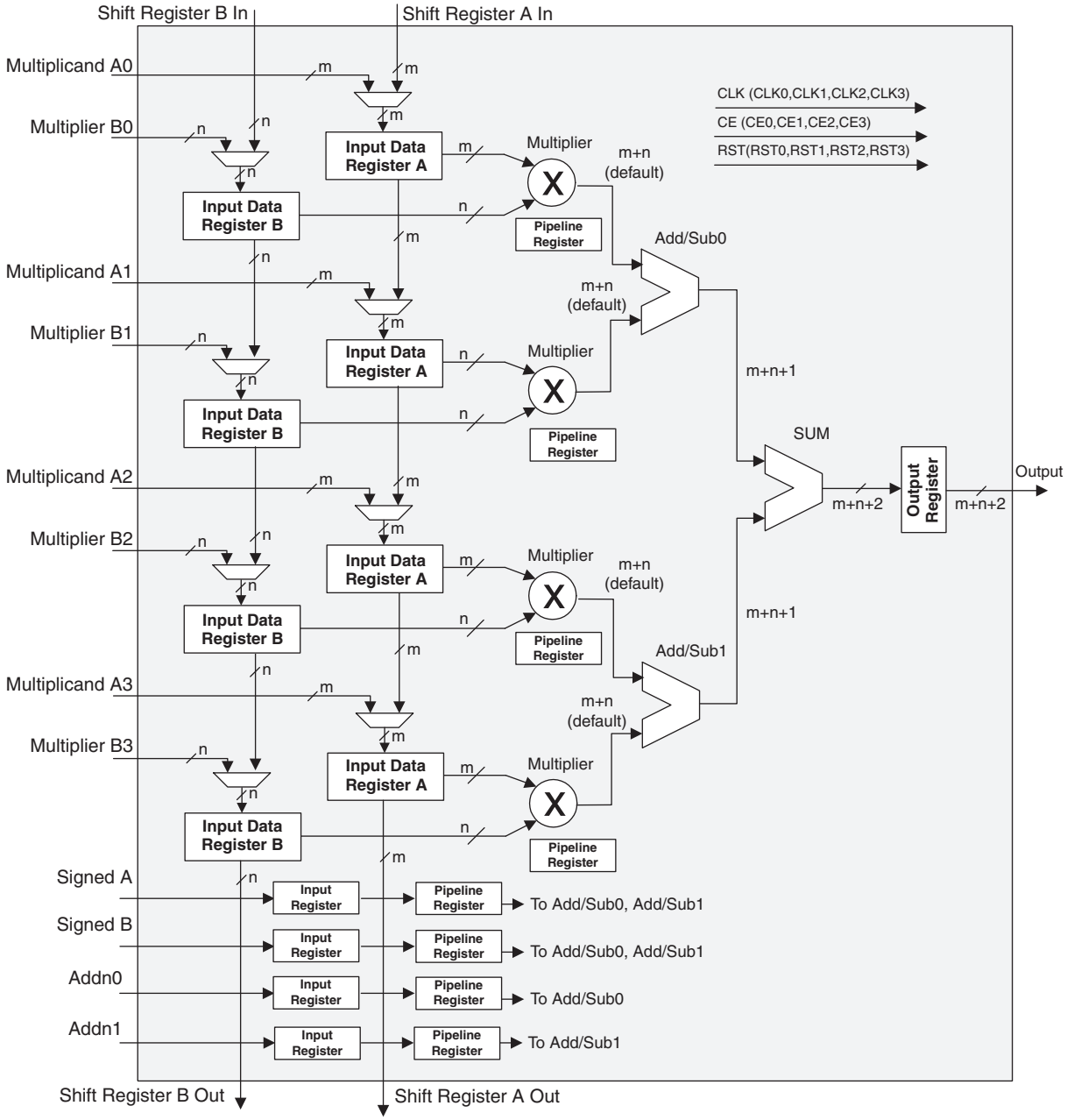
Figure 2-21. MAC sysDSP



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output

shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.

Figure 2-27. Output and Tristate Block

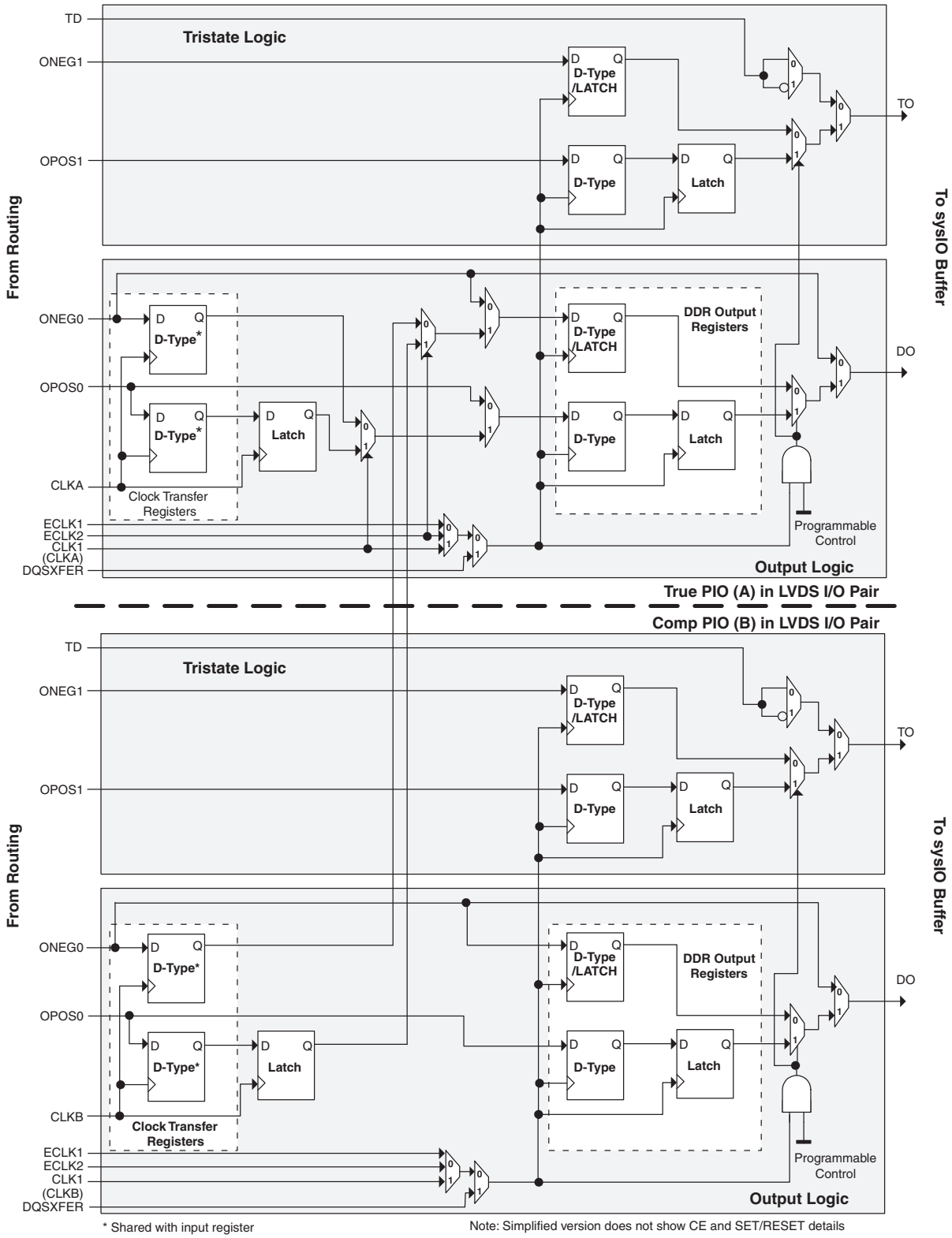


Figure 2-28. DQS Input Routing (Left and Right)

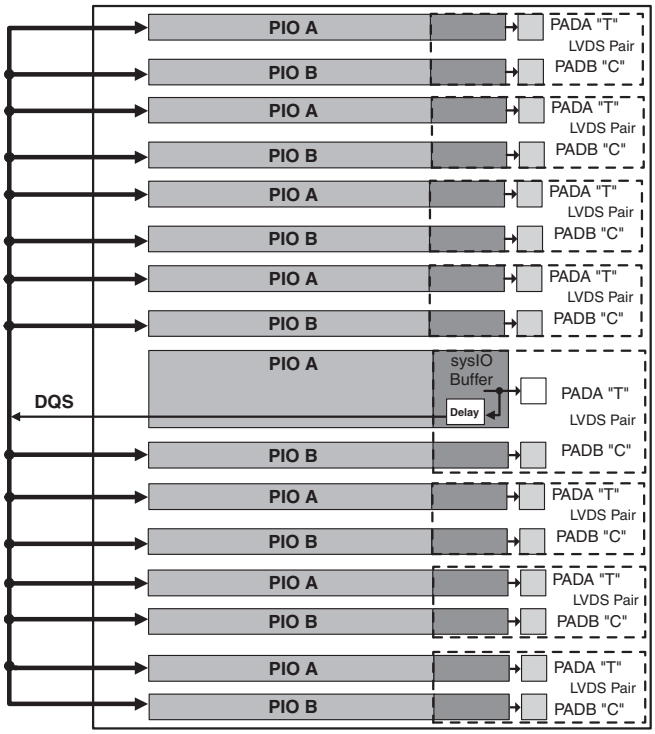


Figure 2-29. DQS Input Routing (Top and Bottom)

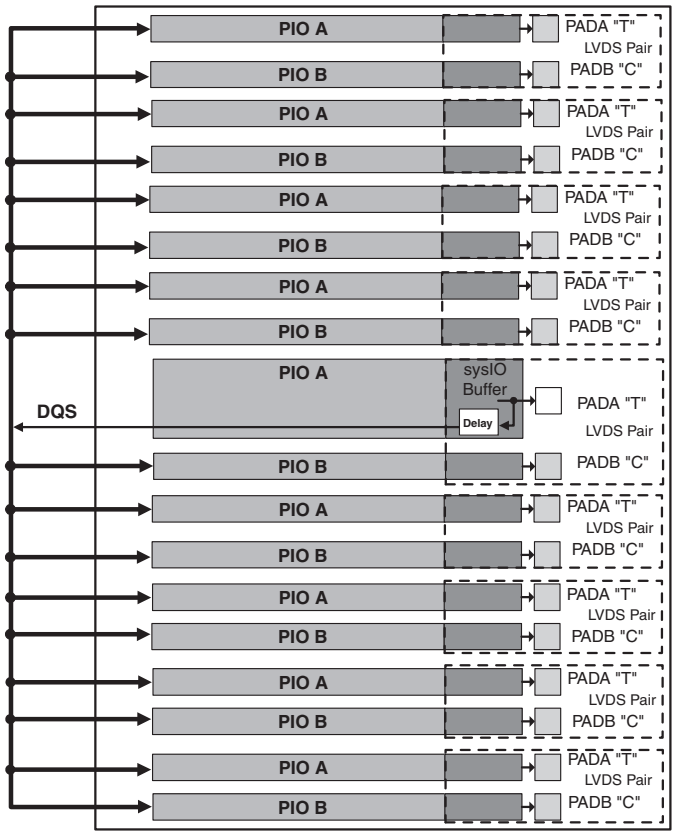
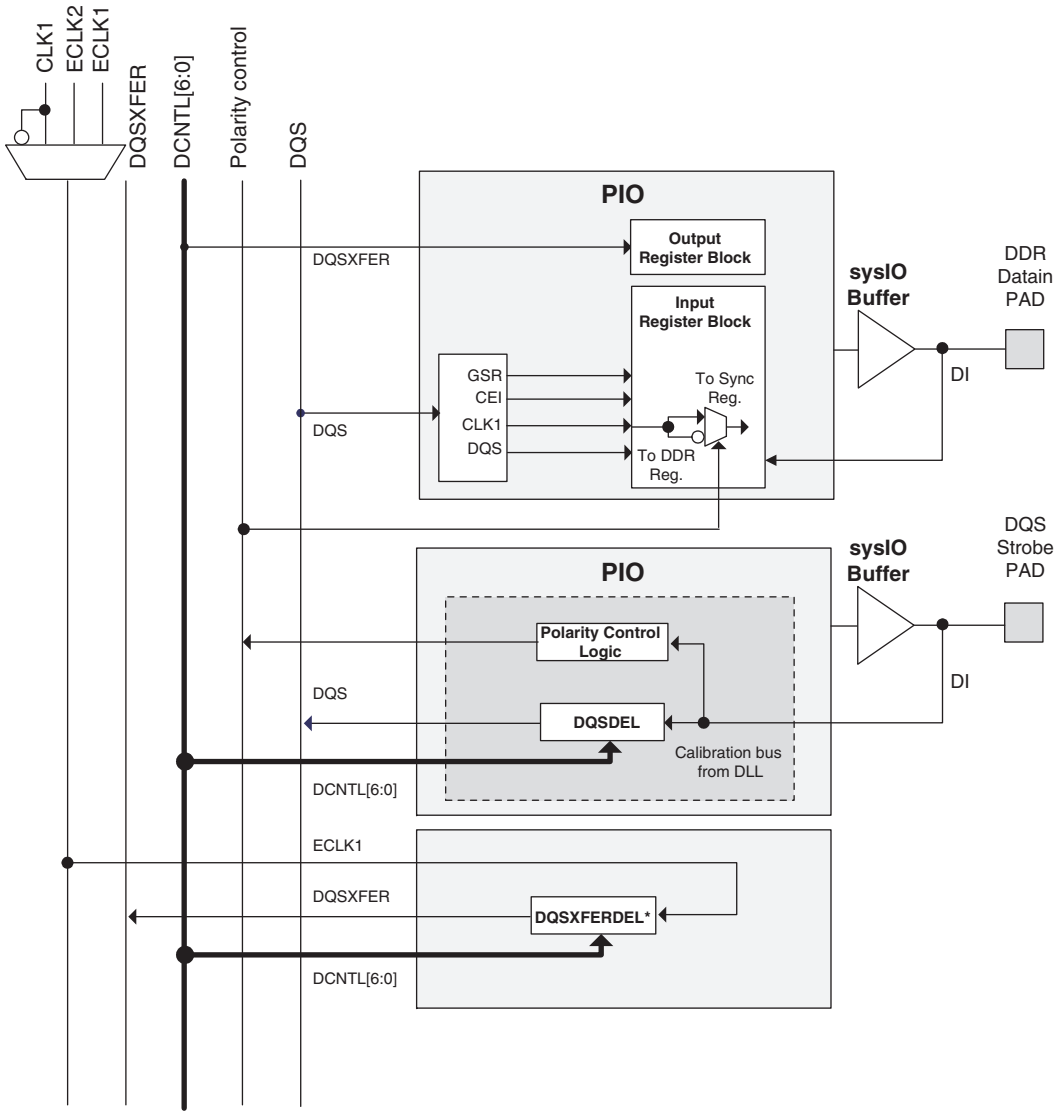


Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

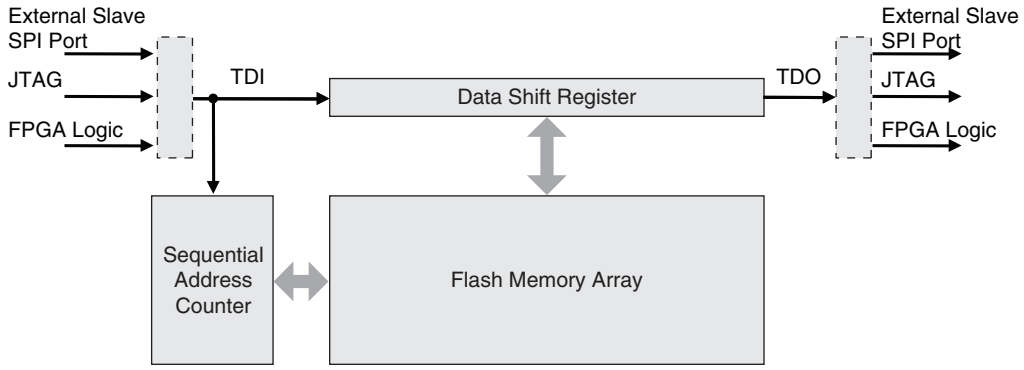
1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LA-LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LA-LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
   LA-LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1143, LatticeXP2 TransFR I/O.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LA-LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LA-LatticeXP2 device can revert back

Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25 °C, Max. Supply)[6]	Units
I_{CC}	Core Power Supply Current	LA-XP2-5	17	mA
		LA-XP2-8	21	mA
		LA-XP2-17	28	mA
I_{CCAUX}	Auxiliary Power Supply Current[7]	LA-XP2-5	64	mA
		LA-XP2-8	66	mA
		LA-XP2-17	83	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I_{CCJ}	V_{CCJ} Power Supply Current[8]		14	mA

1. For further information on supply current, see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are con•gured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz (excludes dynamic power from FPGA operation).
4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
5. Bypass or decoupling capacitor across the supply.
6. T_J = 25 °C, power supplies at nominal voltage.
7. In fpBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
8. When programming via JTAG.

RSDS

The LA-LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

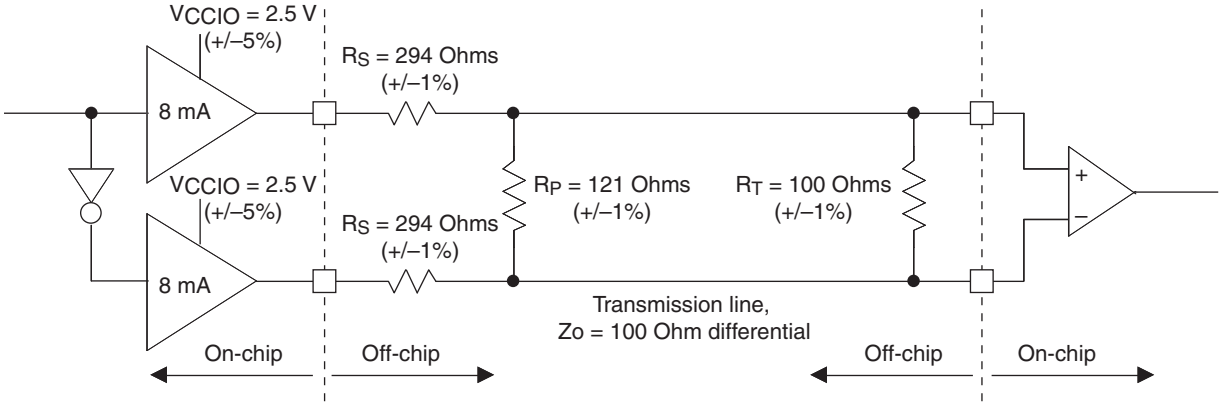


Table 3-4. RSDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	294	Ω
R_P	Driver Parallel Resistor (+/–1%)	121	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage (After R_P)	1.35	V
V_{OL}	Output Low Voltage (After R_P)	1.15	V
V_{OD}	Output Differential Voltage (After R_P)	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance[1]

Over Recommended Operating Conditions

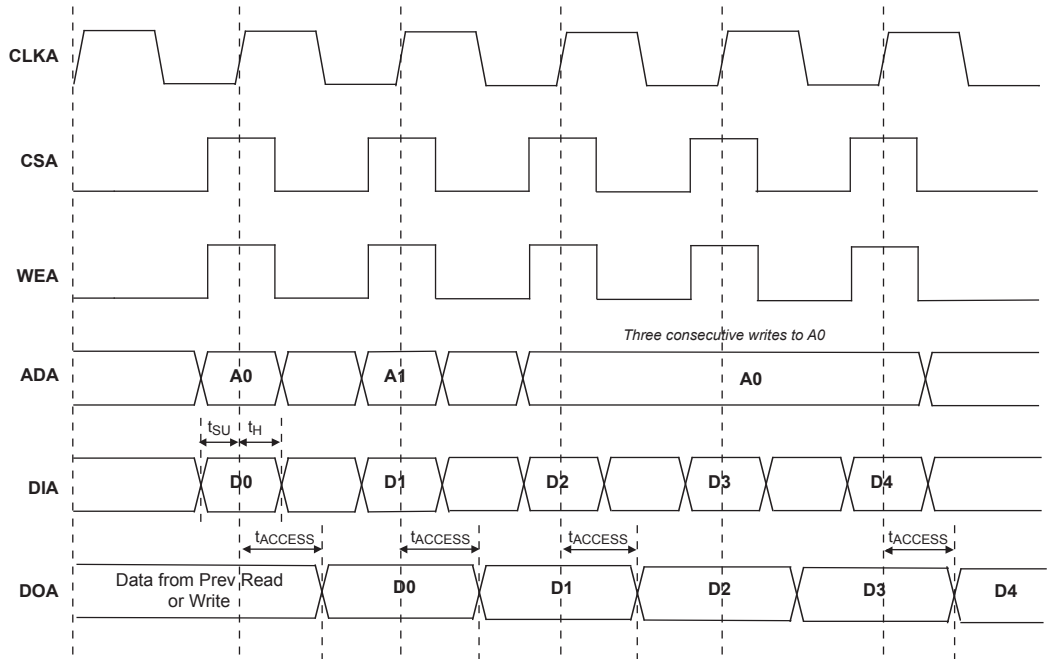
Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	5.7	ns
32-bit Decoder	6.9	ns
64-bit Decoder	7.7	ns
4:1 MUX	4.8	ns
8:1 MUX	5.1	ns
16:1 MUX	5.6	ns
32:1 MUX	5.8	ns

Register-to-Register Performance

Function	–5 Timing	Units
Basic Functions		
16-bit Decoder	354	MHz
32-bit Decoder	318	MHz
64-bit Decoder	280	MHz
4:1 MUX	493	MHz
8:1 MUX	458	MHz
16:1 MUX	424	MHz
32:1 MUX	364	MHz
8-bit Adder	326	MHz
16-bit Adder	306	MHz
64-bit Adder	178	MHz
16-bit Counter	312	MHz
32-bit Counter	257	MHz
64-bit Counter	191	MHz
64-bit Accumulator	161	MHz
Embedded Memory Functions		
512 x 36 Single Port RAM, EBR Output Registers	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	252	MHz
1024 x 18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	173	MHz
Distributed Memory Functions		
16 x 4 Pseudo-Dual Port RAM (One PFU)	508	MHz
32 x 2 Pseudo-Dual Port RAM	313	MHz
64 x 1 Pseudo-Dual Port RAM	235	MHz
DSP Functions		
18 x 18 Multiplier (All Registers)	276	MHz
9 x 9 Multiplier (All Registers)	276	MHz
36 x 36 Multiply (All Registers)	244	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	176	MHz
18 x 18 Multiply-Add/Sub-Sum (All Registers)	235	MHz

Figure 3-8. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LA-LatticeXP2 Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
Input Adjusters			
LVDS25	LVDS	0.05	ns
BLVDS25	BLVDS	0.05	ns
MLVDS	LVDS	0.05	ns
RSDS	RSDS	0.05	ns
LVPECL33	LVPECL	0.05	ns
HSTL18_I	HSTL_18 class I	0.07	ns
HSTL18_II	HSTL_18 class II	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	0.02	ns
HSTL15_I	HSTL_15 class I	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	ns
SSTL33_I	SSTL_3 class I	0.12	ns
SSTL33_II	SSTL_3 class II	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	0.04	ns
SSTL25_I	SSTL_2 class I	0.10	ns
SSTL25_II	SSTL_2 class II	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	0.03	ns
SSTL18_I	SSTL_18 class I	0.07	ns
SSTL18_II	SSTL_18 class II	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	0.02	ns
LVTTL33	LVTTL	0.19	ns
LVCMOS33	LVCMOS 3.3	0.19	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.17	ns
LVCMOS12	LVCMOS 1.2	-0.04	ns
PCI33	3.3V PCI	0.19	ns
Output Adjusters			
LVDS25E	LVDS 2.5 E[4]	0.32	ns
LVDS25	LVDS 2.5	0.32	ns
BLVDS25	BLVDS 2.5	0.29	ns
MLVDS	MLVDS 2.5[4]	0.29	ns
RSDS	RSDS 2.5[4]	0.32	ns
LVPECL33	LVPECL 3.3[4]	0.19	ns
HSTL18_I	HSTL_18 class I 8mA drive	0.45	ns
HSTL18_II	HSTL_18 class II	0.31	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	0.45	ns
HSTL18D_II	Differential HSTL 18 class II	0.31	ns

LA-LatticeXP2 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
sysCONFIG POR, Initialization and Wake Up				
t_{ICFG}	Minimum Vcc to INITN High	—	50	ms
t_{VMC}	Time from tICFG to valid Master CCLK	—	2	µs
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	12	ns
t_{PRGM}	PROGRAMN Low Time to Start Con•guration	50	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay	—	1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	50	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	50	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	0	—	cycles
sysCONFIG SPI Port (Master)				
t_{CFGX}	INITN High to CCLK Low	—	1	µs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	µs
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns
f_{MAXSPI}	Max CCLK Frequency	—	20	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	10	—	ns
sysCONFIG SPI Port (Slave)				
$f_{MAXSPIS}$	Slave CCLK Frequency	—	25	MHz
t_{RF}	Rise and Fall Time	50	—	mV/ns
t_{STCO}	Falling Edge of CCLK to SOSPI Active	—	20	ns
t_{STOZ}	Falling Edge of CCLK to SOSPI Disable	—	20	ns
t_{STSU}	Data Setup Time (SISPI)	8	—	ns
t_{STH}	Data Hold Time (SISPI)	10	—	ns
t_{STCKH}	CCLK Clock Pulse Width, High	0.02	200	µs
t_{STCKL}	CCLK Clock Pulse Width, Low	0.02	200	µs
t_{STVO}	Falling Edge of CCLK to Valid SOSPI Output	—	20	ns
t_{SCS}	CSSPISN High Time	25	—	ns
t_{SCSS}	CSSPISN Setup Time	25	—	ns
t_{SCSH}	CSSPISN Hold Time	25	—	ns

On-Chip Oscillator and Configuration Master Clock Characteristics

Over Recommended Operating Conditions

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value –30%	Selected value +30%	MHz
Duty Cycle	40	60	%

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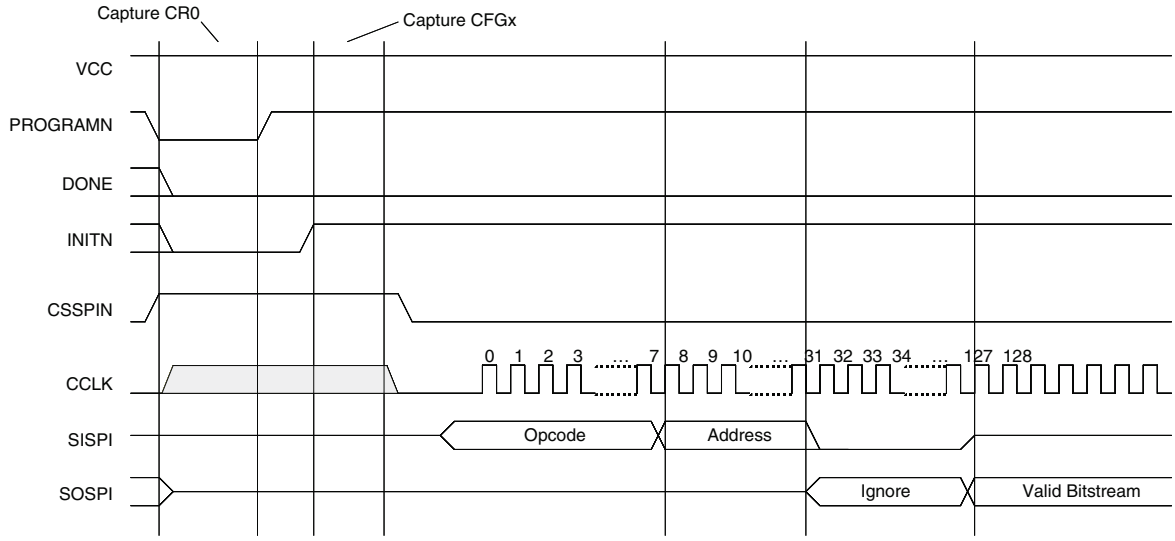
Figure 3-9. Master SPI Configuration Waveforms



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Top and Bottom Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.