Lattice Semiconductor Corporation - LAXP2-8E-5FTN256E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

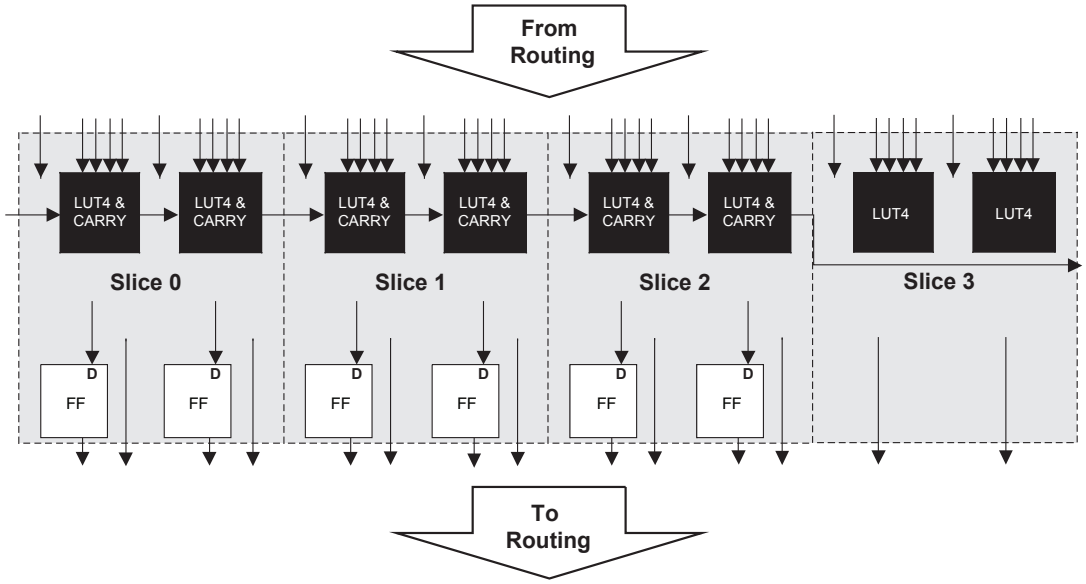
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-8e-5ftn256e

Figure 2-2. PFU Diagram



Slice

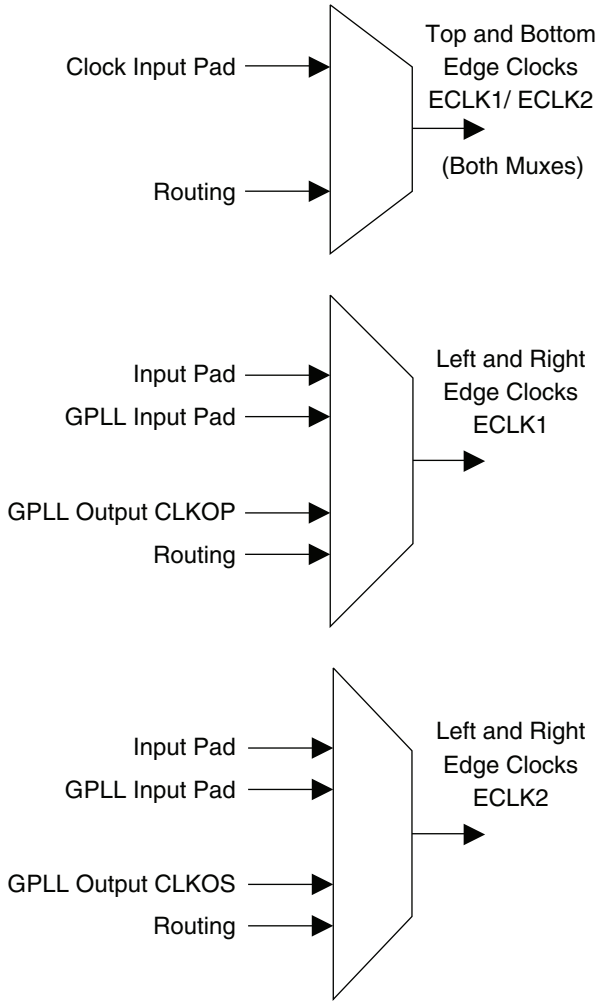
Slice 0 through Slice 2 contain two 4-input combinatorial Look-Up Tables (LUT4), which feed two registers. Slice 3 contains two LUT4s and no registers. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in PFF blocks. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured as positive/negative edge triggered or level sensitive clocks.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slice 0 through Slice 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Figure 2-15. Edge Clock Mux Connections



sysMEM Memory

LA-LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Con• gurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

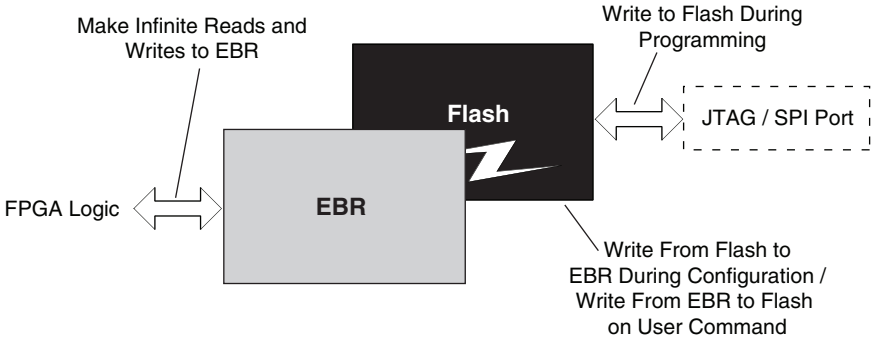
Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

FlashBAK EBR Content Storage

All the EBR memory in the LA-LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tool. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.

Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on speci•c design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Table 2-11. PIO Signal List

Name	Type	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK[2]	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0[1], QPOS1[1]	Input to the core	Gearbox pipelined inputs to the core
QNEG0[1], QNEG1[1]	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.
2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

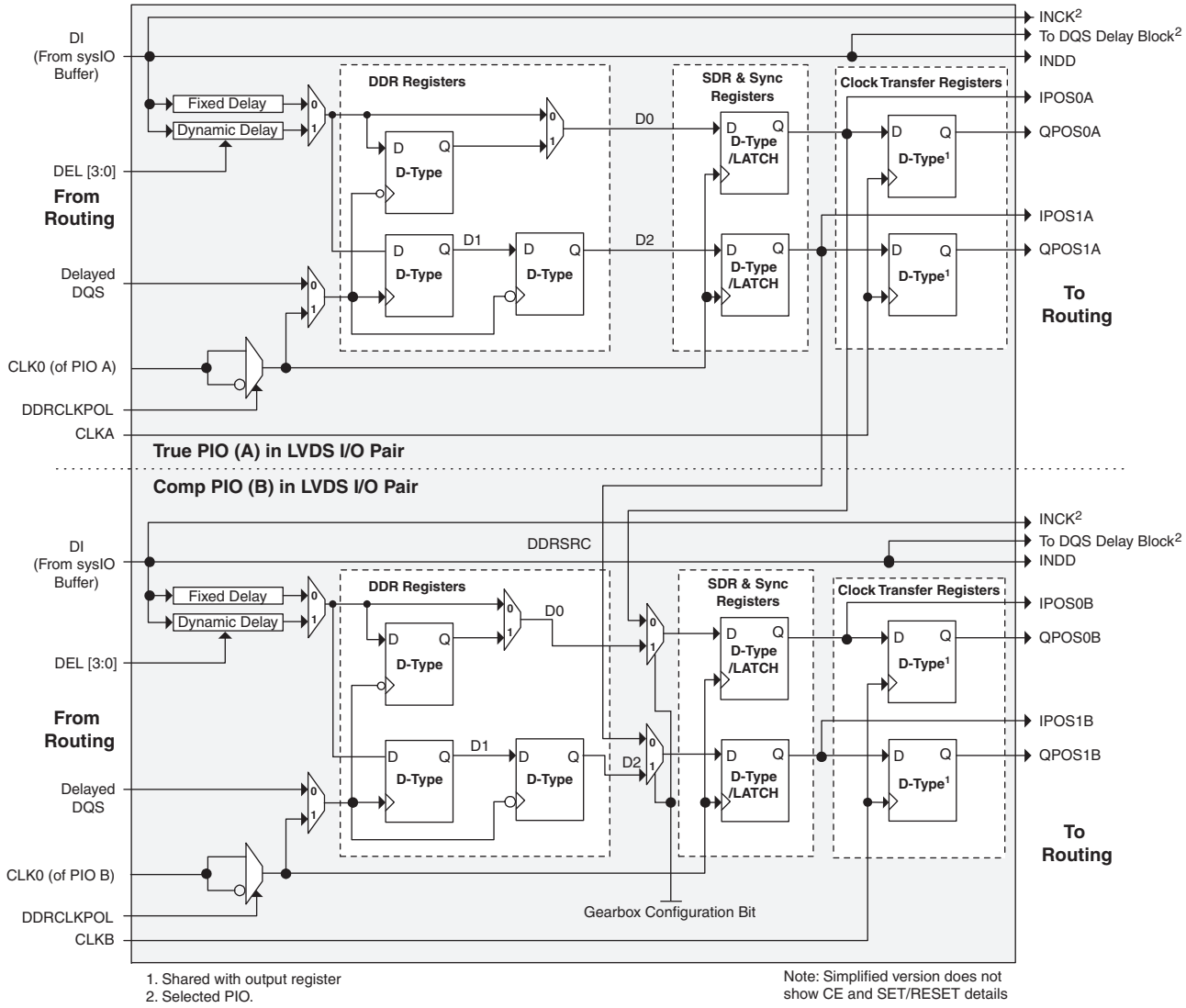
Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Block



1. Shared with output register
2. Selected PIO.

Note: Simplified version does not show CE and SET/RESET details

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support, see TN1138, LatticeXP2 High Speed I/O Interface.

DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution

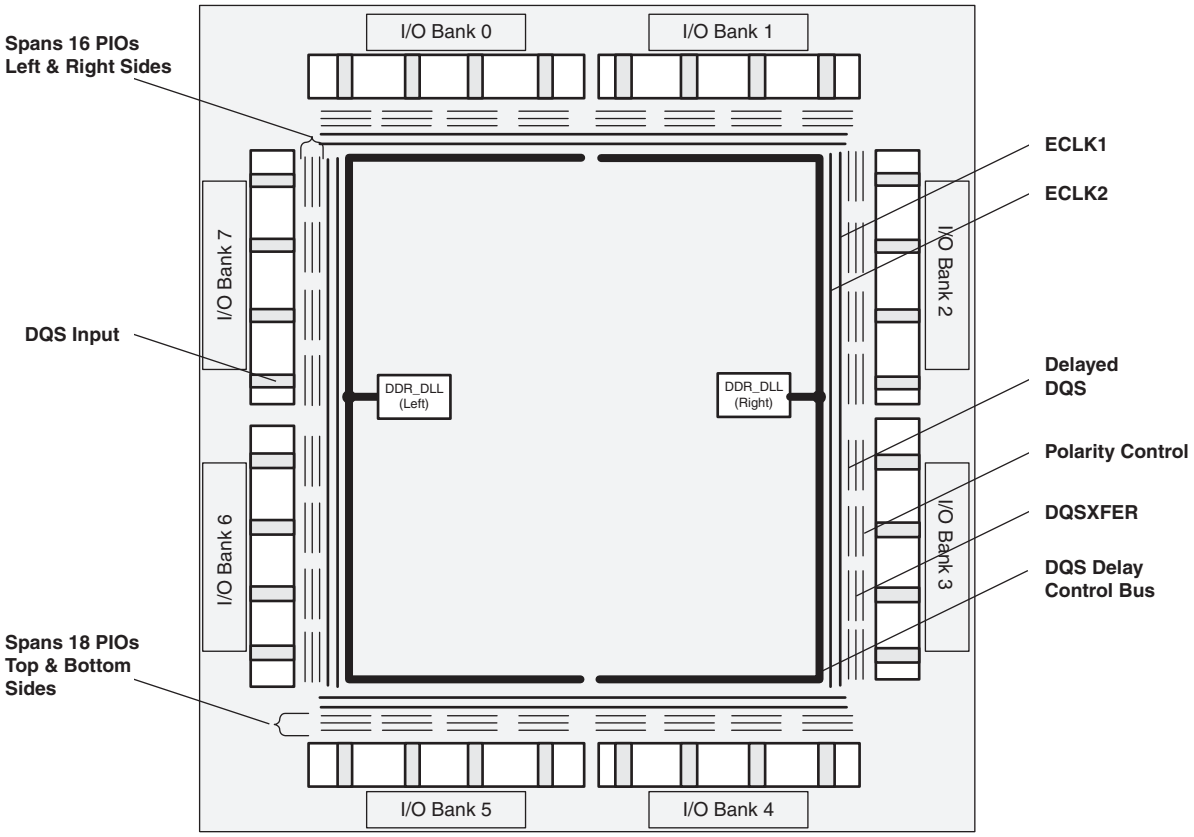
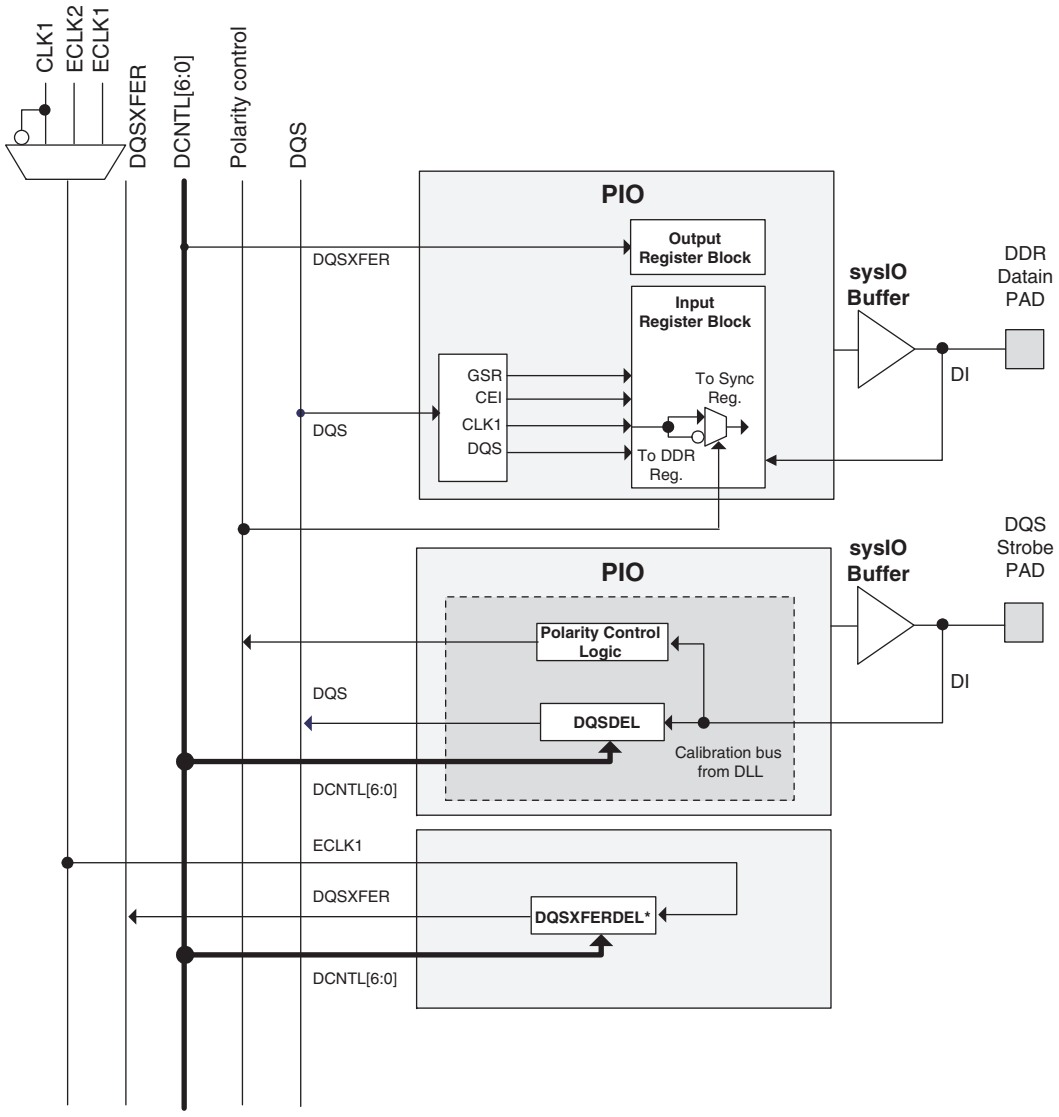


Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

Table 2-12. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12	—	—
PCI33	—	—
HSTL18 Class I, II	0.9	—
HSTL15 Class I	0.75	—
SSTL33 Class I, II	1.5	—
SSTL25 Class I, II	1.25	—
SSTL18 Class I, II	0.9	—
Differential Interfaces		
Differential SSTL18 Class I, II	—	—
Differential SSTL25 Class I, II	—	—
Differential SSTL33 Class I, II	—	—
Differential HSTL15 Class I	—	—
Differential HSTL18 Class I, II	—	—
LVDS, MLVDS, LVPECL, BLVDS, RSDS	—	—

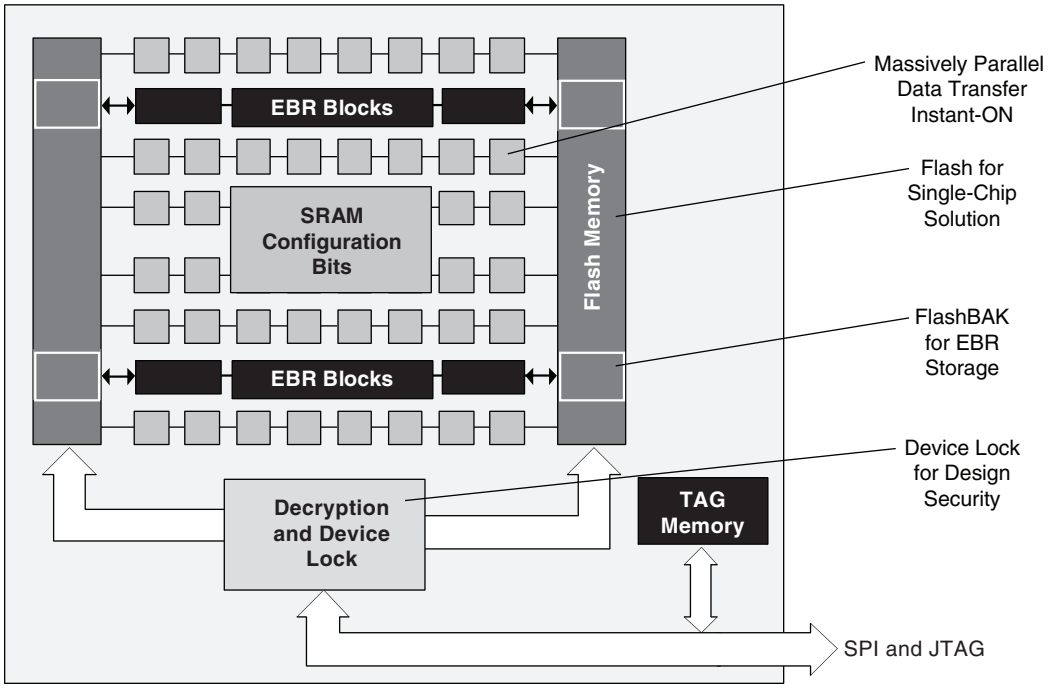
1. When not specified, V_{CCIO} can be set anywhere in the valid operating range (page 3-1).

be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for veri•cation. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LA-LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.

Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LA-LatticeXP2 Devices



At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:

to the original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, LatticeXP2 Dual Boot Feature.

4. For more information on device configuration, see TN1141, LatticeXP2 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LA-LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LA-LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

On-Chip Oscillator

Every LA-LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, see TN1141, LatticeXP2 sysCONFIG Usage Guide.

Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

CCLK/Oscillator (MHz)
2.5[1]
3.1[2]
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80[3]
163[3]

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

Density Shifting

The LA-LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LA-LatticeXP2 Family Data Sheet DC and Switching Characteristics

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Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.32 V

Supply Voltage V_{CCAUX} . . . . . –0.5 V to 3.75 V

Supply Voltage V_{CCJ} . . . . . –0.5 V to 3.75 V

Supply Voltage V_{CCPLL}[4] . . . . . –0.5 V to 3.75 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.75 V

Input or I/O Tristate Voltage Applied[5] . . . –0.5 V to 3.75 V

Storage Temperature (Ambient) . . . . . –65 °C to 150 °C

Junction Temperature Under Bias (Tj) . . . . . +125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
5. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[4]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}[1]	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3, 4]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JAUTO}	Junction Temperature, Automotive Operation	–40	125	°C
$t_{JFLASHAUTO}$	Junction Temperature, Flash Programming, Automotive	–40	125	°C

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX}.

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units
$N_{PROGCYC}$	Flash Programming Cycles per $t_{RETENTION}$	10,000	Cycles
	Flash Functional Programming Cycles	100,000	
$t_{RETENTION}$	Data Retention	20	Years

Initialization Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25 °C, Max. Supply)[6]	Units
I_{CC}	Core Power Supply Current	LA-XP2-5	20	mA
		LA-XP2-8	21	mA
		LA-XP2-17	44	mA
I_{CCAUX}	Auxiliary Power Supply Current[7]	LA-XP2-5	67	mA
		LA-XP2-8	74	mA
		LA-XP2-17	112	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
I_{CCJ}	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are con•gured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Does not include additional current from bypass or decoupling capacitor across the supply.
5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
6. T_J = 25 °C, power supplies at nominal voltage.
7. In fpBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and $I_{CCPLL.}$ For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS33	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVTTL33	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	–16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS15	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	–8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS12	–0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	–6, –2
					0.2	V_{CCIO} - 0.2	0.1	–0.1
PCI33	–0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	–0.5
SSTL33_I	–0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	–8
SSTL33_II	–0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	–16
SSTL25_I	–0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	–7.6
							12	–12
SSTL25_II	–0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	–15.2
							20	–20
SSTL18_I	–0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	–6.7
SSTL18_II	–0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	–8
							11	–11
HSTL15_I	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
HSTL18_I	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	–8
							12	–12
HSTL18_II	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	–16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8 mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

LA-LatticeXP2 External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	–5		Units
			Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[1]					
t_{CO}	Clock to Output - PIO Output Register	LA-XP2-5	—	4.77	ns
		LA-XP2-8	—	4.77	ns
		LA-XP2-17	—	4.78	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LA-XP2-5	-0.06	—	ns
		LA-XP2-8	-0.06	—	ns
		LA-XP2-17	-0.06	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.98	—	ns
		LA-XP2-8	1.99	—	ns
		LA-XP2-17	1.99	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	1.87	—	ns
		LA-XP2-8	1.87	—	ns
		LA-XP2-17	1.86	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.06	—	ns
		LA-XP2-8	0.06	—	ns
		LA-XP2-17	0.07	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LA-XP2	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)[1]					
t_{COE}	Clock to Output - PIO Output Register	LA-XP2-5	—	4.00	ns
		LA-XP2-8	—	4.00	ns
		LA-XP2-17	—	4.00	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.62	—	ns
		LA-XP2-8	1.62	—	ns
		LA-XP2-17	1.62	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	1.62	—	ns
		LA-XP2-8	1.62	—	ns
		LA-XP2-17	1.62	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	LA-XP2	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]					
t_{COPLL}	Clock to Output - PIO Output Register	LA-XP2-5	—	3.80	ns
		LA-XP2-8	—	3.80	ns
		LA-XP2-17	—	3.80	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LA-XP2-5	1.25	—	ns
		LA-XP2-8	1.27	—	ns
		LA-XP2-17	1.23	—	ns

LA-LatticeXP2 Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
Input Adjusters			
LVDS25	LVDS	0.05	ns
BLVDS25	BLVDS	0.05	ns
MLVDS	LVDS	0.05	ns
RSDS	RSDS	0.05	ns
LVPECL33	LVPECL	0.05	ns
HSTL18_I	HSTL_18 class I	0.07	ns
HSTL18_II	HSTL_18 class II	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	0.02	ns
HSTL15_I	HSTL_15 class I	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	ns
SSTL33_I	SSTL_3 class I	0.12	ns
SSTL33_II	SSTL_3 class II	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	0.04	ns
SSTL25_I	SSTL_2 class I	0.10	ns
SSTL25_II	SSTL_2 class II	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	0.03	ns
SSTL18_I	SSTL_18 class I	0.07	ns
SSTL18_II	SSTL_18 class II	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	0.02	ns
LVTTL33	LVTTL	0.19	ns
LVCMOS33	LVCMOS 3.3	0.19	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.17	ns
LVCMOS12	LVCMOS 1.2	-0.04	ns
PCI33	3.3V PCI	0.19	ns
Output Adjusters			
LVDS25E	LVDS 2.5 E[4]	0.32	ns
LVDS25	LVDS 2.5	0.32	ns
BLVDS25	BLVDS 2.5	0.29	ns
MLVDS	MLVDS 2.5[4]	0.29	ns
RSDS	RSDS 2.5[4]	0.32	ns
LVPECL33	LVPECL 3.3[4]	0.19	ns
HSTL18_I	HSTL_18 class I 8mA drive	0.45	ns
HSTL18_II	HSTL_18 class II	0.31	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	0.45	ns
HSTL18D_II	Differential HSTL 18 class II	0.31	ns

LA-LatticeXP2 Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	1.60	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.40	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.63	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.41	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.84	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.52	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.32	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.55	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	1.79	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	0.01	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	1.73	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.02	ns
PCI33	3.3V PCI	0.27	ns

1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.

Timing v. A 0.12

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		10	—	435	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f_{OUT2}	K-Divider Output Frequency	CLKOK	0.078	—	217.5	MHz
		CLKOK2	3.3	—	145	MHz
f_{VCO}	PLL VCO Frequency		435	—	870	MHz
f_{PFD}	Phase Detector Input Frequency		10	—	435	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected [3]	45	50	55	%
t_{CPA}	Coarse Phase Adjust		-5	0	5	%
t_{PH} [4]	Output Phase Accuracy		-5	0	5	%
t_{OPJIT} [1]	Output Clock Period Jitter	f_{OUT} > 400 MHz	—	—	±50	ps
		100 MHz < f_{OUT} < 400 MHz	—	—	±125	ps
		f_{OUT} < 100 MHz	—	—	0.025	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±240	ps
t_{OPW}	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK} [2]	PLL Lock-in Time	25 to 435MHz	—	—	50	µs
		10 to 25MHz	—	—	100	µs
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_R / t_F	Input Clock Rise/Fall Time	10% to 90%	—	—	1	ns
t_{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t_{RSTW}	Reset Signal Pulse Width (RST)		500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

Timing v. A 0.12

Lead-Free Packaging

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-5E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	5
LAXP2-5E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	5
LAXP2-5E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	5
LAXP2-5E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-8E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	8
LAXP2-8E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	8
LAXP2-8E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	8
LAXP2-8E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-17E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	17
LAXP2-17E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	17