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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	86
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-8e-5mn132e

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Introduction

LA-LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LA-LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LA-LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond[®] design software allows large and complex designs to be efficiently implemented using the LA-LatticeXP2 family of FPGA devices. Synthesis library support for LA-LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LA-LatticeXP2 device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE[™] modules for the LA-LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.



Figure 2-3. Slice Diagram



DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data

WAD [A:D] is a 4bit address from Slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	MO	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Fourinput logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LA-LatticeXP2 devices, see TN1137, LatticeXP2 Memory Usage Guide.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4				
Number of slices	3	3				

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.



Figure 2-15. Edge Clock Mux Connections



sysMEM Memory

LA-LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.



mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be con•gured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-6 shows the capabilities of the block.

Table 2-6. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	_
MULTADDSUB	4	2	_
MULTADDSUBSUM	2	1	_

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting 'dynamic operation' the following operations are possible:

- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.



Figure 2-20. MULT sysDSP Element





MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/ subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output



Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.



CLKB

ECLK1 ECLK2 CLK1 (CLKB) DQSXFER Clock Transfer Registers

* Shared with input register

то

DO

то

DO

Programmable Control

Output Logic

Note: Simplified version does not show CE and SET/RESET details

To sysIO Buffer

To sysIO Buffer

shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.



Figure 2-27. Output and Tristate Block



Figure 2-28. DQS Input Routing (Left and Right)

	PIO A		PADA "T"
	PIO B	+	PADB "C"
	PIO A		PADA "T"
	PIO B	·	PADB "C"
	PIO A	┝	PADA "T"
	PIO B	·	PADB "C"
	PIO A		PADA "T"
	PIO B	+	PADB "C"
↓ DQS	PIO A	sysIO Buffer Delay ◀	PADA "T"
	PIO B		PADB "C"
	PIO A		PADA "T" LVDS Pair
		•	
—	PIO B	·	PADB "C"
	PIO B PIO A	· · · · · · · · · · · · · · · · · · · ·	PADB "C"
	→ PIO B → PIO A → PIO B		PADB "C" PADA "T" LVDS Pair PADB "C"
	→ PIO B → PIO A → PIO B → PIO A	+ + +	PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T"

Figure 2-29. DQS Input Routing (Top and Bottom)

	PIO A		PADA "T"
	PIO B	·	PADB "C"
	PIO A		PADA "T"
	PIO B	· · · · · · · · · · · · · · · · · · ·	PADB "C"
	PIO A		PADA "T"
	PIO B	·	PADB "C"
	PIO A		PADA "T"
	PIO B	·	PADB "C"
	PIO A	sysIO Buffer	
DQS			PADA "T"
4		Delay	LVDS Pair
+	PIO B		LVDS Pair PADB "C"
<	PIO B PIO A		LVDS Pair PADB "C" PADA "T"
	→ PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
	→ PIO B → PIO A → PIO B → PIO A		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADB "T"
	→ PIO B → PIO A → PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
	→ PIO B → PIO A → PIO A → PIO A → PIO B → PIO A		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T"
			LVDS Pair PADB "C" IVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
			LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair



be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for veri• cation. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LA-LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.



Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LA-LatticeXP2 Devices

At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:



- 1. Unlocked
- 2. Key Locked Presenting the key through the programming interface allows the device to be unlocked.
- 3. Permanently Locked The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LA-LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LA-LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. Decryption Support

LA-LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1143, LatticeXP2 TransFR I/O.

3. Dual Boot Image Support

Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LA-LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LA-LatticeXP2 device can revert back



LA-LatticeXP2 Family Data Sheet DC and Switching Characteristics

February 2015

Data Sheet DS1024

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V _{CC} –0.5 V to 1.32 V
Supply Voltage V _{CCAUX}
Supply Voltage V_{CCJ}
Supply Voltage V_{CCPLL}^{4}
Output Supply Voltage V_{CCIO} –0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied $^5.$ –0.5 V to 3.75 V
Storage Temperature (Ambient) $\dots -65$ °C to 150 °C
Junction Temperature Under Bias (Tj)+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

- 4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
- 5. Overshoot and undershoot of -2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Core Supply Voltage	1.14	1.26	V
V _{CCAUX} ⁴	Auxiliary Supply Voltage	3.135	3.465	V
V _{CCPLL} ¹	PLL Supply Voltage	3.135	3.465	V
V _{CCIO} ^{2, 3, 4}	I/O Driver Supply Voltage	1.14	3.465	V
V _{CCJ} ²	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t _{JAUTO}	Junction Temperature, Automotive Operation	-40	125	°C
t _{JFLASHAUTO}	Junction Temperature, Flash Programming, Automotive	-40	125	°C

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.

If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC.} If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX}.

3. See recommended voltages by I/O standard in subsequent table.

4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX} .

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units
N	Flash Programming Cycles per t _{RETENTION}	10,000	Cyclos
PROGCYC	Flash Functional Programming Cycles	100,000	Cycles
t _{RETENTION}	Data Retention	20	Years

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LA-LatticeXP2 External Switching Characteristics (Continued)

			-	5	
Parameter	Description	Device	Min.	Max.	Units
		LA-XP2-5	1.32		ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	LA-XP2-8	1.32	—	ns
		LA-XP2-17	1.32		ns
		LA-XP2-5	2.16	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-8	2.18	—	ns
		LA-XP2-17	2.14	—	ns
		LA-XP2-5	0.00	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
DDR ² and DDR2 ³	I/O Pin Parameters				
t _{DVADQ}	Data Valid After DQS (DDR Read)	LA-XP2	_	0.29	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	LA-XP2	0.71	—	UI
t _{DQVBS}	Data Valid Before DQS	LA-XP2	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	LA-XP2	0.25	—	UI
f _{MAX_DDR}	DDR Clock Frequency	LA-XP2	95	133	MHz
f _{MAX_DDR2}	DDR Clock Frequency	LA-XP2	133	166	MHz
Primary Clock					
f _{MAX_PRI}	Frequency for Primary Clock Tree	LA-XP2		311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	LA-XP2	1	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	LA-XP2	_	160	ps
Edge Clock (ECL	K1 and ECLK2)				
f _{MAX_ECLK}	Frequency for Edge Clock	LA-XP2	_	311	MHz
tw_ECLK	Clock Pulse Width for Edge Clock	LA-XP2	1		ns
t _{SKEW_ECLK}	Edge Clock Skew Within an Edge of the Device	LA-XP2	_	130	ps

Over Recommended Operating Conditions

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.

2. DDR timing numbers based on SSTL25.

3. DDR2 timing numbers based on SSTL18.

Timing v. A 0.12







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



LA-LatticeXP2 Family Timing Adders^{1, 2, 3} (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	Units
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	1.60	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.40	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.63	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.41	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.84	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.52	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.32	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.55	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	1.79	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	0.01	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	1.73	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.02	ns
PCI33	3.3V PCI	0.27	ns

1. Timing Adders are characterized but not tested on every device.

2. LVCMOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. These timing adders are measured with the recommended resistor values.

Timing v. A 0.12



Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The speciec values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
	8	œ	0pF	LVCMOS 3.3 = 1.5 V	
LVTTL and other LVCMOS settings (L -> H, H -> L)				LVCMOS 2.5 = $V_{CCIO}/2$	
				LVCMOS 1.8 = $V_{CCIO}/2$	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = $V_{CCIO}/2$	
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> L)	1MΩ	8 S		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V _{OH} – 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Pin Information Summary (Continued)

	LA-XP2-5				LA-XP2-8				LA-XP2-17		
Pin Type		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA
	Bank0	1	1	1	1	1	1	1	1	1	1
	Bank1	0	0	1	1	0	0	1	1	1	1
	Bank2	1	1	1	1	1	1	1	1	1	1
DDR Banks Bonding Out	Bank3	0	0	1	1	0	0	1	1	1	1
per I/O Bank ¹	Bank4	0	0	1	1	0	0	1	1	1	1
	Bank5	1	1	1	1	1	1	1	1	1	1
	Bank6	0	0	1	1	0	0	1	1	1	1
	Bank7	1	1	1	1	1	1	1	1	1	1
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28
	Bank1	4	6	18	18	4	6	18	22	18	22
	Bank2	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26
	Bank5	14	18	20	24	14	18	20	24	20	24
	Bank6	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQS + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found on the LatticeXP2 product pages on the Lattice website at www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package-specific thermal values.

For Further Information

- TN1139 Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool included with Lattice Diamond design software or as a standalone download from www.latticesemi.com/software



Lead-Free Packaging

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-5E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	5
LAXP2-5E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	5
LAXP2-5E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	5
LAXP2-5E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-8E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	8
LAXP2-8E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	8
LAXP2-8E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	8
LAXP2-8E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-17E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	17
LAXP2-17E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	17



LA-LatticeXP2 Family Data Sheet Revision History

February 2015

Data Sheet DS1024

Revision History

Date	Version	Section	Change Summary
February 2015	1.5	Multiple	Corrected formatting; fixed page, table and figure numbers.
August 2014	1.4	All	Updated for Lattice corporate logo.
		Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
January 2012	01.3	Multiple	Updated for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary informa- tion.
May 2009	01.2	Introduction	Added support for 132 csBGA to Features list and Family Selection Guide table.
		Pinout Information	Added support for 132 csBGA to Pin Information Summary table.
		Ordering Information	Added support for 132 csBGA to Part Number Description diagram and Ordering Information tables.
August 2008	01.1	_	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching	Updated Typical Building Block Function Performance table.
		Characteristics	Updated External Switching Characteristics table.
			Updated Internal Switching Characteristics table.
			Updated Family Timing Adders table.
June 2008	01.0		Initial release.

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