Lattice Semiconductor Corporation - LAXP2-8E-5TN144E Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/laxp2-8e-5tn144e

Routing

There are many resources provided in the LA-LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LA-LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LA-LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.

Figure 2-4. General Purpose PLL (GPLL) Diagram

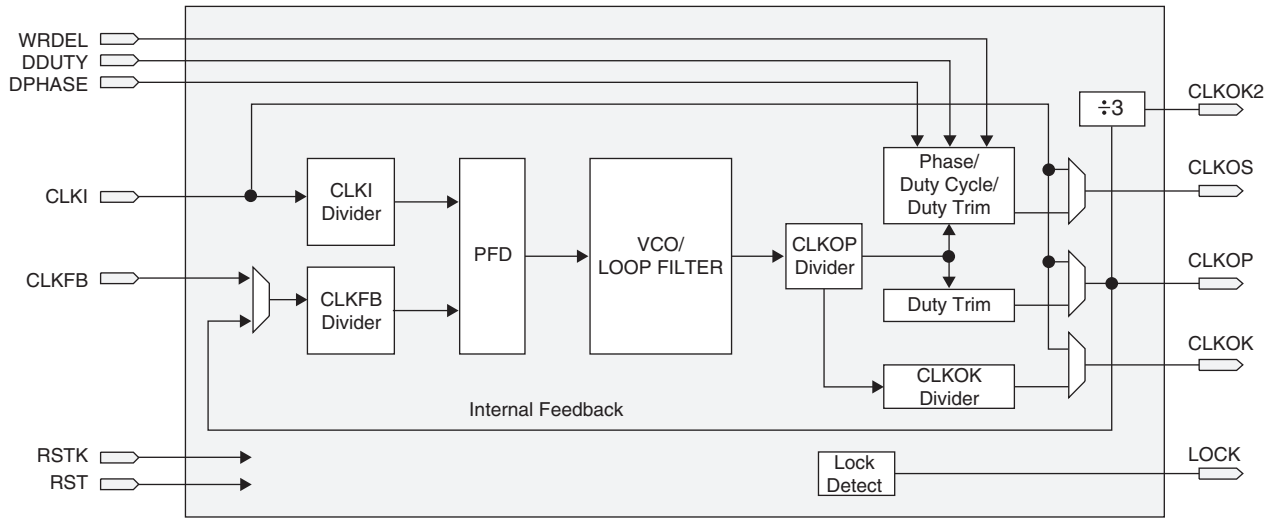


Table 2-4 provides a description of the signals in the GPLL blocks.

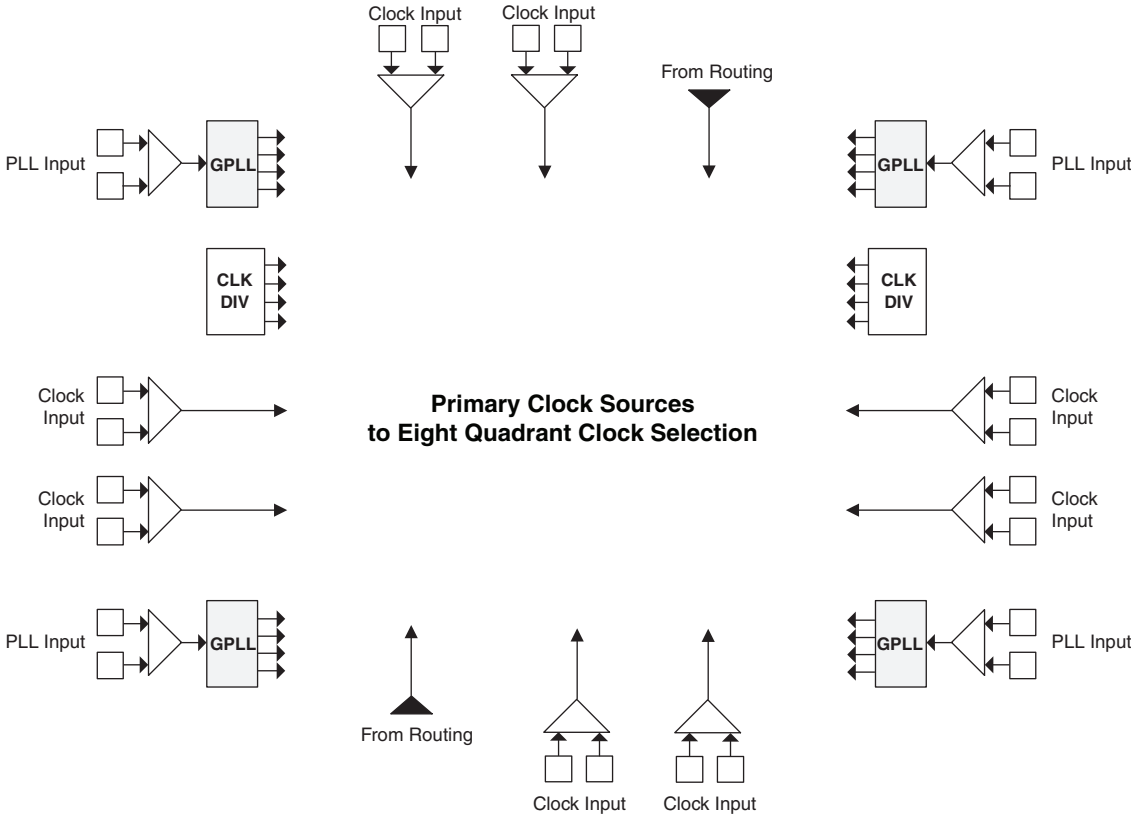
Table 2-4. GPLL Block Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

Clock Dividers

LA-LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.

Figure 2-6. Primary Clock Sources for LatticeXP2-17

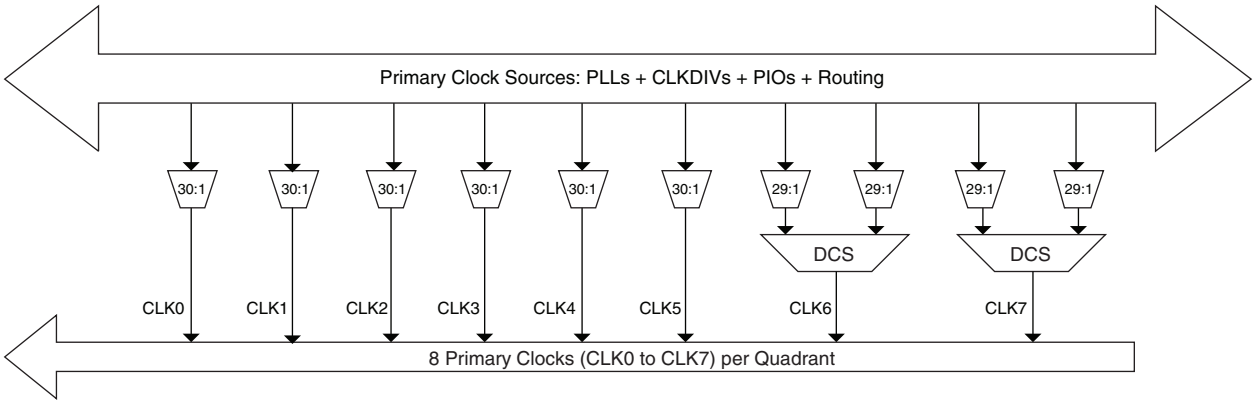


Note: This diagram shows sources for the LA-LatticeXP2-17 device. Smaller LA-LatticeXP2 devices have two GPLLs.

Primary Clock Routing

The clock routing structure in LA-LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-9 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-9. Per Quadrant Primary Clock Selection

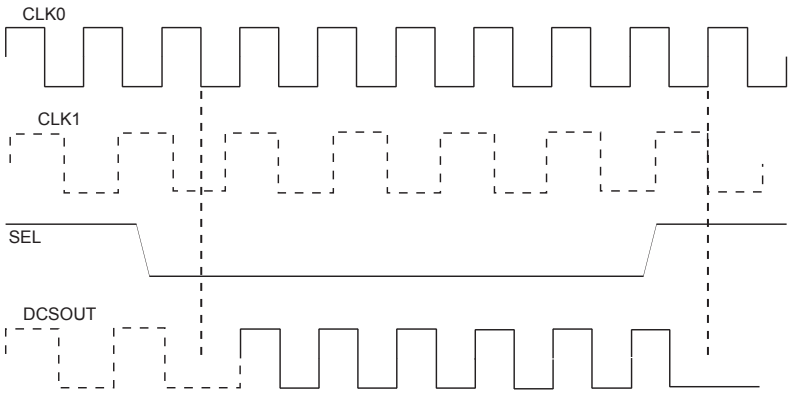


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-9).

Figure 2-10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.

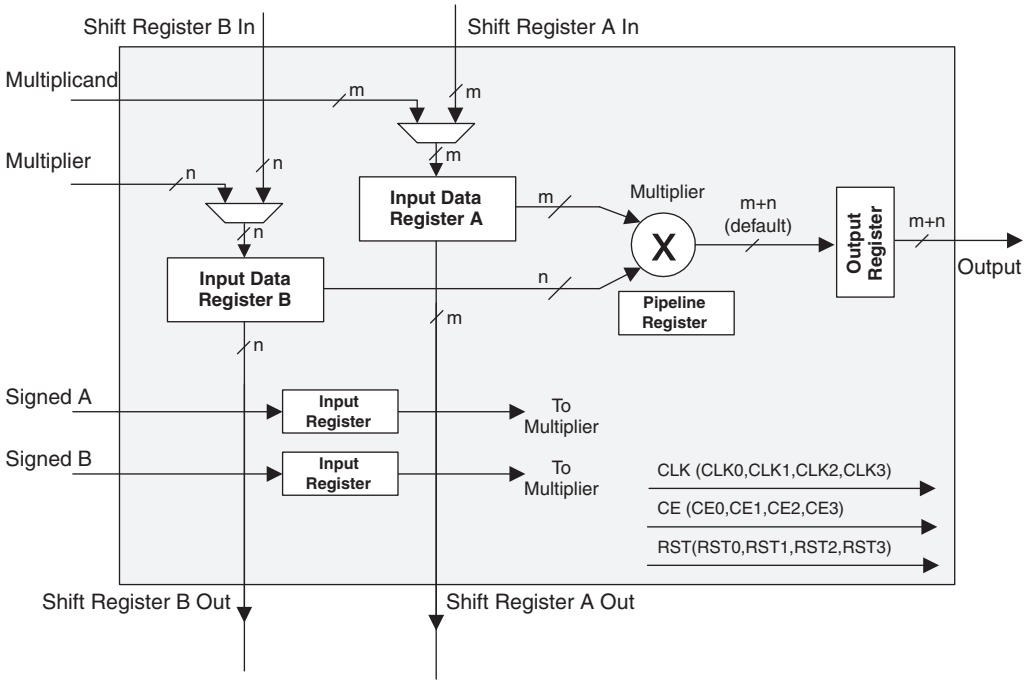
Figure 2-10. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LA-LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-11 shows this special vertical routing channel and the six secondary clock regions for the LA-

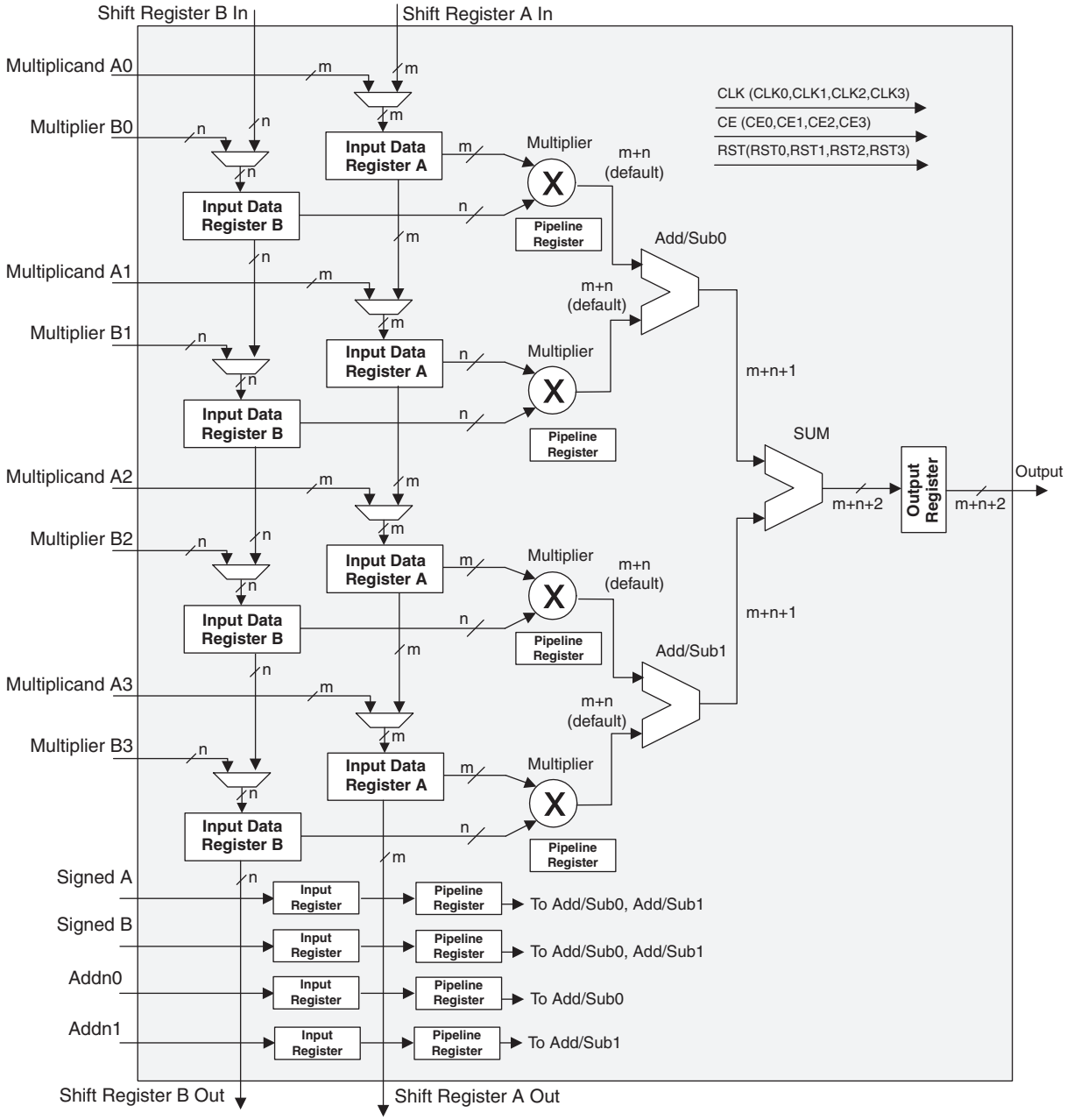
Figure 2-20. MULT sysDSP Element



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical[5]	Units
I_{CC}	Core Power Supply Current	LA-XP2-5	14	mA
		LA-XP2-8	18	mA
		LA-XP2-17	24	mA
I_{CCAUX}	Auxiliary Power Supply Current[6]	LA-XP2-5	15	mA
		LA-XP2-8	15	mA
		LA-XP2-17	15	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		1	mA
I_{CCIO}	Bank Power Supply Current (per bank)		2	mA
I_{CCJ}	V_{CCJ} Power Supply Current		1	mA

1. For further information on supply current, see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are con•gured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” con•guration data •le.
5. T_J = 25 °C, power supplies at nominal voltage.
6. In fpBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

LVPECL

The LA-LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

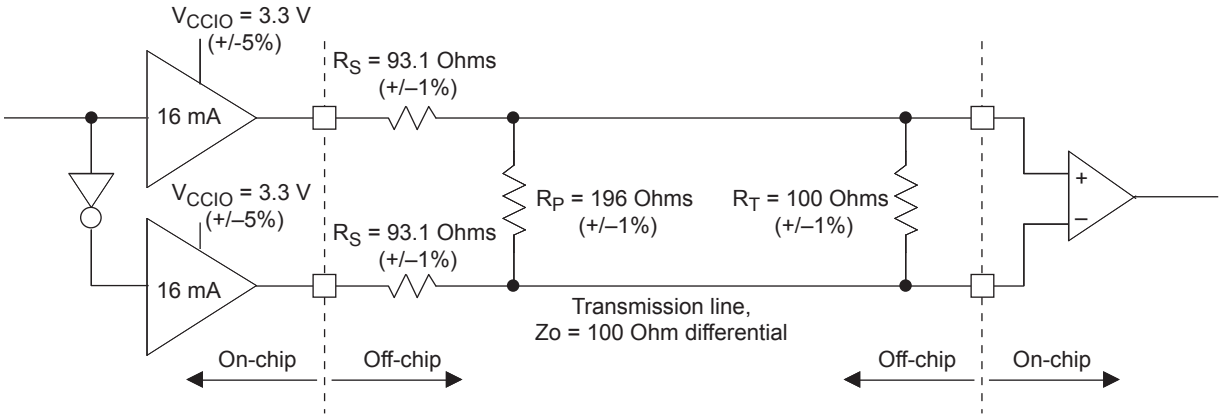


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/–1%)	93	Ω
R_P	Driver Parallel Resistor (+/–1%)	196	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage (After R_P)	2.05	V
V_{OL}	Output Low Voltage (After R_P)	1.25	V
V_{OD}	Output Differential Voltage (After R_P)	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

RSDS

The LA-LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

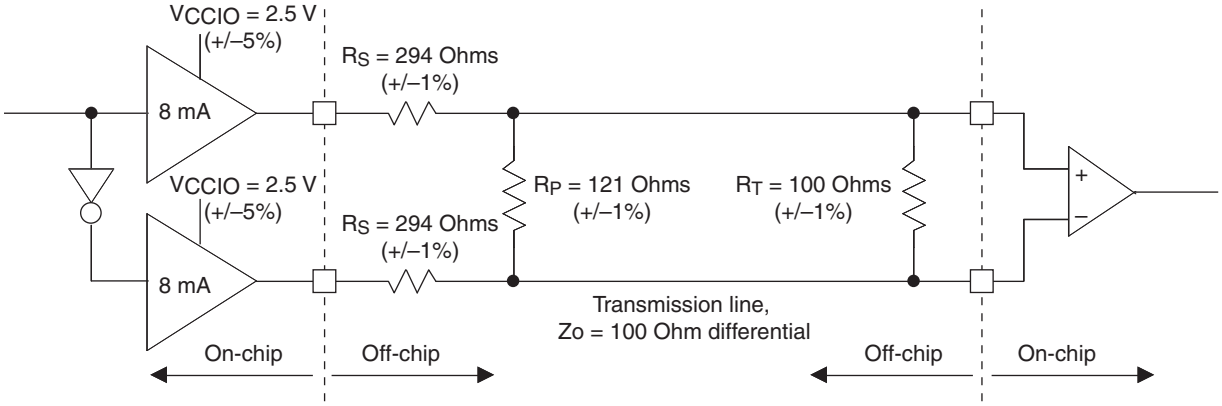


Table 3-4. RSDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	294	Ω
R_P	Driver Parallel Resistor (+/–1%)	121	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage (After R_P)	1.35	V
V_{OL}	Output Low Voltage (After R_P)	1.15	V
V_{OD}	Output Differential Voltage (After R_P)	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

LA-LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	–5		Units
			Min.	Max.	
t_{HPLL}	Clock to Data Hold - PIO Input Register	LA-XP2-5	1.32	—	ns
		LA-XP2-8	1.32	—	ns
		LA-XP2-17	1.32	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LA-XP2-5	2.16	—	ns
		LA-XP2-8	2.18	—	ns
		LA-XP2-17	2.14	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LA-XP2-5	0.00	—	ns
		LA-XP2-8	0.00	—	ns
		LA-XP2-17	0.00	—	ns
DDR[2] and DDR2[3] I/O Pin Parameters					
t_{DVADQ}	Data Valid After DQS (DDR Read)	LA-XP2	—	0.29	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	LA-XP2	0.71	—	UI
t_{DQVBS}	Data Valid Before DQS	LA-XP2	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	LA-XP2	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	LA-XP2	95	133	MHz
f_{MAX_DDR2}	DDR Clock Frequency	LA-XP2	133	166	MHz
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	LA-XP2	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	LA-XP2	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	LA-XP2	—	160	ps
Edge Clock (ECLK1 and ECLK2)					
f_{MAX_ECLK}	Frequency for Edge Clock	LA-XP2	—	311	MHz
t_{W_ECLK}	Clock Pulse Width for Edge Clock	LA-XP2	1	—	ns
t_{SKEW_ECLK}	Edge Clock Skew Within an Edge of the Device	LA-XP2	—	130	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25.
3. DDR2 timing numbers based on SSTL18.

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LA-LatticeXP2 Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	–5	Units
HSTL15_I	HSTL_15 class I 4mA drive	1.11	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	1.11	ns
SSTL33_I	SSTL_3 class I	0.37	ns
SSTL33_II	SSTL_3 class II	0.29	ns
SSTL33D_I	Differential SSTL_3 class I	0.37	ns
SSTL33D_II	Differential SSTL_3 class II	0.29	ns
SSTL25_I	SSTL_2 class I 8mA drive	0.32	ns
SSTL25_II	SSTL_2 class II 16mA drive	0.29	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	0.32	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	0.29	ns
SSTL18_I	SSTL_1.8 class I	0.45	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	0.44	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.45	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	0.44	ns
LVTTL33_4mA	LVTTL 4mA drive	0.28	ns
LVTTL33_8mA	LVTTL 8mA drive	0.11	ns
LVTTL33_12mA	LVTTL 12mA drive	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	0.10	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.28	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.11	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	0.10	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.09	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	0.05	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	0.01	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	0.09	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	1.94	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	1.65	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	1.45	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	1.69	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	1.47	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	1.90	ns

LA-LatticeXP2 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
sysCONFIG POR, Initialization and Wake Up				
t_{ICFG}	Minimum Vcc to INITN High	—	50	ms
t_{VMC}	Time from tICFG to valid Master CCLK	—	2	µs
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	12	ns
t_{PRGM}	PROGRAMN Low Time to Start Con•guration	50	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay	—	1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	50	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	50	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	0	—	cycles
sysCONFIG SPI Port (Master)				
t_{CFGX}	INITN High to CCLK Low	—	1	µs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	µs
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns
f_{MAXSPI}	Max CCLK Frequency	—	20	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	10	—	ns
sysCONFIG SPI Port (Slave)				
$f_{MAXSPIS}$	Slave CCLK Frequency	—	25	MHz
t_{RF}	Rise and Fall Time	50	—	mV/ns
t_{STCO}	Falling Edge of CCLK to SOSPI Active	—	20	ns
t_{STOZ}	Falling Edge of CCLK to SOSPI Disable	—	20	ns
t_{STSU}	Data Setup Time (SISPI)	8	—	ns
t_{STH}	Data Hold Time (SISPI)	10	—	ns
t_{STCKH}	CCLK Clock Pulse Width, High	0.02	200	µs
t_{STCKL}	CCLK Clock Pulse Width, Low	0.02	200	µs
t_{STVO}	Falling Edge of CCLK to Valid SOSPI Output	—	20	ns
t_{SCS}	CSSPISN High Time	25	—	ns
t_{SCSS}	CSSPISN Setup Time	25	—	ns
t_{SCSH}	CSSPISN Hold Time	25	—	ns

On-Chip Oscillator and Configuration Master Clock Characteristics

Over Recommended Operating Conditions

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value –30%	Selected value +30%	MHz
Duty Cycle	40	60	%

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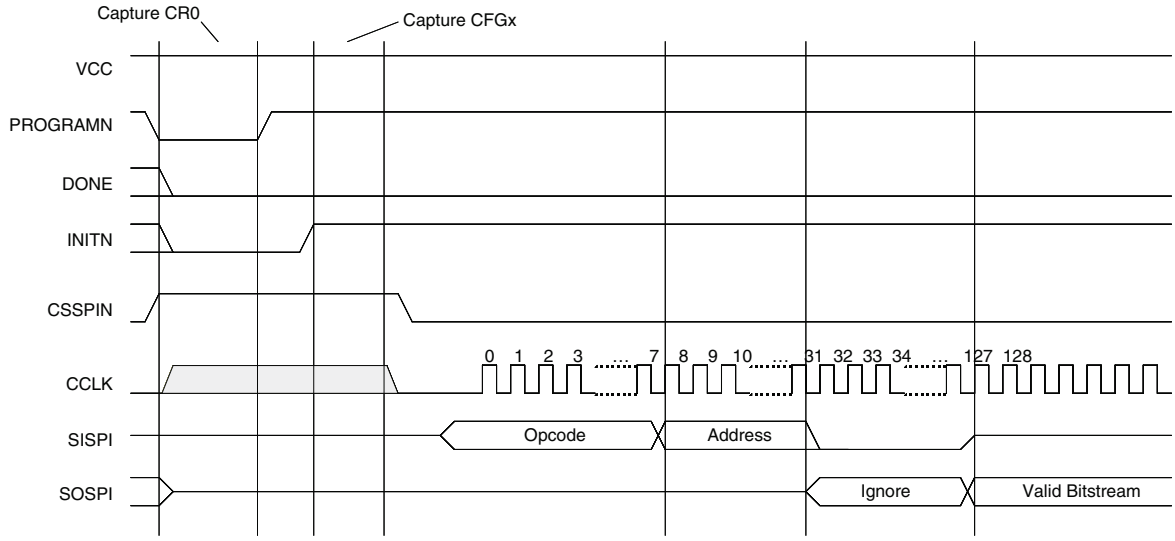
Figure 3-9. Master SPI Configuration Waveforms



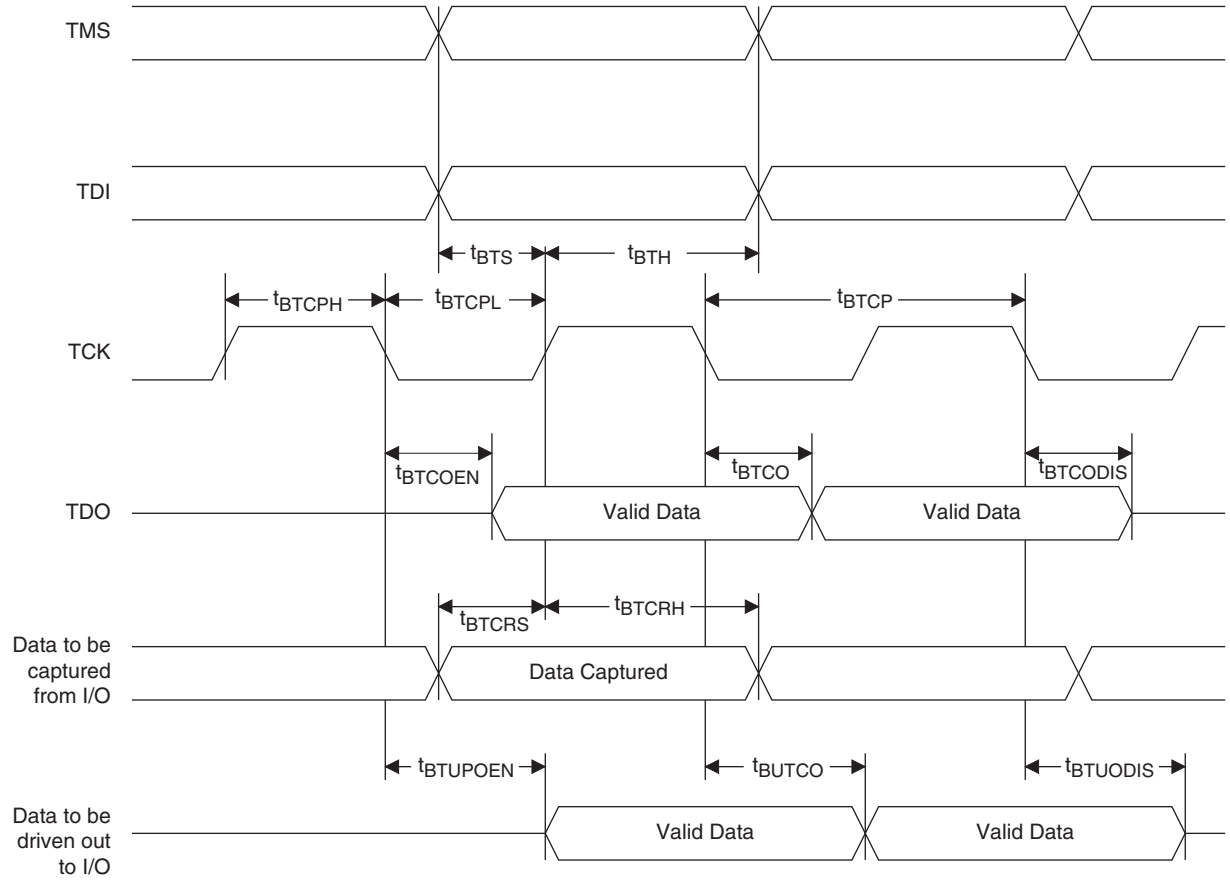
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v. A 0.12

Figure 3-10. JTAG Port Timing Waveforms



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Top and Bottom Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

Pin Information Summary

Pin Type		LA-XP2-5				LA-XP2-8				LA-XP2-17	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA
Single Ended User I/O		86	100	146	172	86	100	146	201	146	201
Differential Pair User I/O	Normal	35	39	57	66	35	39	57	77	57	77
	Highspeed	8	11	16	20	8	11	16	23	16	23
Configuration	TAP	5	5	5	5	5	5	5	5	5	5
	Muxed	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1
Non Configuration	Muxed	5	5	7	7	7	7	9	9	11	11
	Dedicated	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6
Vccaux		4	4	4	4	4	4	4	4	4	4
VCCPLL		2	2	2	-	2	2	2	-	4	-
VCCIO	Bank0	2	2	2	2	2	2	2	2	2	2
	Bank1	1	1	2	2	1	1	2	2	2	2
	Bank2	2	2	2	2	2	2	2	2	2	2
	Bank3	1	1	2	2	1	1	2	2	2	2
	Bank4	1	1	2	2	1	1	2	2	2	2
	Bank5	2	2	2	2	2	2	2	2	2	2
	Bank6	1	1	2	2	1	1	2	2	2	2
	Bank7	2	2	2	2	2	2	2	2	2	2
GND, GND0-GND7		15	15	20	20	15	15	22	20	22	20
NC		—	—	4	31	—	—	2	2	—	2
Single Ended/ Differential I/O per Bank	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14
	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13
	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12
	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12
True LVDS Pairs Bonding Out per Bank	Bank0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6
	Bank3	1	1	4	5	1	1	4	6	4	6
	Bank4	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6
	Bank7	3	4	4	5	3	4	4	5	4	5

Pin Information Summary (Continued)

Pin Type		LA-XP2-5				LA-XP2-8				LA-XP2-17	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA
DDR Banks Bonding Out per I/O Bank[1]	Bank0	1	1	1	1	1	1	1	1	1	1
	Bank1	0	0	1	1	0	0	1	1	1	1
	Bank2	1	1	1	1	1	1	1	1	1	1
	Bank3	0	0	1	1	0	0	1	1	1	1
	Bank4	0	0	1	1	0	0	1	1	1	1
	Bank5	1	1	1	1	1	1	1	1	1	1
	Bank6	0	0	1	1	0	0	1	1	1	1
	Bank7	1	1	1	1	1	1	1	1	1	1
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28
	Bank1	4	6	18	18	4	6	18	22	18	22
	Bank2	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26
	Bank5	14	18	20	24	14	18	20	24	20	24
	Bank6	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found on the LatticeXP2 product pages on the Lattice website at www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package-specific thermal values.

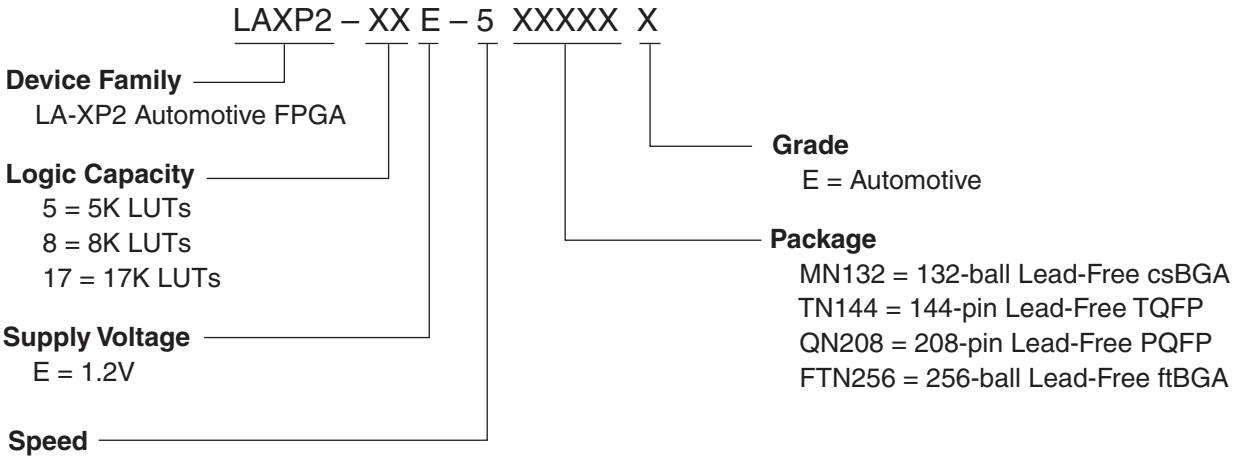
For Further Information

- TN1139 - Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool included with Lattice Diamond design software or as a standalone download from www.latticesemi.com/software

LA-LatticeXP2 Family Data Sheet Ordering Information

August 2014 Data Sheet DS1024

Part Number Description



Ordering Information

The LA-LatticeXP2 devices are marked with a single automotive temperature grade, as shown below.

Automotive Disclaimer

Products are not designed, intended or warranted to be fail-safe and are not designed, intended or warranted for use in applications related to the deployment of airbags. Further, products are not intended to be used, designed or warranted for use in applications that affect the control of the vehicle unless there is a fail-safe or redundancy feature and also a warning signal to the operator of the vehicle upon failure. Use of products in such applications is fully at the risk of the customer, subject to applicable laws and regulations governing limitations on product liability.

Lead-Free Packaging

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-5E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	5
LAXP2-5E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	5
LAXP2-5E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	5
LAXP2-5E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-8E-5MN132E	1.2V	-5	Lead-Free csBGA	132	AUTO	8
LAXP2-8E-5TN144E	1.2V	-5	Lead-Free TQFP	144	AUTO	8
LAXP2-8E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	8
LAXP2-8E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LAXP2-17E-5QN208E	1.2V	-5	Lead-Free PQFP	208	AUTO	17
LAXP2-17E-5FTN256E	1.2V	-5	Lead-Free ftBGA	256	AUTO	17

LA-LatticeXP2 Family Data Sheet Revision History

Revision History

Date	Version	Section	Change Summary
February 2015	1.5	Multiple	Corrected formatting; fixed page, table and figure numbers.
August 2014	1.4	All	Updated for Lattice corporate logo.
		Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
January 2012	01.3	Multiple	Updated for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary information.
May 2009	01.2	Introduction	Added support for 132 csBGA to Features list and Family Selection Guide table.
		Pinout Information	Added support for 132 csBGA to Pin Information Summary table.
		Ordering Information	Added support for 132 csBGA to Part Number Description diagram and Ordering Information tables.
August 2008	01.1	—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Updated Typical Building Block Function Performance table.
			Updated External Switching Characteristics table.
			Updated Internal Switching Characteristics table.
			Updated Family Timing Adders table.
June 2008	01.0	—	Initial release.