Infineon Technologies - CY8C5467AXI-LP108 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5467axi-lp108

VBAT. Battery supply to boost pump.

VCCA. Output of the analog core regulator or the input to the analog core. Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 27.

VCCD. Output of the digital core regulator or the input to the digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 27.

VDDA. Supply for all analog peripherals and analog core regulator. **VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.**

VDDD. Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

VSSA. Ground for all analog peripherals.

VSSB. Ground connection for boost pump.

VSSD. Ground for all digital logic and I/O pins.

VDDIO0, VDDIO1, VDDIO2, VDDIO3. Supply for I/O pins. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

$\overline{\text{XRES}}$. External reset pin. Active low with internal pull-up.

4. CPU

4.1 ARM Cortex-M3 CPU

The CY8C54LP family of devices has an ARM Cortex-M3 CPU core. The Cortex-M3 is a low power 32-bit three-stage pipelined Harvard architecture CPU that delivers 1.25 DMIPS/MHz. It is intended for deeply embedded applications that require fast interrupt handling features.

Table 4-2. Cortex M3 CPU Registers (continued)

Register	Description
PRIMASK	A 1-bit interrupt mask register. When set, it allows only the nonmaskable interrupt (NMI) and hard fault exception. All other exceptions and interrupts are masked.
FAULTMASK	A 1-bit interrupt mask register. When set, it allows only the NMI. All other exceptions and interrupts are masked.
BASEPRI	A register of up to nine bits that define the masking priority level. When set, it disables all interrupts of the same or higher priority value. If set to 0 then the masking function is disabled.
CONTROL	A 2-bit register for controlling the operating mode. Bit 0: 0 = privileged level in thread mode, 1 = user level in thread mode. Bit 1: 0 = default stack (MSP) is used, 1 = alternate stack is used. If in thread mode or user level then the alternate stack is the PSP. There is no alternate stack for handler mode; the bit must be 0 while in handler mode.

4.2 Cache Controller

The CY8C58LP family has a 1 KB, 4-way set-associative instruction cache between the CPU and the flash memory. This guarantees a faster instruction execution rate. The flash cache also reduces system power consumption by requiring less frequent flash access.

4.3 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.3.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

Table 4-3. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, I^2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

4.3.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- Large transactions may be broken into smaller bursts of 1 to 127 bytes
- TDs may be nested and/or chained for complex transactions

4.3.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-4 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

Table 4-4. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

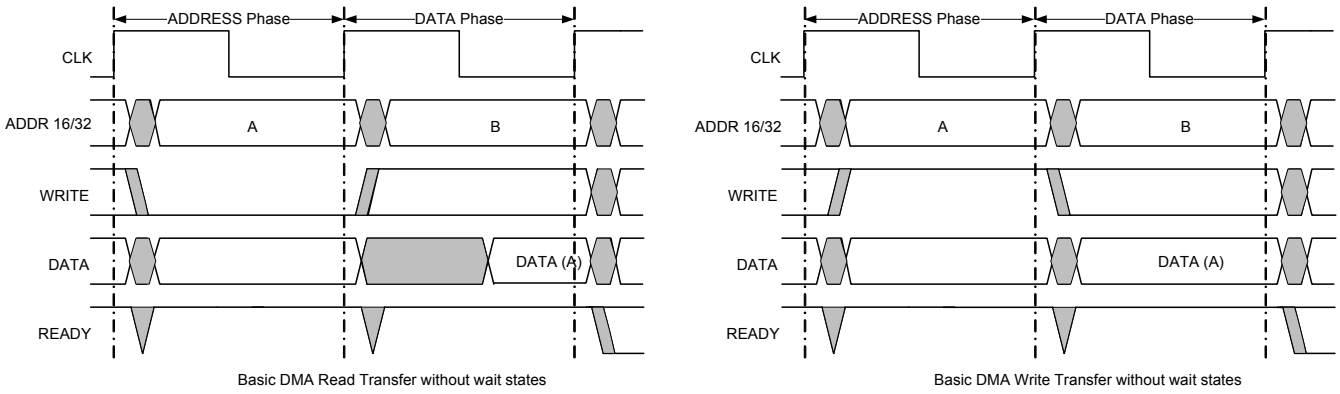
4.3.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.3.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-2. For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-2. DMA Timing Diagram



4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

chains that transmit multiple packets in this way. A similar

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

4.4 Interrupt Controller

The Cortex-M3 NVIC supports 16 system exceptions and 32 interrupts from peripherals, as shown in Table 4-5.

Table 4-5. Cortex-M3 Exceptions and Interrupts

Exception Number	Exception Type	Priority	Exception Table Address Offset	Function
			0x00	Starting value of R13 / MSP
1	Reset	–3 (highest)	0x04	Reset
2	NMI	–2	0x08	Non maskable interrupt
3	Hard fault	–1	0x0C	All classes of fault, when the corresponding fault handler cannot be activated because it is currently disabled or masked
4	MemManage	Programmable	0x10	Memory management fault, for example, instruction fetch from a nonexecutable region
5	Bus fault	Programmable	0x14	Error response received from the bus system; caused by an instruction prefetch abort or data access error
6	Usage fault	Programmable	0x18	Typically caused by invalid instructions or trying to switch to ARM mode
7–10	–	–	0x1C–0x28	Reserved
11	SVC	Programmable	0x2C	System service call via SVC instruction
12	Debug monitor	Programmable	0x30	Debug monitor
13	–	–	0x34	Reserved
14	PendSV	Programmable	0x38	Deferred request for system service
15	SYSTICK	Programmable	0x3C	System tick timer
16–47	IRQ	Programmable	0x40–0x3FC	Peripheral interrupt request #0–#31

Bit 0 of each exception vector indicates whether the exception is executed using ARM or Thumb instructions. Because the Cortex-M3 only supports Thumb instructions, this bit must always be 1. The Cortex-M3 non maskable interrupt (NMI) input can be routed to any pin, via the DSI, or disconnected from all pins. See "DSI Routing Interface Description" section on page 45.

The NVIC handles interrupts from the peripherals, and passes the interrupt vectors to the CPU. It is closely integrated with the CPU for low latency interrupt handling. Features include:

- 32 interrupts. Multiple sources for each interrupt.
- Eight priority levels, with dynamic priority control.
- Priority grouping. This allows selection of preempting and non preempting interrupt levels.
- Support for tail-chaining, and late arrival, of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. All interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

5.6 External Memory Interface

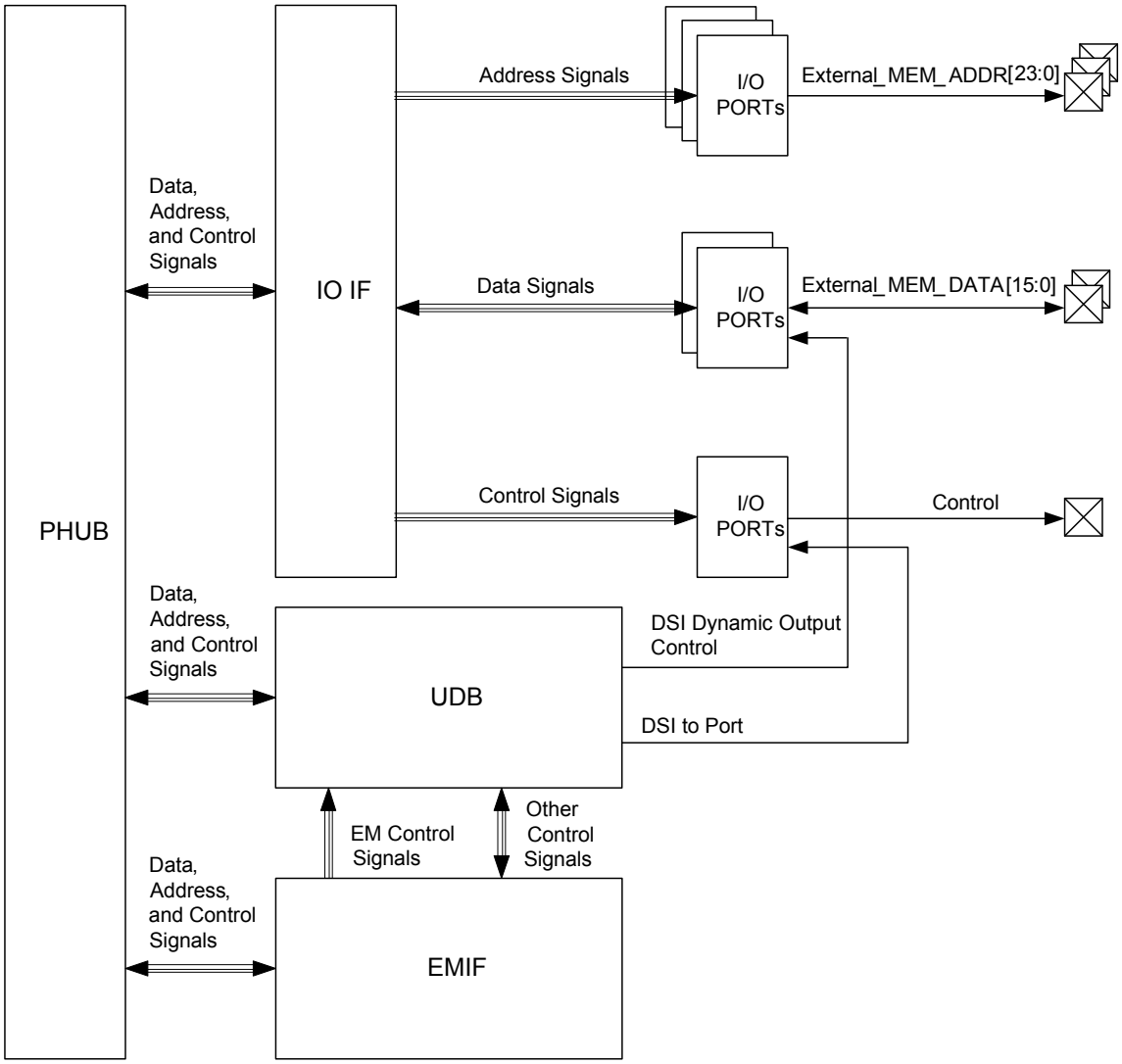
CY8C54LP provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C54LP only supports one type of external memory device at a time.

External memory is located in the Cortex-M3 external RAM space; it can use up to 24 address bits. See Table 5-4 on page 22Memory Map on page 22. The memory can be 8 or 16 bits wide.

Cortex-M3 instructions can be fetched from external memory if it is 16-bit. Other limitations apply; for details, see application note AN89610, PSoC® 4 and PSoC 5LP ARM Cortex Code Optimization.There is no provision for code security in external memory. If code must be kept secure, then it should be placed in internal flash. See Flash Security on page 19 and Device Security on page 63.

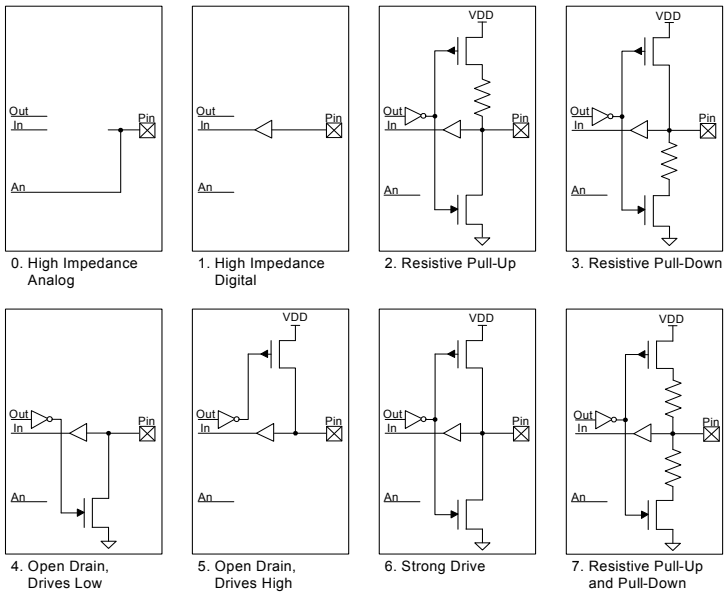
Figure 5-1. EMIF Block Diagram



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode



The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.

Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High-Z	High-Z
1	High Impedance digital	0	0	1	High-Z	High-Z
2	Resistive pull-up[9]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[9]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High-Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High-Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[9]	1	1	1	Res High (5K)	Res Low (5K)

Note
9. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

7. Digital Subsystem

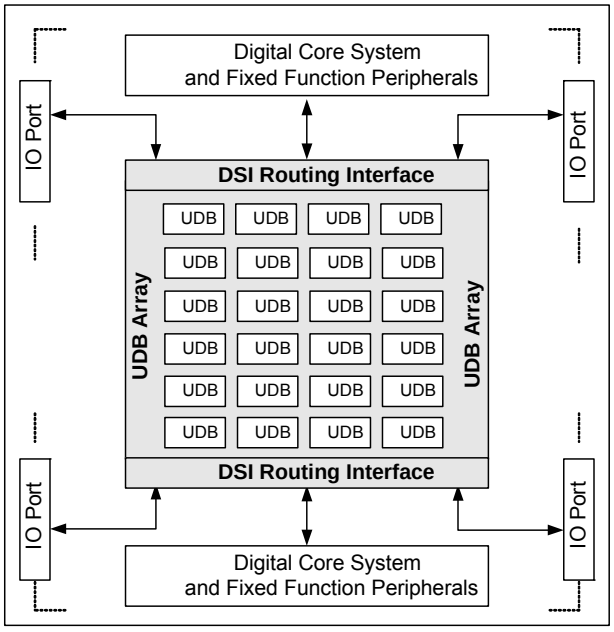
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal digital blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal digital block array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital system interconnect (DSI) - Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block array.

Figure 7-1. CY8C54LP Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C54LP family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C54LP family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C54LP family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C54LP family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

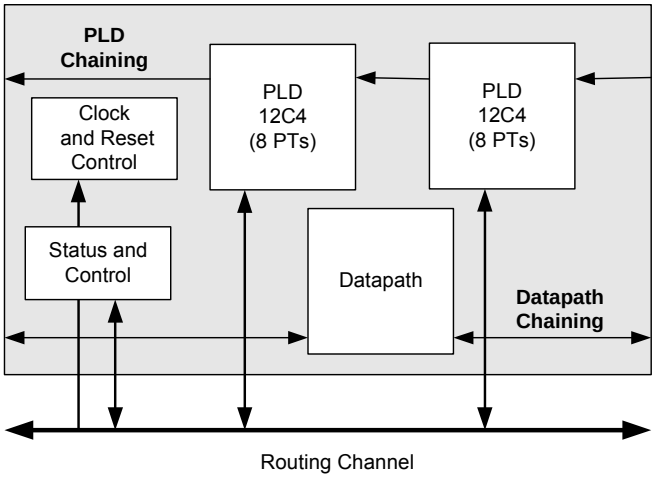
- Amplifiers
  - TIA
  - PGA
  - opamp
- ADC
  - Delta-Sigma
  - Successive Approximation (SAR)
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



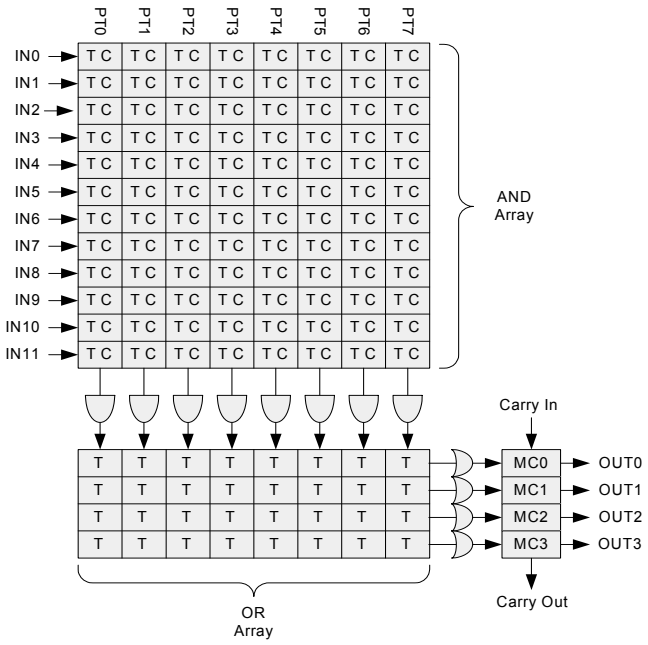
The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V 10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

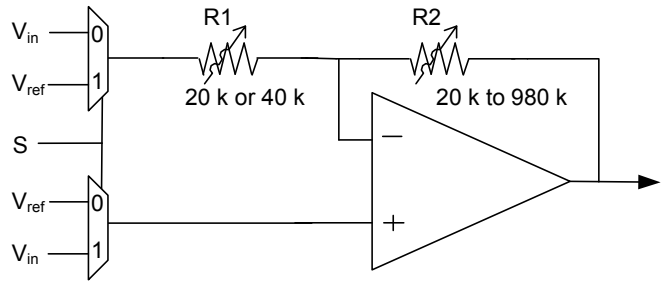
8.6.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

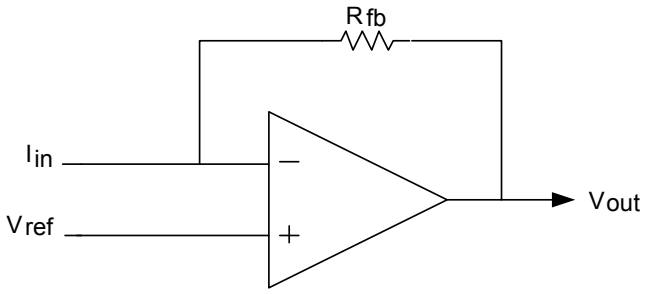
8.6.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.7 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C54LP family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

9.3 Debug Features

The CY8C54LP supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Six program address breakpoints and two literal access breakpoints
- Data watchpoint events to CPU
- Patch and remap instruction from flash to SRAM
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C54LP compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The following trace features are supported:

- Instruction trace
- Data watchpoint on access to data address, address range, or data value
- Trace trigger on data watchpoint
- Debug exception trigger
- Code profiling
- Counters for measuring clock cycles, folded instructions, load/store operations, sleep cycles, cycles per instruction, interrupt overhead
- Interrupt events trace
- Software event monitoring, “printf-style” debugging

9.5 SWV and TRACEPORT Interfaces

The SWV and TRACEPORT interfaces provide trace data to a debug host via the Cypress MiniProg3 or an external trace port analyzer. The 5 pin TRACEPORT is used for rapid transmission of large trace streams. The single pin SWV mode is used to minimize the number of trace pins. SWV is shared with a JTAG pin. If debugging and tracing are done at the same time then SWD may be used with either SWV or TRACEPORT, or JTAG may be used with TRACEPORT, as shown in Table 9-1.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
TRACEPORT	5
JTAG + TRACEPORT	9 or 10
SWD + SWV	3
SWD + TRACEPORT	7

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. Designers can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 5LP offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a ‘1’ if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a ‘0’ if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see “Flash Security” section on page 19). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 27	0.9	1	1.1	µF

Figure 11-5. Analog and Digital Regulators, V_{CC} vs V_{DD}, 10 mA Load

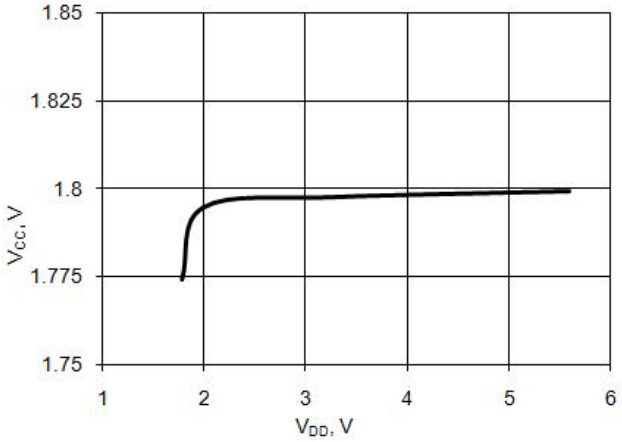
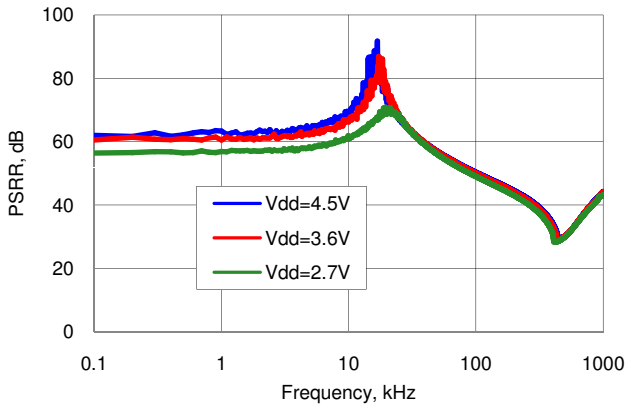


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}

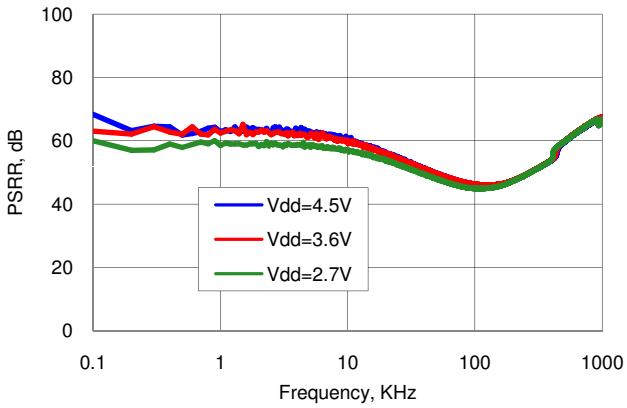


Table 11-12. SIO Comparator Specifications[36]

Parameter	Description	Conditions	Min	Typ	Max	Units
Vos	Offset voltage	V_{DDIO} = 2 V	–	–	68	mV
		V_{DDIO} = 2.7 V	–	–	72	
		V_{DDIO} = 5.5 V	–	–	82	
TCVos	Offset voltage drift with temp		–	–	250	µV/°C
CMRR	Common mode rejection ratio	V_{DDIO} = 2 V	30	–	–	dB
		V_{DDIO} = 2.7 V	35	–	–	
		V_{DDIO} = 5.5 V	40	–	–	
Tresp	Response time		–	–	30	ns

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 66.

Table 11-13. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance[36]	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance[36]	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high[36]	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low[36]	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vihgpio	Input voltage high, GPIO mode[36]	V_{DDD} = 1.8 V	1.5	–	–	V
		V_{DDD} = 3.3 V	2	–	–	V
		V_{DDD} = 5.0 V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode[36]	V_{DDD} = 1.8 V	–	–	0.8	V
		V_{DDD} = 3.3 V	–	–	0.8	V
		V_{DDD} = 5.0 V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode[36]	I_{OH} = 4 mA, V_{DDD} = 1.8 V	1.6	–	–	V
		I_{OH} = 4 mA, V_{DDD} = 3.3 V	3.1	–	–	V
		I_{OH} = 4 mA, V_{DDD} = 5.0 V	4.2	–	–	V
Volgpio	Output voltage low, GPIO mode[36]	I_{OL} = 4 mA, V_{DDD} = 1.8 V	–	–	0.3	V
		I_{OL} = 4 mA, V_{DDD} = 3.3 V	–	–	0.3	V
		I_{OL} = 4 mA, V_{DDD} = 5.0 V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+)–(D–)|	–	–	0.2	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single ended receiver threshold		0.8	–	2	V
Rps2	PS/2 pull-up resistance[36]	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor [36]	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance[36]	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance		–	–	20	pF
I_{IL}[36]	Input leakage current (absolute value)[36]	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Note
36. Based on device characterization (Not production tested).

Figure 11-27. Opamp Vos vs Vcommon and V_{DDA}, 25 °C

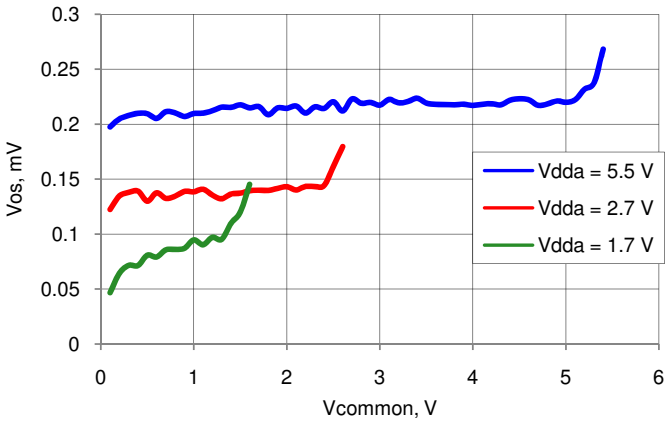


Figure 11-28. Opamp Output Voltage vs Load Current and Temperature, High Power Mode, 25 °C, V_{DDA} = 2.7 V

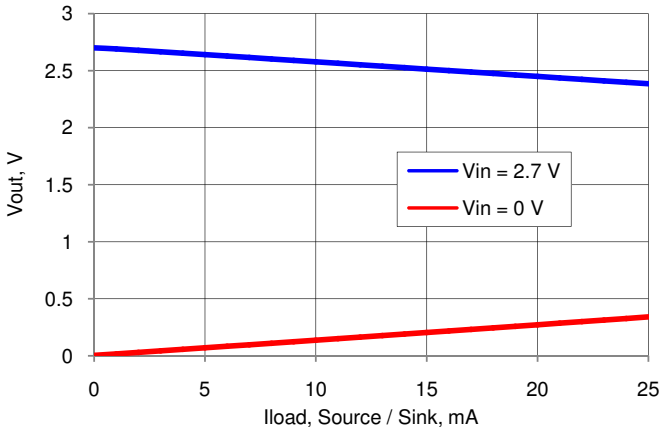


Figure 11-29. Opamp Operating Current vs V_{DDA} and Power Mode

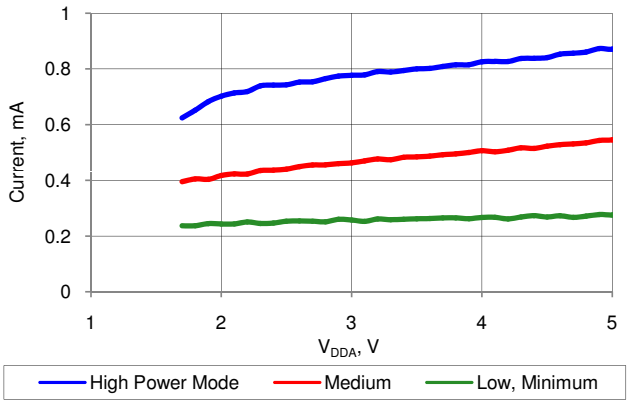


Table 11-19. Opamp AC Specifications[40]

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	–	–	MHz
		Power mode = low, 15 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = minimum, 15 pF load	1.1	–	–	V/µs
		Power mode = low, 15 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, V_{DDA} = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Note
40. Based on device characterization (Not production tested).

Figure 11-46. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

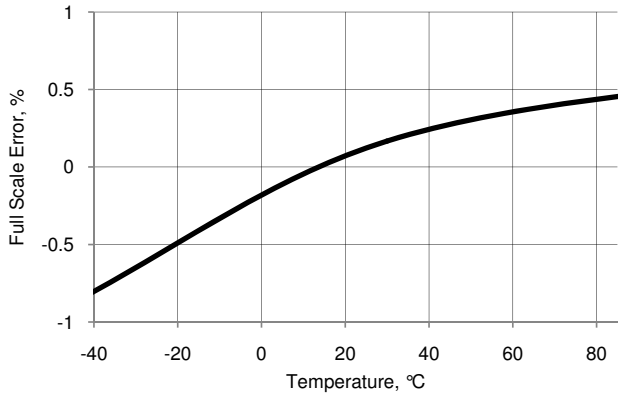


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

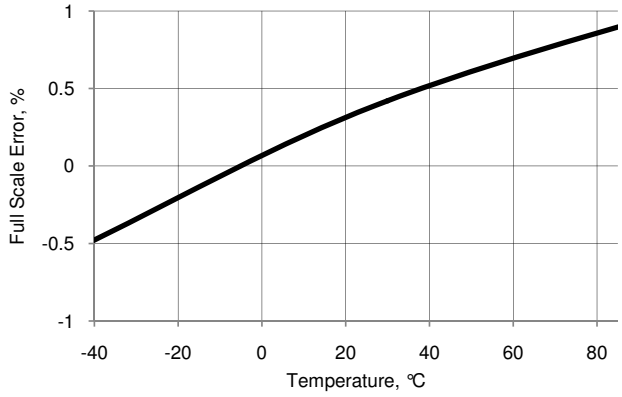


Figure 11-48. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

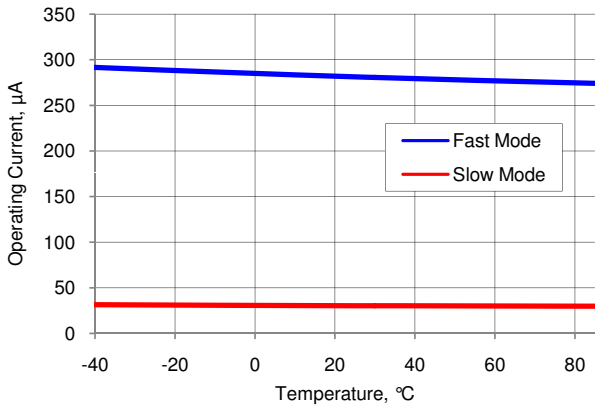


Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

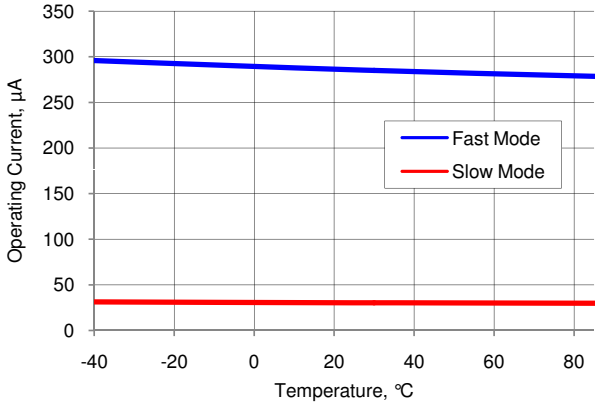


Table 11-31. IDAC AC Specifications[54]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
		Range = 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Note
54. Based on device characterization (Not production tested).

Figure 11-50. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

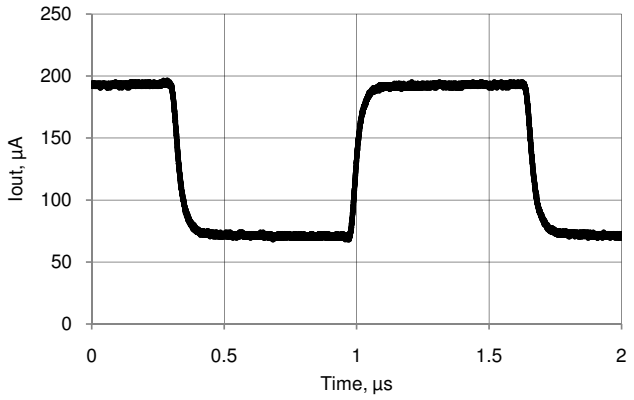


Figure 11-51. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

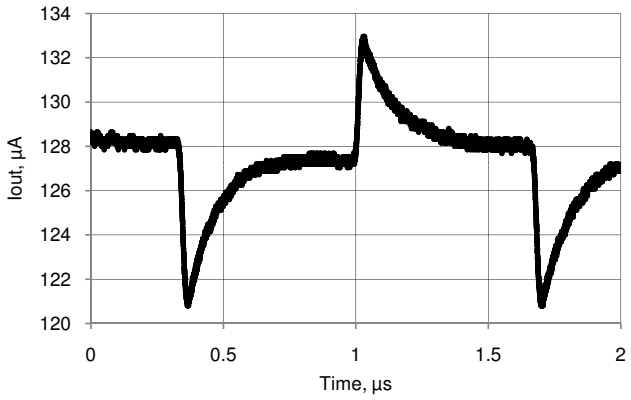


Figure 11-52. IDAC PSRR vs Frequency

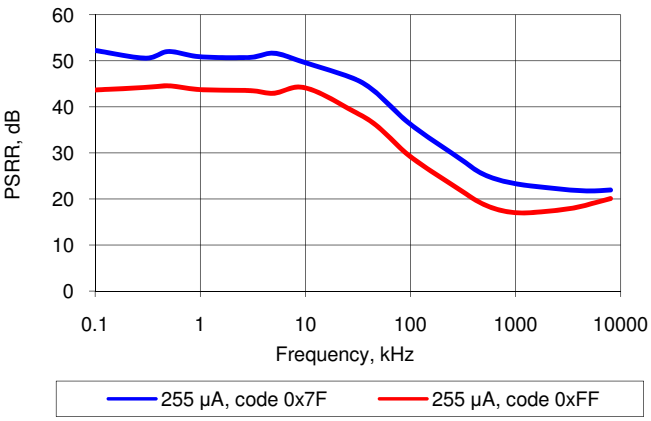
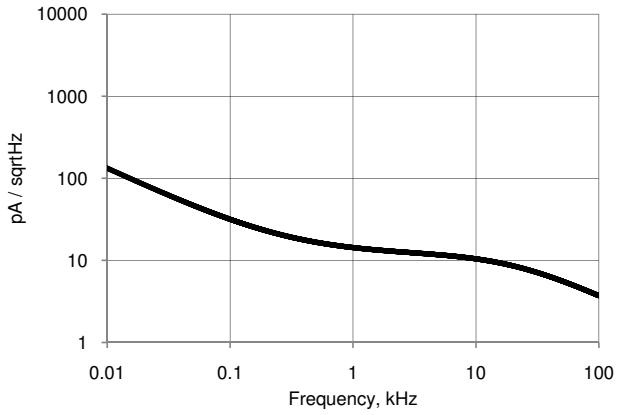


Figure 11-53. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V



11.5.7 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-32. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
INL4	Integral nonlinearity[55]	4 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
DNL4	Differential nonlinearity[55]	4 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ

Note
55. Based on device characterization (Not production tested).

11.7.3 Nonvolatile Latches (NVL)

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1 K	–	–	Program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	Program/ erase cycles
	NVL data retention time	Average ambient temp. $T_A \le 55$ °C	20	–	–	Years
		Average ambient temp. $T_A \le 85$ °C	10	–	–	Years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage[70]		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	80.01	MHz

Note
70. Based on device characterization (Not production tested).

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 Internal Main Oscillator

Table 11-71. IMO DC Specifications[85]

Parameter	Description	Conditions	Min	Typ	Max	Units
Icc_imo	Supply current					
	74.7 MHz		–	–	730	µA
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-74. IMO Current vs. Frequency

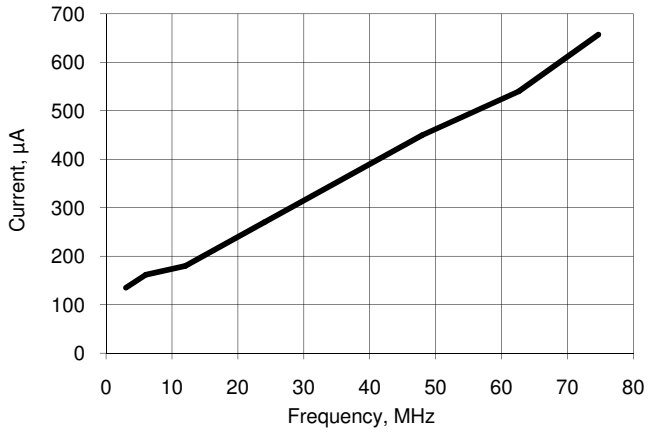


Table 11-72. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	74.7 MHz		–7	–	7	%
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz		–2	–	2	%
Tstart_imo	Startup time[85]	From enable (during normal system operation)	–	–	13	µs

Note
85. Based on device characterization (Not production tested).

Table 11-72. IMO AC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Jp-p	Jitter (peak to peak)[86]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[86]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-75. IMO Frequency Variation vs. Temperature

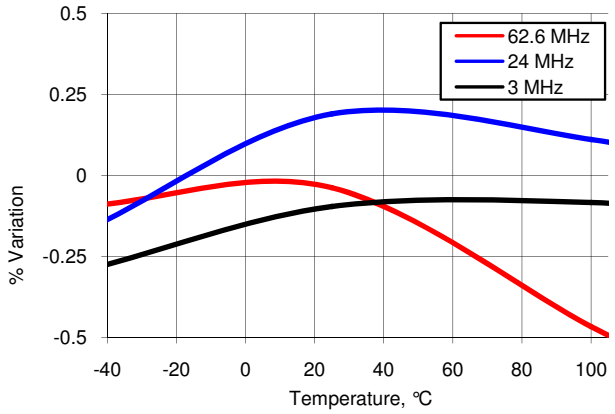
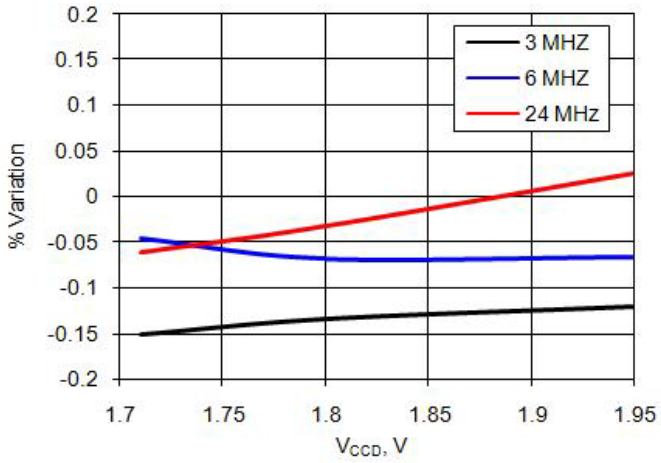


Figure 11-76. IMO Frequency Variation vs. V_{CC}



Note
86. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C54LP device includes: up to 256 KB flash, 64 KB SRAM, 2 KB EEPROM, a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, JTAG/SWD programming and debug, external memory interface, boost, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C54LP derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C54LP Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog							Digital			I/O[94]				Package	JTAG ID[95]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparators	SC/CT Analog Blocks[92]	Opamps	DFB	CapSense	UDBs[93]	16-bit Timer/PWM	FS USB	Total I/O	GPIO	SIO	USBIO		
CY8C5468LTI-LP026	67	256	64	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	48	38	8	2	68-QFN	0x2E11A069
CY8C5468AXI-LP106	67	256	64	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	72	62	8	2	100-TQFP	0x2E16A069
CY8C5468AXI-LP042	67	256	64	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	72	62	8	2	100-TQFP	0x2E12A069
CY8C5467LTI-LP003	67	128	32	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	48	38	8	2	68-QFN	0x2E103069
CY8C5467AXI-LP108	67	128	32	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	72	62	8	2	100-TQFP	0x2E16C069
CY8C5466AXI-LP002	67	64	16	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	✔	72	62	8	2	100-TQFP	0x2E102069
CY8C5466LTI-LP072	67	64	16	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	–	46	38	8	0	68-QFN	0x2E148069
CY8C5466LTI-LP085	67	64	16	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	✔	48	38	8	2	68-QFN	0x2E155069
CY8C5466AXI-LP107	67	64	16	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	–	70	62	8	0	100-TQFP	0x2E16B069
CY8C5465AXI-LP043	67	32	8	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	✔	72	62	8	2	100-TQFP	0x2E12B069
CY8C5465LTI-LP104	67	32	8	2	✔	1x12-bit SAR	2	4	2	2	–	✔	20	4	✔	48	38	8	2	68-QFN	0x2E168069
CY8C5488AXI-LP120	80	256	64	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	72	62	8	2	100-TQFP	0x2E178069
CY8C5488LTI-LP093	80	256	64	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	48	38	8	2	68-QFN	0x2E15D069
CY8C5488FNI-LP212	80	256	64	2	✔	1x12-bit SAR	2	4	2	2	–	✔	24	4	✔	72	62	8	2	99-WLCSP	0x2E1D4069

Notes

92. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 40 for more information on how analog blocks can be used.
93. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 40 for more information on how UDBs can be used.
94. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See I/O System and Routing on page 33 for details on the functionality of each of these types of I/O.
95. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

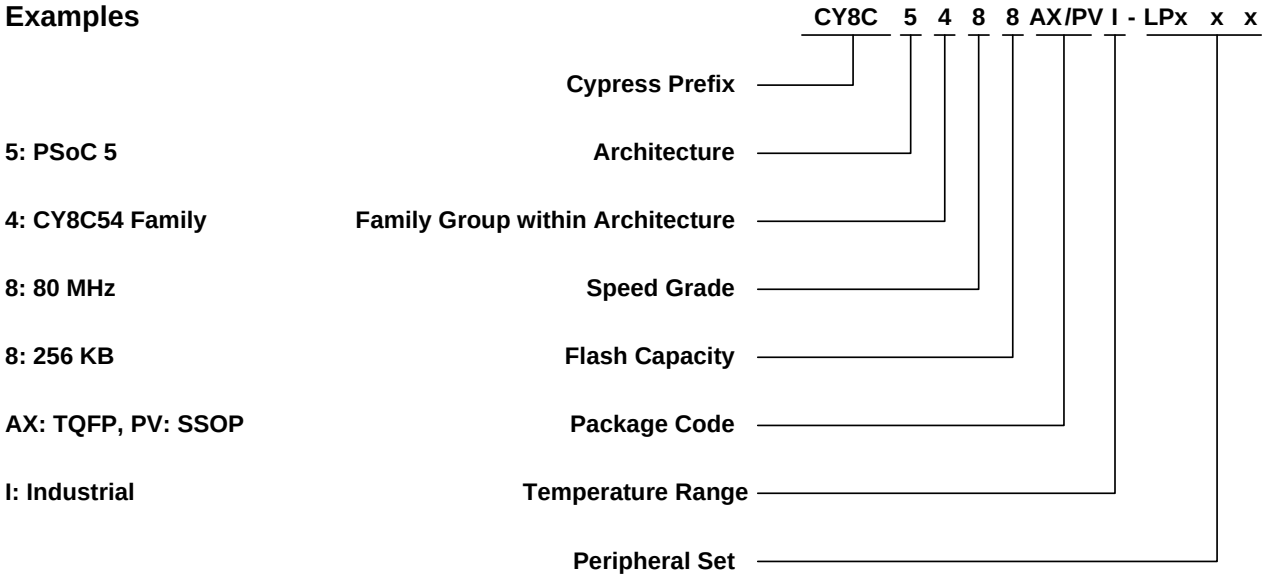
12.1 Part Numbering Conventions

PSoC 5LP devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-LPxxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 2: CY8C52LP family
  - 4: CY8C54LP family
  - 6: CY8C56LP family
  - 8: CY8C58LP family
- c: Speed grade
  - 6: 67 MHz
  - 8: 80 MHz
- d: Flash capacity
  - 5: 32 KB
  - 6: 64 KB
  - 7: 128 KB
  - 8: 256 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - FN: CSP
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters

Examples



Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 5LP CY8C54LP family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.