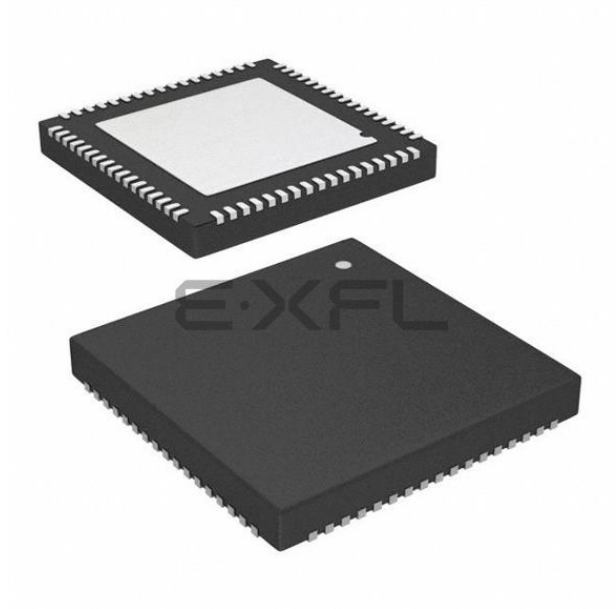

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5467lti-lp003

Contents

The CY8C54LP family supports a wide supply operating range from 1.71 to 5.5 V. This allows operation from regulated supplies such as 1.8 ± 5%, 2.5 V ±10%, 3.3 V ± 10%, or 5.0 V ± 10%, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5 V. This enables the device to be powered directly from a single battery. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3 V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 300-nA hibernate mode with RAM retention and a 2-µA sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 3.1 mA when the CPU is running at 6 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 27 of this datasheet.

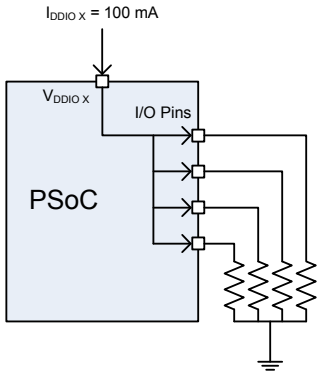
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include FPB, DWT, ETM, and ITM. These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 60 of this datasheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 and Figure 2-4, as well as Table 2-1, show the pins that are powered by each VDDIO.

Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit

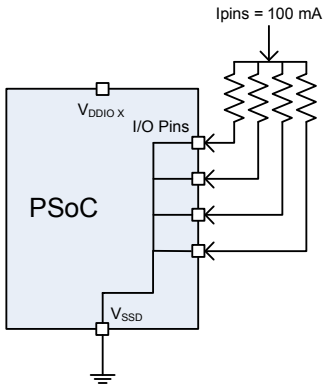


Figure 4-1. ARM Cortex-M3 Block Diagram

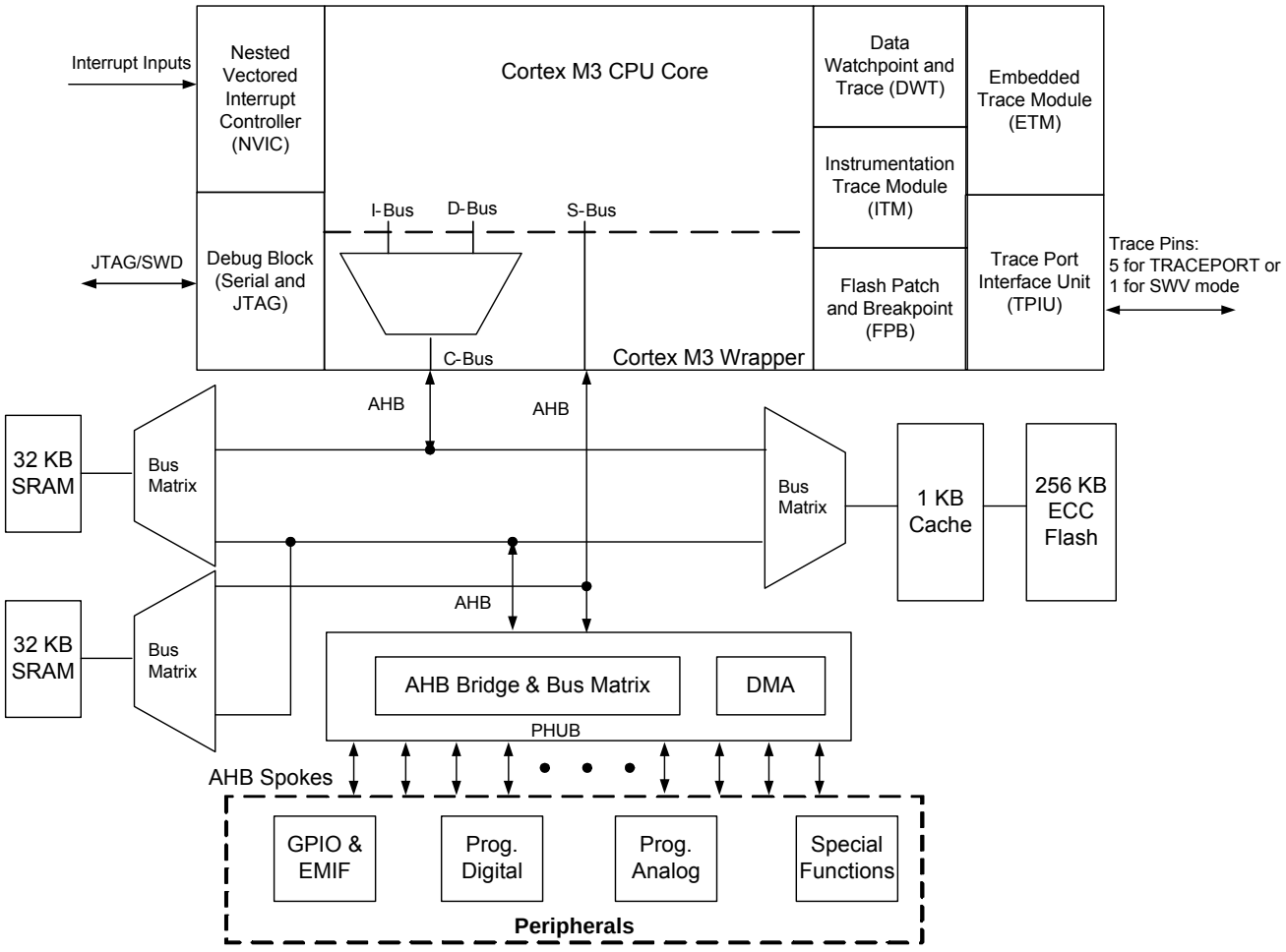
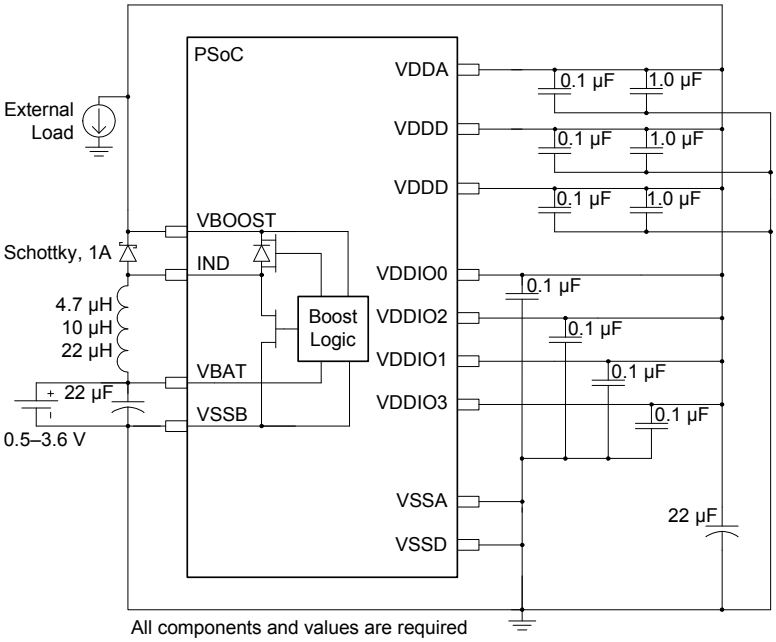
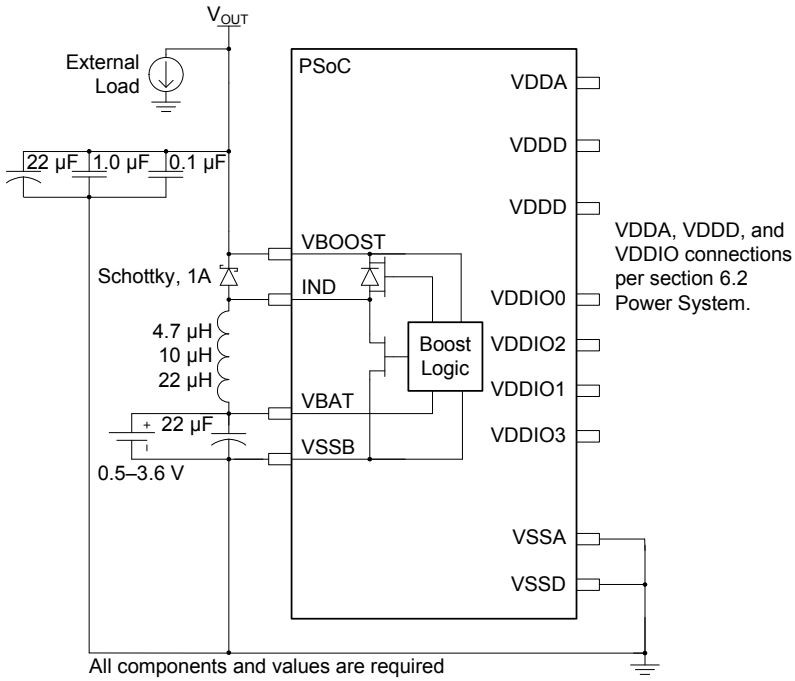


Figure 6-6. Application of Boost Converter powering PSoC device



The boost converter may also generate a supply that is not used directly by the PSoC device. An example of this use case is boosting a 1.8 V supply to 4.0 V to drive a white LED. If the boost converter is not supplying the PSoC devices V_{DDA}, V_{DDD}, and V_{DDIO} it must comply with the same design rules as supplying the PSoC device, but with a change to the bulk capacitor requirements. A parallel arrangement 22 µF, 1.0 µF, and 0.1 µF capacitors are all required on the Vout supply and must be placed within 1 cm of the VBOOST pin to ensure regulator stability.

Figure 6-7. Application of Boost Converter not powering PSoC device



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-10 on page 35 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated VDDIO supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-12 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low Power Functionality

In all low power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in "Pinouts" on page 6. The special features are:

- Digital
  - 4- to 25-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - TRACEPORT interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all pins for board level test.

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

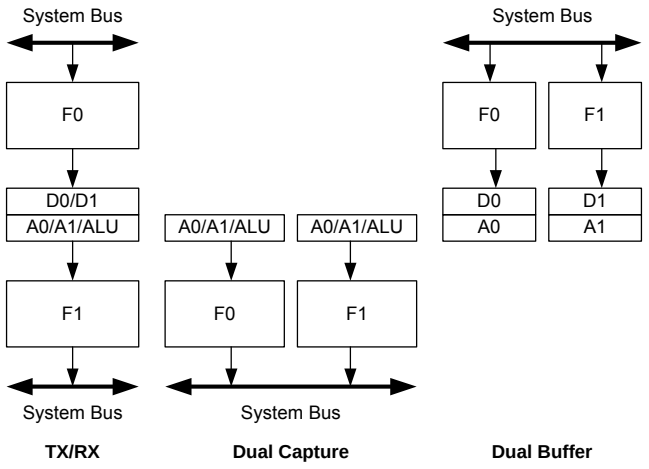
7.2.2.5 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-5. Example FIFO Configurations



7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

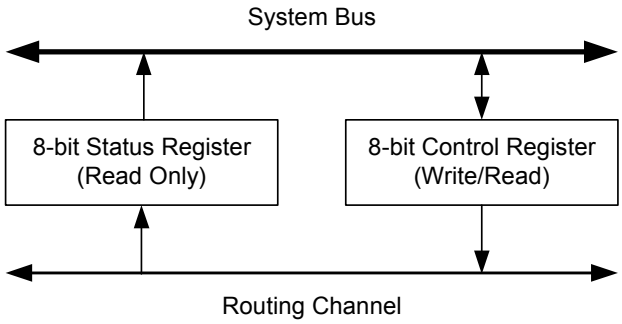
7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-6. Status and Control Registers

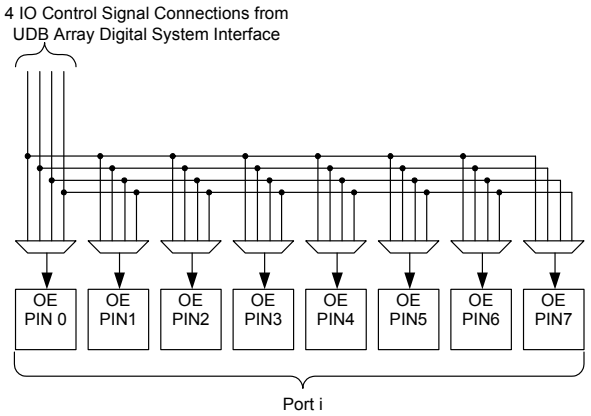


The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

7.2.3.1 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a “compare true” condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

Figure 7-13. I/O Pin Output Enable Connectivity



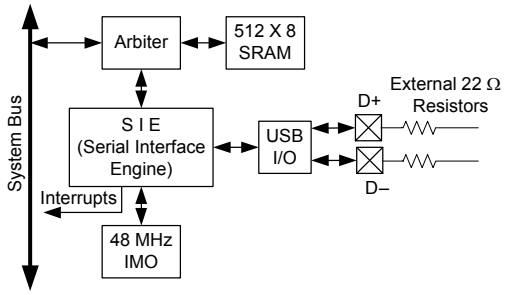
7.5 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz oscillator that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-14. USB



7.6 Timers, Counters, and PWMs

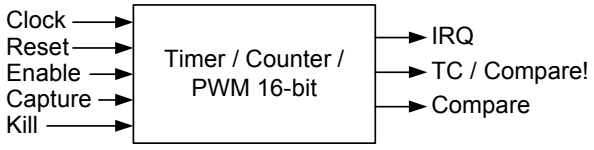
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-15. Timer/Counter/PWM



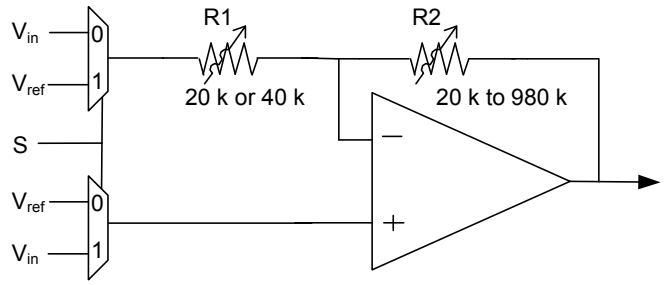
8.6.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

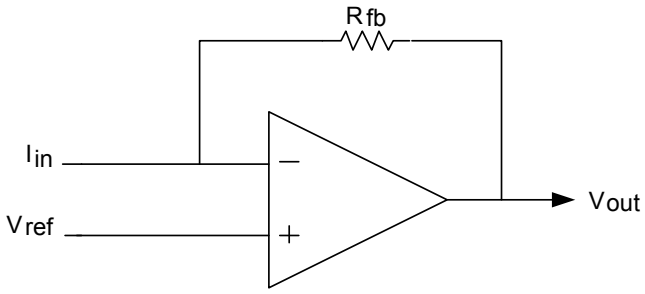
8.6.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.7 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C54LP family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled		1.8	–	V_{DDA}[15]	V
				–	–	V_{DDA} + 0.1[17]	
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V
V_{DDIO}[16]	I/O supply voltage relative to V_{SSIO}			1.71	–	V_{DDA}[15]	V
				–	–	V_{DDA} + 0.1[17]	
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
Active Mode							
I_{DD}[18]	Sum of digital and analog IDDD + IDDA. IDDIOX for I/Os not included. IMO enabled, bus clock and CPU clock enabled. CPU executing complex program from flash	V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 3 MHz[19]	T = –40 °C	–	1.9	3.8	mA
			T = 25 °C	–	1.9	3.8	
			T = 85 °C	–	2	3.8	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 6 MHz	T = –40 °C	–	3.1	5	
			T = 25 °C	–	3.1	5	
			T = 85 °C	–	3.2	5	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 12 MHz[19]	T = –40 °C	–	5.4	7	
			T = 25 °C	–	5.4	7	
			T = 85 °C	–	5.6	7	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 24 MHz[19]	T = –40 °C	–	8.9	10.5	
			T = 25 °C	–	8.9	10.5	
			T = 85 °C	–	9.1	10.5	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 48 MHz[19]	T = –40 °C	–	15.5	17	
			T = 25 °C	–	15.4	17	
			T = 85 °C	–	15.7	17	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 62 MHz	T = –40 °C	–	18	19.5	
			T = 25 °C	–	18	19.5	
			T = 85 °C	–	18.5	19.5	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 74 MHz	T = –40 °C	–	26.5	30	
			T = 25 °C	–	26.5	30	
			T = 85 °C	–	27	30	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 80 MHz, IMO = 3 MHz with PLL	T = –40 °C	–	22	25.5	
			T = 25 °C	–	22	25.5	
			T = 85 °C	–	22.5	25.5	

Notes

15. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.
16. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
17. Guaranteed by design, not production tested.
18. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
19. Based on device characterization (Not production tested).

Figure 11-1. Active Mode Current vs F_{CPU}, V_{DD} = 3.3 V, Temperature = 25 °C

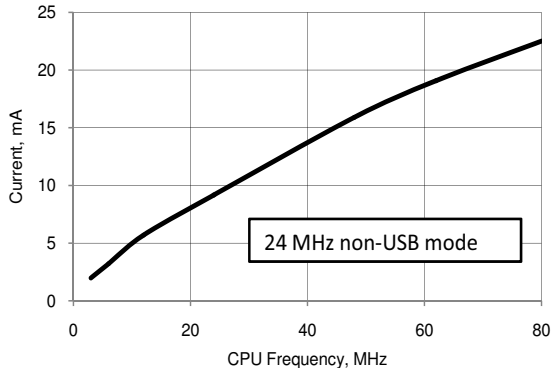


Figure 11-2. I_{DD} vs Frequency at 25 °C

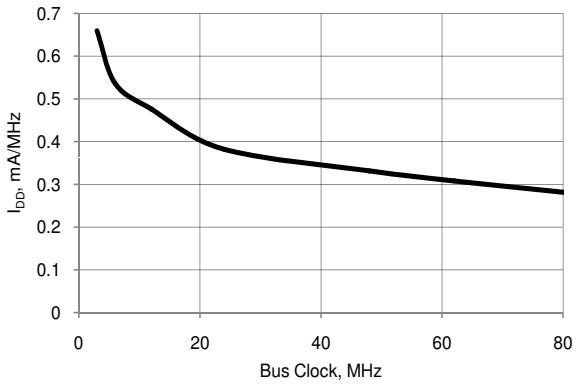


Figure 11-3. Active Mode Current vs Temperature and F_{CPU}, V_{DD} = 3.3 V

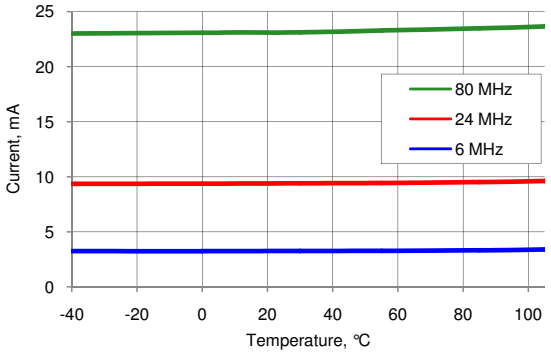


Figure 11-4. Active Mode Current vs V_{DD} and Temperature, F_{CPU} = 24 MHz

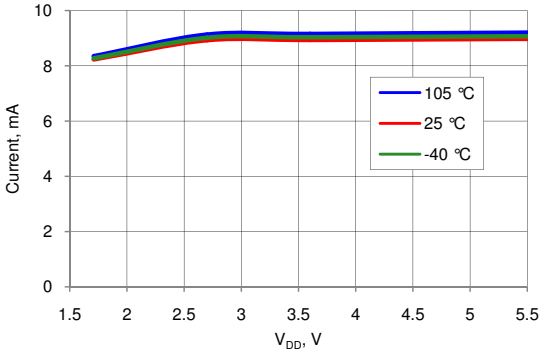


Table 11-3. AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	80.01	MHz
F_{BUSCLK}	Bus frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	80.01	MHz
S_{VDD}[24]	V_{DD} ramp rate		–	–	0.066	V/µs
T_{IO_INIT}[24]	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ IPOR to I/O ports set to their reset states		–	–	10	µs
$T_{STARTUP}$[24]	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ PRES to CPU executing code at reset vector	V_{CCA}/V_{DDA} = regulated from V_{DDA}/V_{DDD}, no PLL used, fast IMO boot mode (48 MHz typ.)	–	–	33	µs
		V_{CCA}/V_{CCD} = regulated from V_{DDA}/V_{DDD}, no PLL used, slow IMO boot mode (12 MHz typ.)	–	–	66	µs
T_{SLEEP}[24]	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	25	µs
$T_{HIBERNATE}$[24]	Wakeup form hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	150	µs

Note
24. Based on device characterization (Not production tested).

Figure 11-17. SIO Output High Voltage and Current, Unregulated Mode

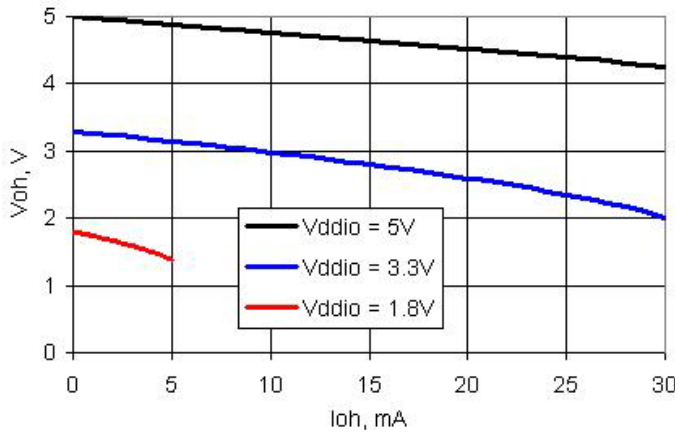


Figure 11-18. SIO Output Low Voltage and Current, Unregulated Mode

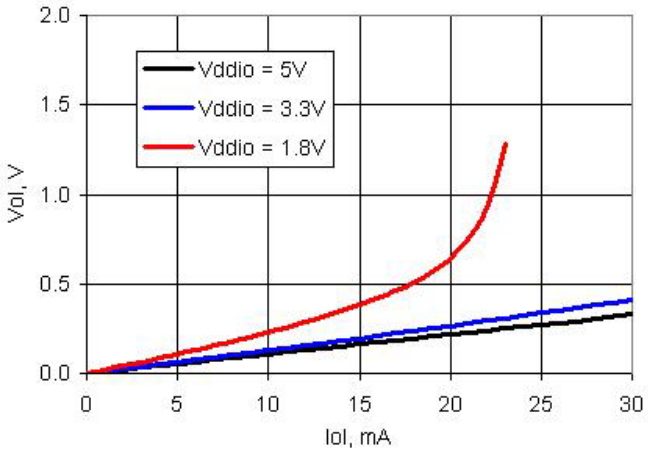


Figure 11-19. SIO Output High Voltage and Current, Regulated Mode

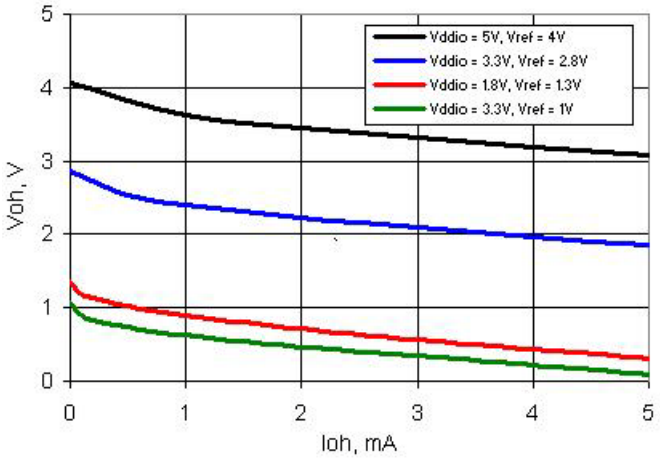


Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode

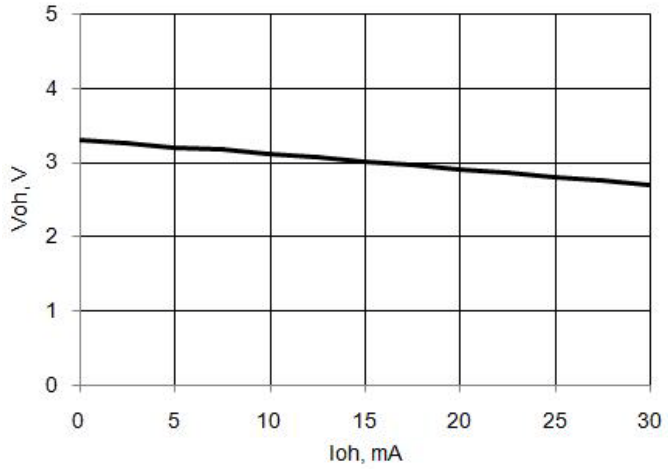


Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode

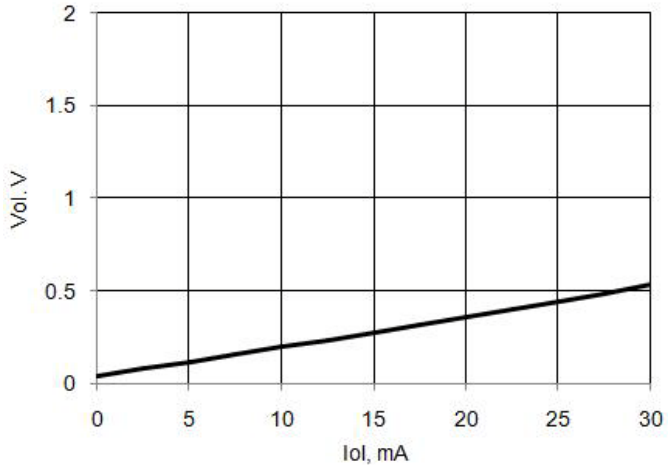


Table 11-14. USBIO AC Specifications[37]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ V_{DDD} ≤ 5.5 V	–	–	20	MHz
		V_{DDD} = 1.71 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns

Note
37. Based on device characterization (Not production tested).

Figure 11-46. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

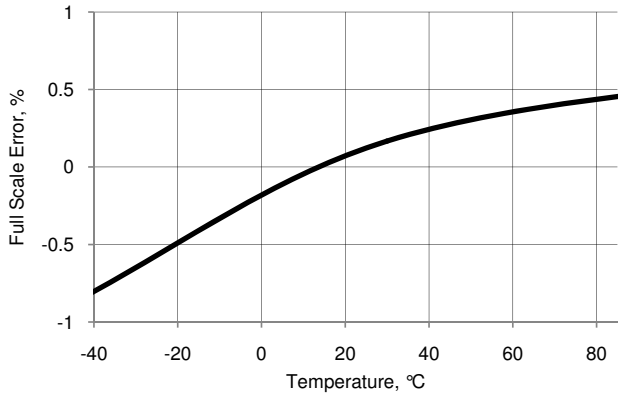


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

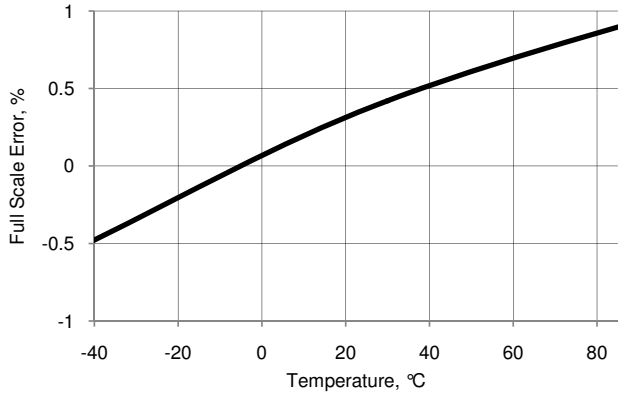


Figure 11-48. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

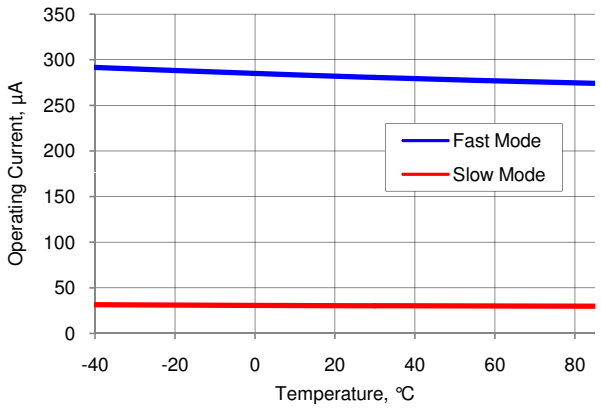


Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

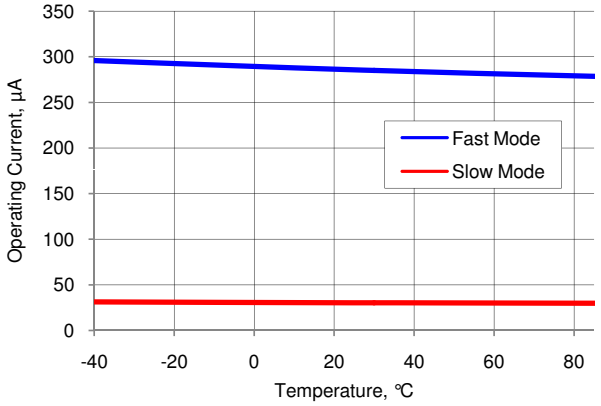


Table 11-31. IDAC AC Specifications[54]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
		Range = 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Note
54. Based on device characterization (Not production tested).

Figure 11-58. VDAC Full Scale Error vs Temperature, 1 V Mode

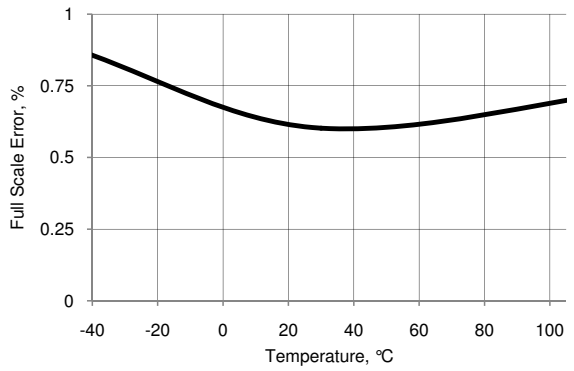


Figure 11-59. VDAC Full Scale Error vs Temperature, 4 V Mode

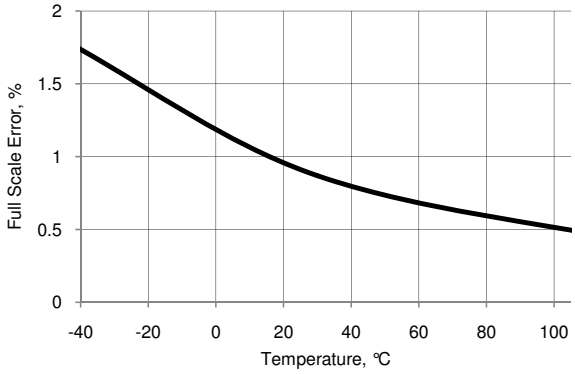


Figure 11-60. VDAC Operating Current vs Temperature, 1V Mode, Slow Mode

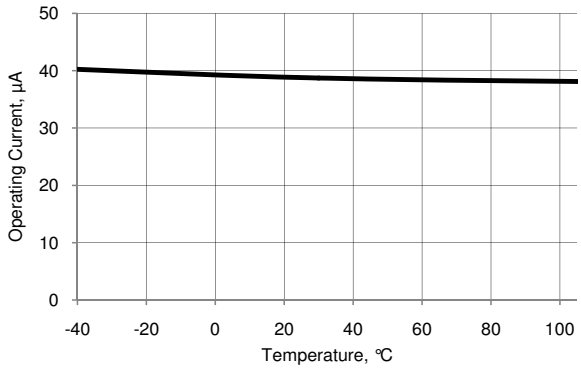


Figure 11-61. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode

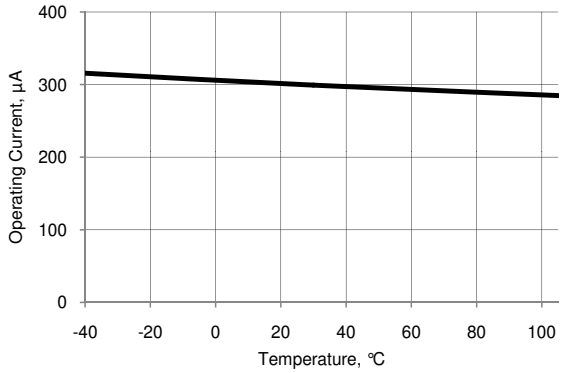


Table 11-33. VDAC AC Specifications[57]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
TsettleP	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	3.2	µs
TsettleN	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	3	µs
	Voltage noise	Range = 1 V, fast mode, V_{DDA} = 5 V, 10 kHz	–	750	–	nV/sqrtHz

Note
57. Based on device characterization (Not production tested).

11.6.4 I²C

Table 11-49. Fixed I²C DC Specifications[66]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	–	250	µA
		Enabled, configured for 400 kbps	–	–	260	µA

Table 11-50. Fixed I²C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	1	Mbps

11.6.5 USB

Table 11-51. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[67]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

Notes
66. Based on device characterization (Not production tested).
67. Rise/fall time matching (TR) not guaranteed, see Table 11-15 on page 80.

11.7.3 Nonvolatile Latches (NVL)

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1 K	–	–	Program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	Program/ erase cycles
	NVL data retention time	Average ambient temp. $T_A \le 55$ °C	20	–	–	Years
		Average ambient temp. $T_A \le 85$ °C	10	–	–	Years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage[70]		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	80.01	MHz

Note
70. Based on device characterization (Not production tested).

11.7.5 External Memory Interface

Figure 11-70. Asynchronous Write and Read Cycle Timing, No Wait States

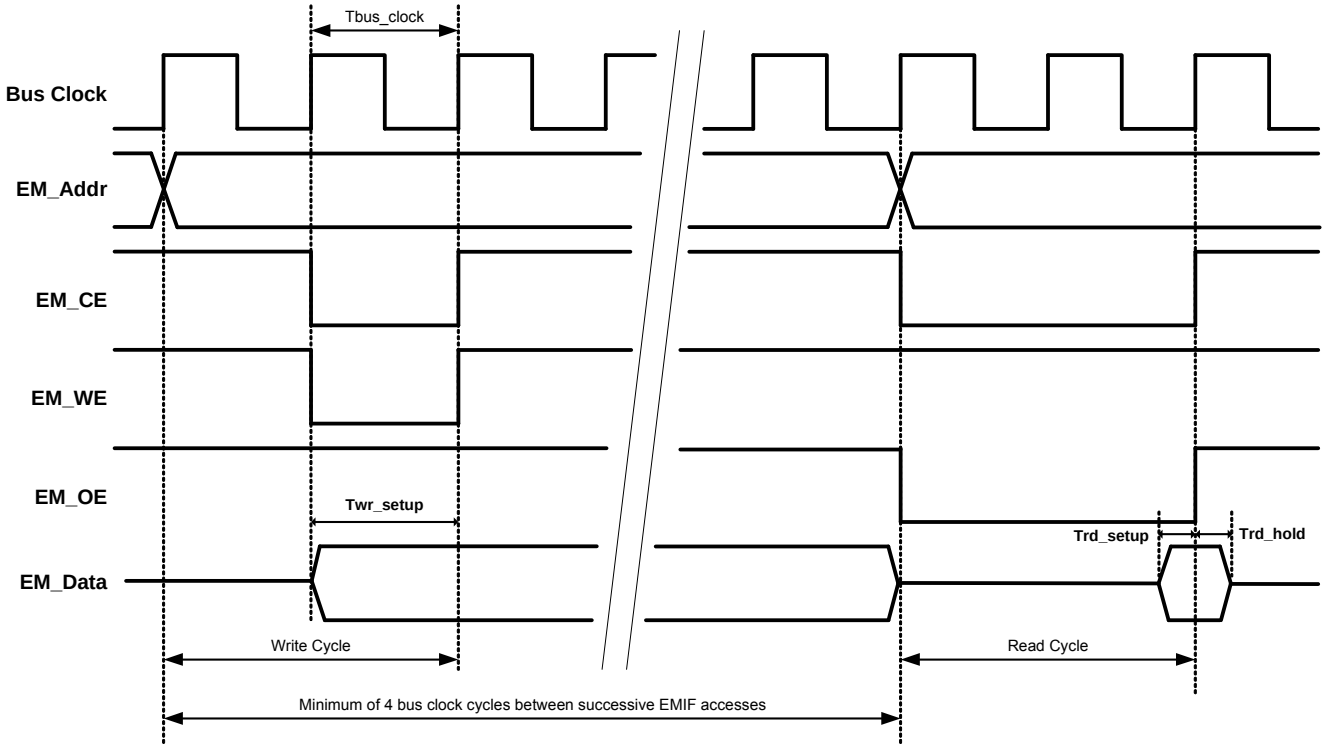


Table 11-61. Asynchronous Write and Read Timing Specifications[71]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency[72]		–	–	33	MHz
Tbus_clock	Bus clock period[73]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_WE and EM_CE		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes
71. Based on device characterization (Not production tested).
72. EMIF signal timings are limited by GPIO frequency limitations. See "GPIO" section on page 73.
73. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

11.9.2 Internal Low-Speed Oscillator

Table 11-73. ILO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[87]	F_{OUT} = 1 kHz	–	–	1.7	µA
		F_{OUT} = 33 kHz	–	–	2.6	µA
		F_{OUT} = 100 kHz	–	–	2.6	µA
	Leakage current[87]	Power down mode	–	–	15	nA

Table 11-74. ILO AC Specifications[88]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstart_ilo	Startup time, all frequencies	Turbo mode	–	–	2	ms
F_{ILO}	ILO frequencies					
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz

Figure 11-77. ILO Frequency Variation vs. Temperature

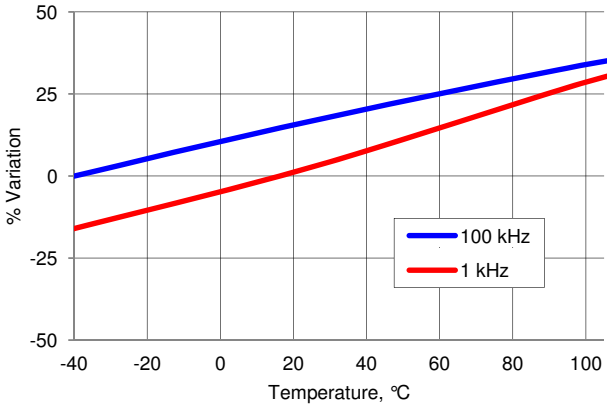
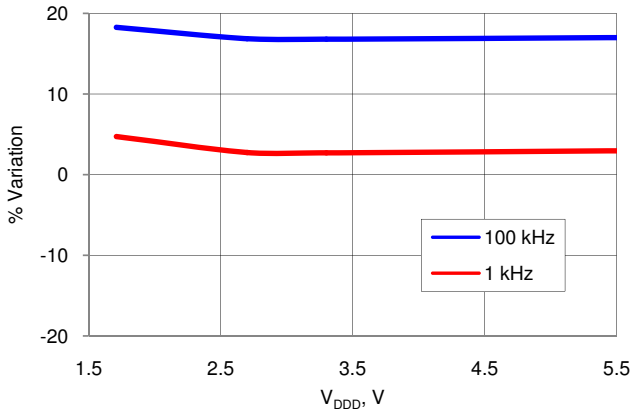


Figure 11-78. ILO Frequency Variation vs. V_{DD}



Notes
87. This value is calculated, not measured.
88. Based on device characterization (Not production tested).

11.9.3 MHz External Crystal Oscillator

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-75. MHzECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[89]	13.56 MHz crystal	–	3.8	–	mA

Table 11-76. MHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 kHz External Crystal Oscillator

Table 11-77. kHzECO DC Specifications[89]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-78. kHzECO AC Specifications[89]

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-79. External Clock Reference AC Specifications[89]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-80. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 80 MHz	–	650	–	µA
		In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-81. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[90]		1	–	48	MHz
	PLL intermediate frequency[91]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[90]		24	–	80	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[89]		–	–	250	ps

Notes
89. Based on device characterization (Not production tested).
90. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
91. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T_A	Operating ambient temperature	For CSP parts	–40	25	85	°C
T_J	Operating junction temperature	For CSP parts	–40	–	100	°C
T_{JA}	Package θ_{JA} (99-ball CSP)			16.5		°C/Watt
T_{Jc}	Package θ_{JC} (99-ball CSP)		–	0.1	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
99-pin CSP	255 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
99-pin CSP	MSL 1