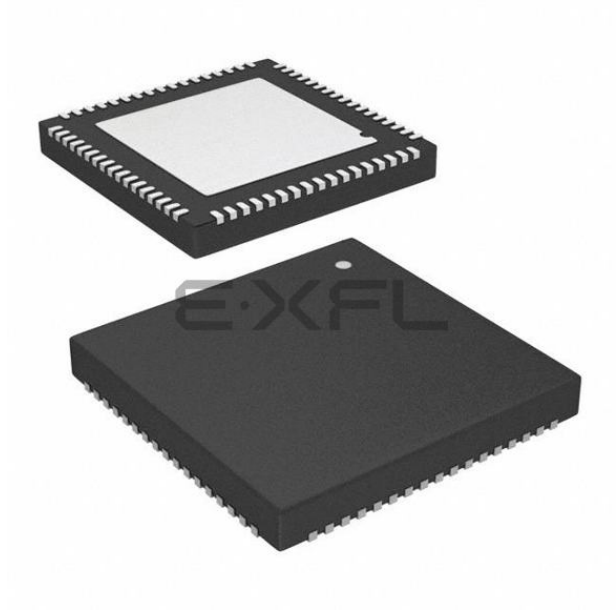

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5468lti-lp026

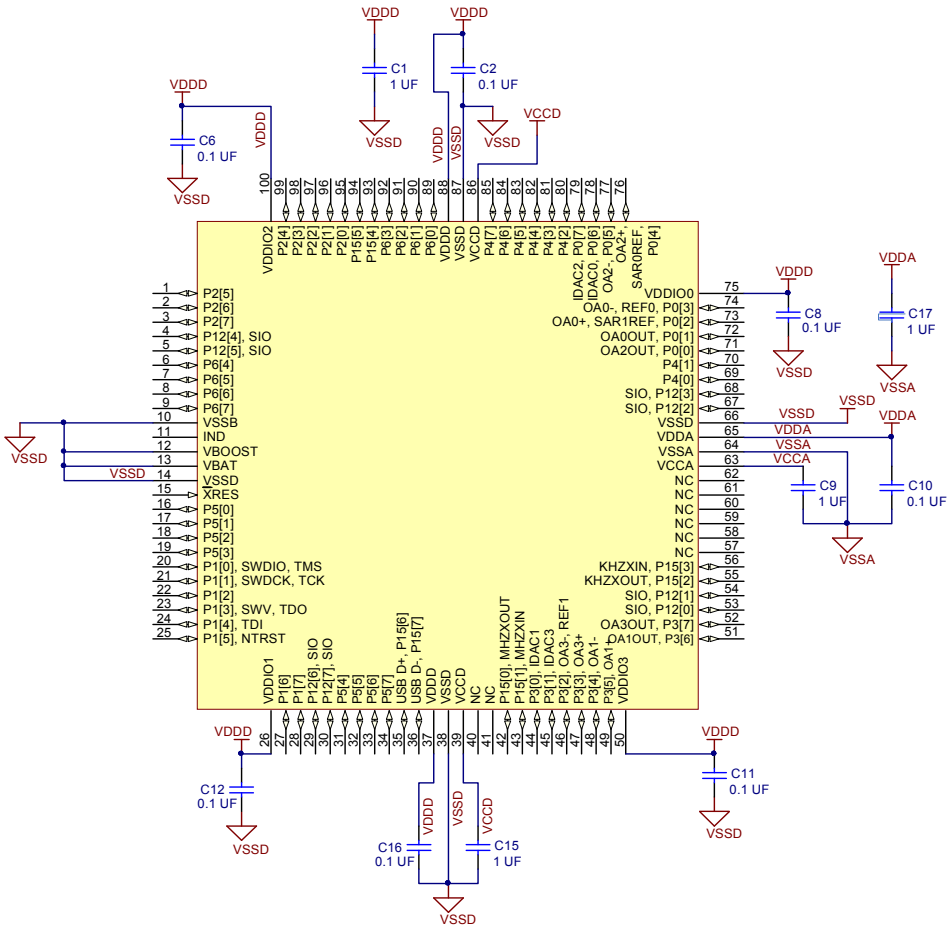
Contents

Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a 2-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 27. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

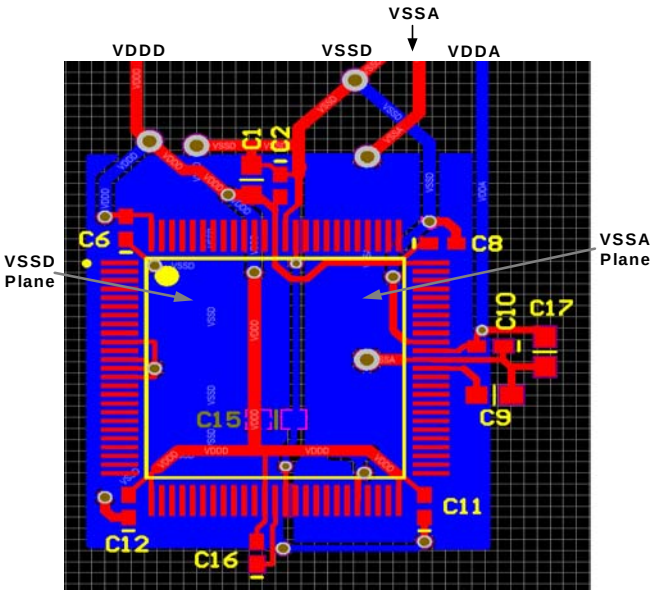
Figure 2-5. Example Schematic for 100-Pin TQFP Part with Power Connections



Note The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.

For more information on pad layout, refer to http://www.cypress.com/cad-resources/psoc-5lp-cad-libraries.

Figure 2-6. Example PCB Layout for 100-Pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2. Low resistance output pin for high current DACs (IDAC).

Opamp0out, Opamp2out. High current output of uncommitted opamp[6].

Extref0, Extref1. External reference input to the analog system.

SAR0 EXTREF, SAR1 EXTREF. External references for SAR ADCs.

Opamp0-, Opamp2-. Inverting input to uncommitted opamp.

Opamp0+, Opamp2+. Noninverting input to uncommitted opamp.

GPIO. General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[6].

I2C0: SCL, I2C1: SCL. I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA. I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind. Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi. 32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 25 MHz crystal oscillator pin.

nTRST. Optional JTAG Test Reset programming and debug port connection to reset the JTAG connection.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. Serial Wire Debug Clock programming and debug port connection.

SWDIO. Serial Wire Debug Input and Output programming and debug port connection.

TCK. JTAG Test Clock programming and debug port connection.

TDI. JTAG Test Data In programming and debug port connection.

TDO. JTAG Test Data Out programming and debug port connection.

TMS. JTAG Test Mode Select programming and debug port connection.

TRACECLK. Cortex-M3 TRACEPORT connection, clocks TRACEDATA pins.

TRACEDATA[3:0]. Cortex-M3 TRACEPORT connections, output data.

SWV. Single Wire Viewer output.

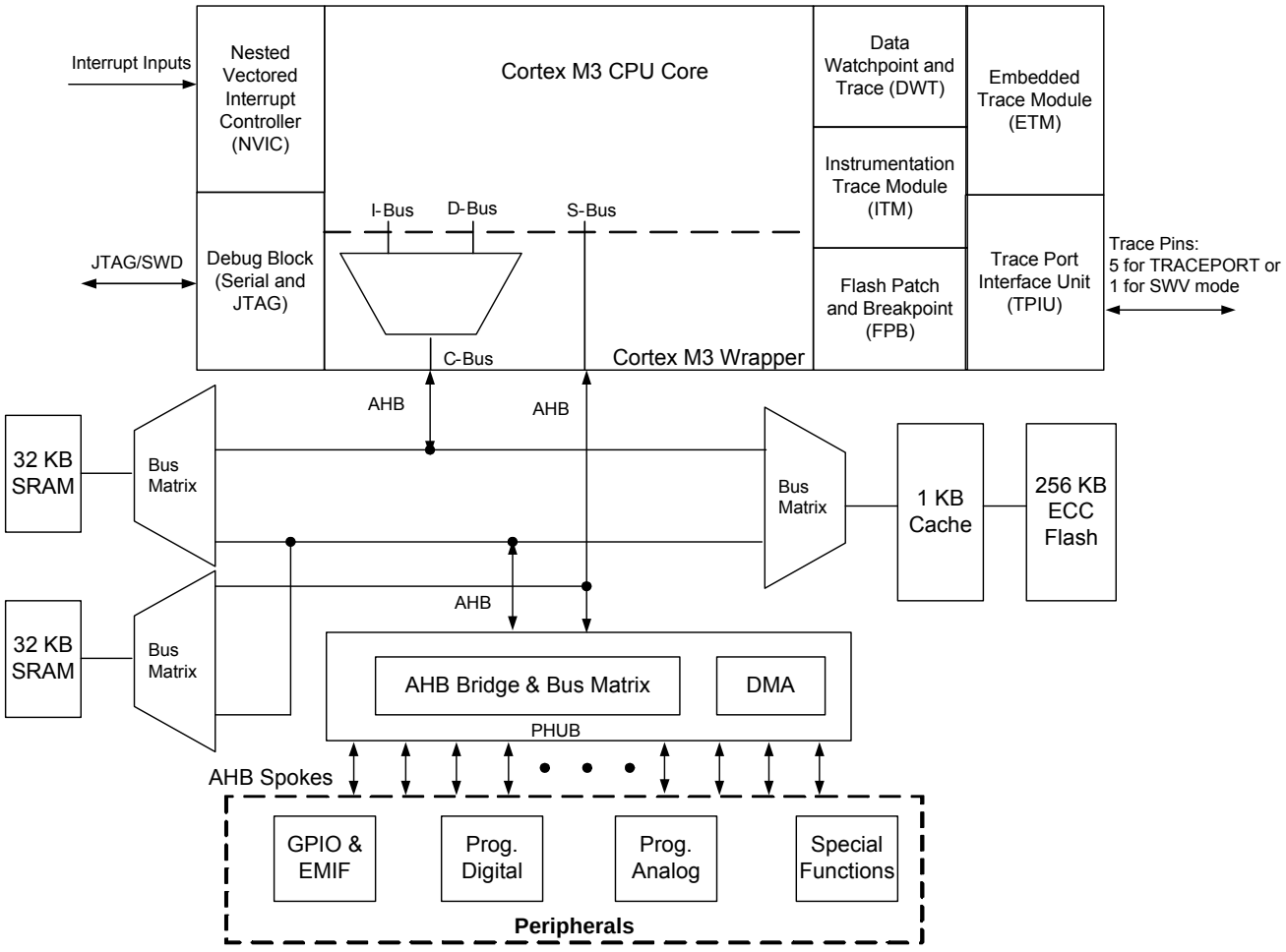
USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-. Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

VBOOST. Power sense connection to boost pump.

Note
6. GPIOs with opamp outputs are not recommended for use with CapSense

Figure 4-1. ARM Cortex-M3 Block Diagram



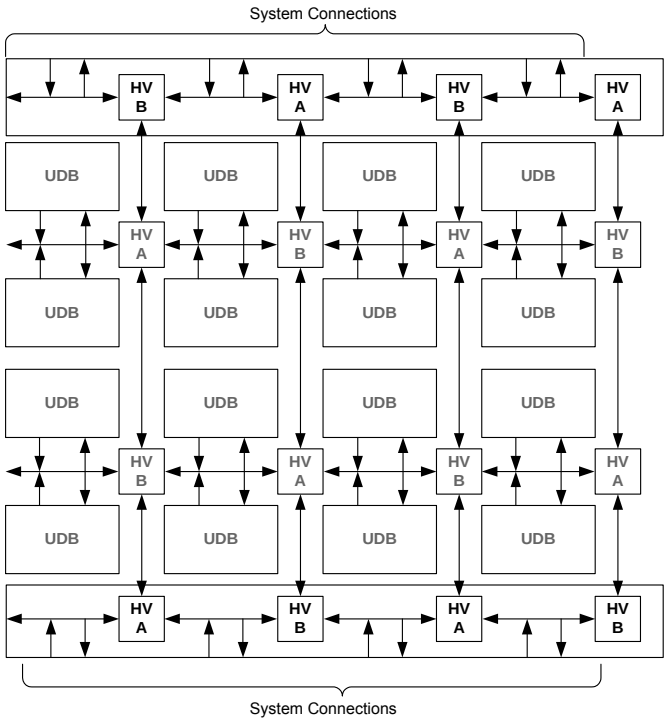
7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

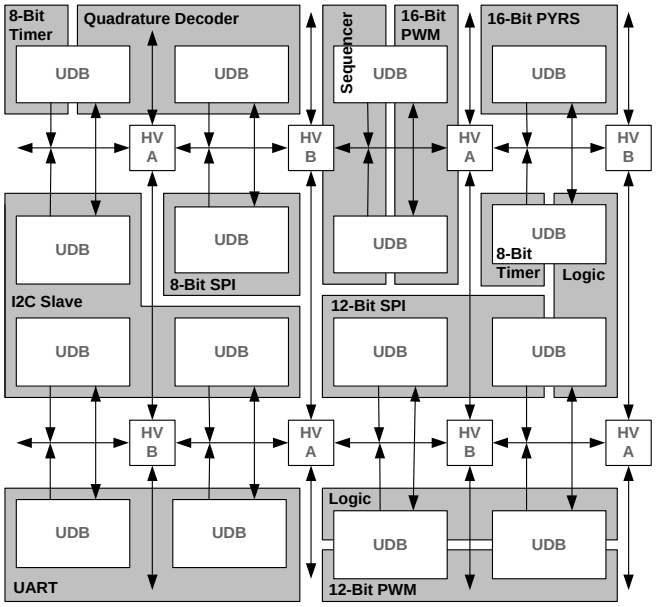


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The PSoC 5LP family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the PSoC 5LP family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in PSoC 5LP, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in PSoC 5LP, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

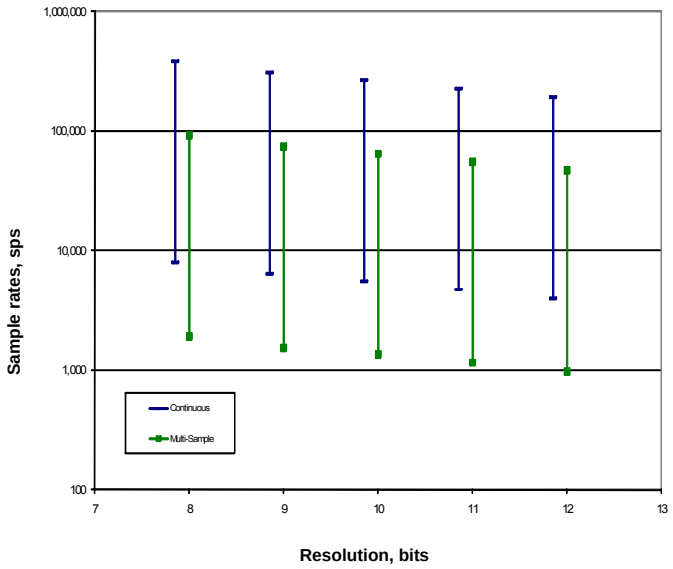
8.2 Delta-sigma ADC

Some CY8C36 devices offer a delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

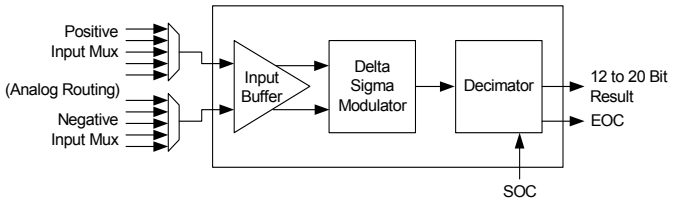
Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

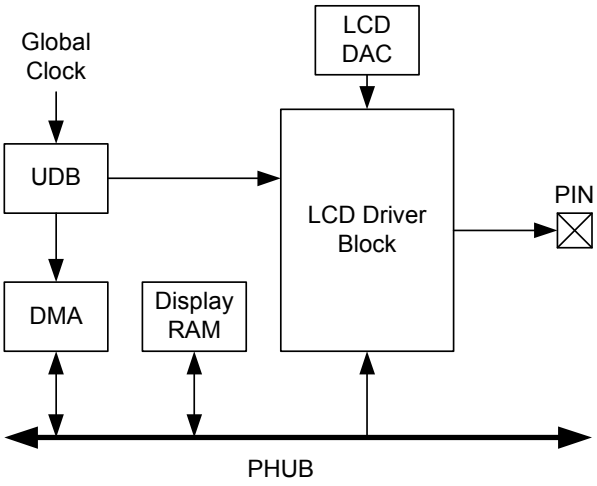
Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane x 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-11. LCD System



8.7.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.7.2 Display Data Flow

The LCD segment driver system reads display data and generates proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.7.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.7.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.8 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, and so on. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.9 Temp Sensor

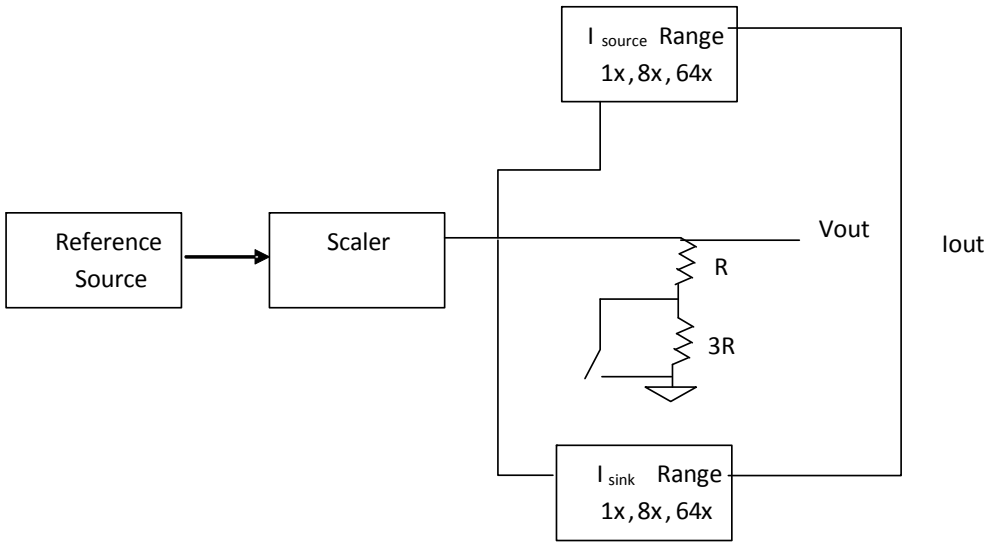
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.10 DAC

The CY8C54LP parts contain two Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.11 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-13. Mixer Configuration

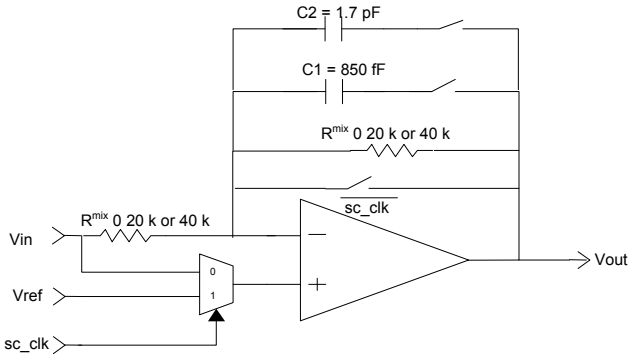


Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

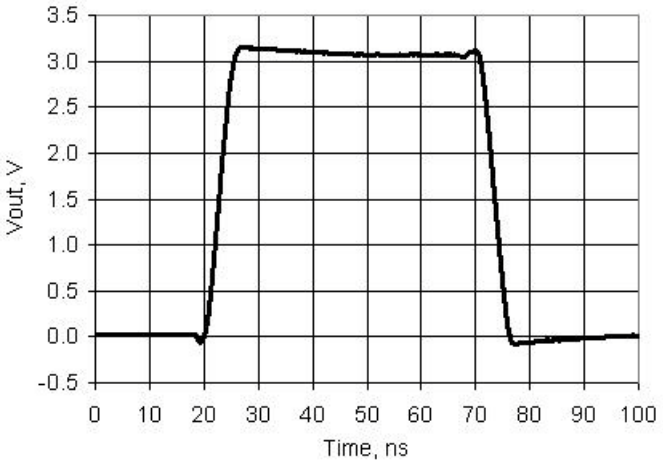


Table 11-15. USB Driver AC Specifications[38]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 103	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-16. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold		–	–	0.3 × V_{DDIO}	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[38]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[38]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-17. XRES AC Specifications[38]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

Note
38. Based on device characterization (Not production tested).

11.5.4 Analog Globals

Table 11-26. Analog Globals DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][48, 49]	V_{DDA} = 3.0 V	–	1500	2200	Ω
		V_{DDA} = 1.71 V	–	1200	1700	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][48, 49]	V_{DDA} = 3.0 V	–	700	1100	Ω
		V_{DDA} = 1.71 V	–	600	900	Ω

Table 11-27. Analog Globals AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Inter-pair crosstalk for analog routes[50]		106	–	–	dB
BWag	Analog globals 3 db bandwidth[50]	V_{DDA} = 3.0 V, 25 °C	–	26	–	MHz

11.5.5 Comparator

Table 11-28. Comparator DC Specifications[51]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, V_{DDA} > 2.7 V, Vin ≥ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, V_{IN} ≥ 0.5 V	–		9	mV
V_{OS}	Input offset voltage in fast mode[48]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[48]	Custom trim	–	–	4	mV
V_{OS}	Input offset voltage in ultra low power mode		–	±12	–	mV
TCVos	Temperature coefficient, input offset voltage	V_{CM} = V_{DDA} / 2, fast mode	–	63	85	µV/°C
		V_{CM} = V_{DDA} / 2, slow mode	–	15	20	
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 1.15	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[48]		–	–	400	µA
	Low current mode/slow mode[48]		–	–	100	µA
	Ultra low power mode[48]		–	6	–	µA

Table 11-29. Comparator AC Specifications[51]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[48]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[48]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low power mode[48]	50 mV overdrive, measured pin-to-pin	–	55	–	µs

Notes
48. Based on device characterization (Not production tested).
49. The resistance of the analog global and analog mux bus is high if V_{DDA} ≤ 2.7 V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.
50. Pin P6[4] to del-sig ADC input; calculated, not measured.
51. The recommended procedure for using a custom trim value for the on-chip comparators are found in the TRM.

11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 11 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-30. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, $V_{DDA} \geq 2.7$ V, Rload = 600 Ω	–	2.04	–	mA
		Range = 2.04 mA, High mode, code = 255, $V_{DDA} \leq 2.7$ V, Rload = 300 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±1	LSB
Eg	Gain error	Range = 2.04 mA	–	–	±2.5	%
		Range = 255 µA	–	–	±2.5	%
		Range = 31.875 µA	–	–	±3.5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.045	% / °C
		Range = 255 µA	–	–	0.045	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Sink mode, range = 255 µA, Codes 8–255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 µA, Codes 8–255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.6	LSB
		Source mode, range = 31.875 µA, Codes 8–255, Rload = 20 kΩ, Cload = 15 pF[52]	–	±0.9	±2	LSB
		Sink mode, range = 31.875 µA, Codes 8–255, Rload = 20 kΩ, Cload = 15 pF[52]	–	±0.9	±2	LSB
		Source mode, range = 2.04 mA, Codes 8–255, Rload = 600 Ω, Cload = 15 pF[52]	–	±0.9	±2	LSB
		Sink mode, range = 2.04 mA, Codes 8–255, Rload = 600 Ω, Cload = 15 pF[52]	–	±0.6	±1	LSB

Note
52. Based on device characterization (Not production tested).

Figure 11-40. IDAC INL vs Input Code, Range = 255 µA, Source Mode

Figure 11-41. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

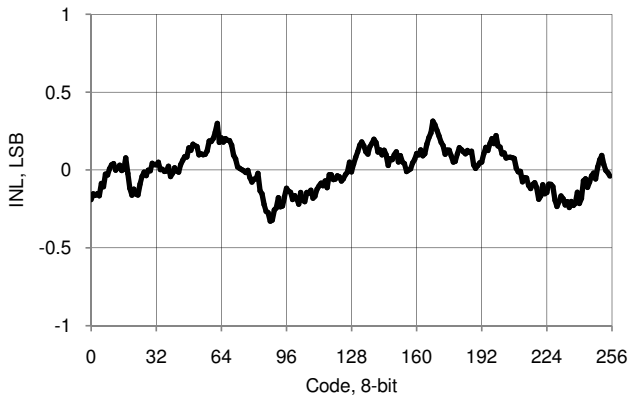


Figure 11-42. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

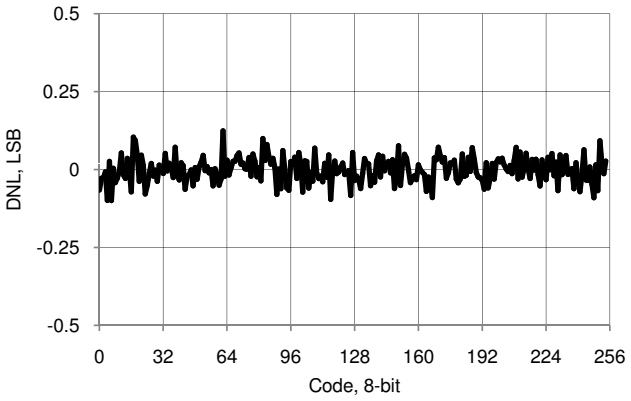


Figure 11-43. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

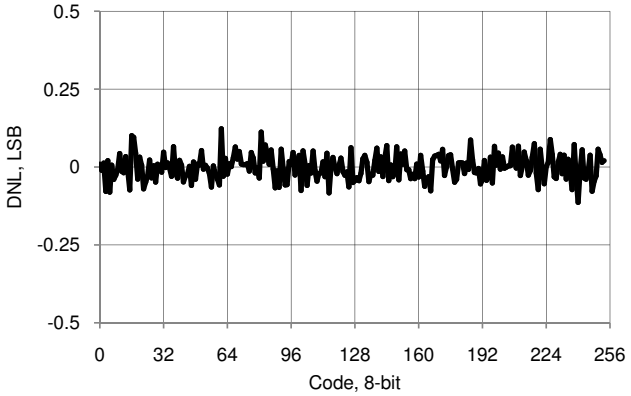


Figure 11-44. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

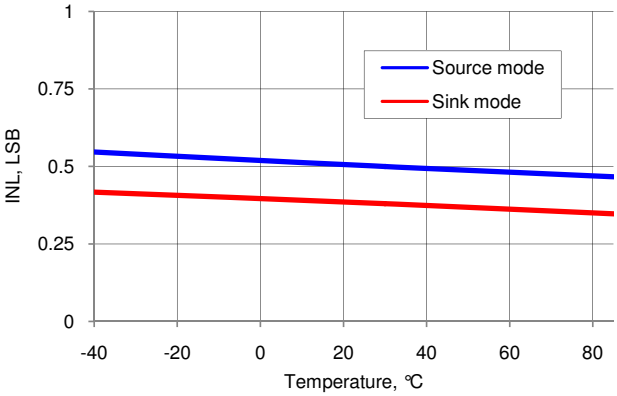


Figure 11-45. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode

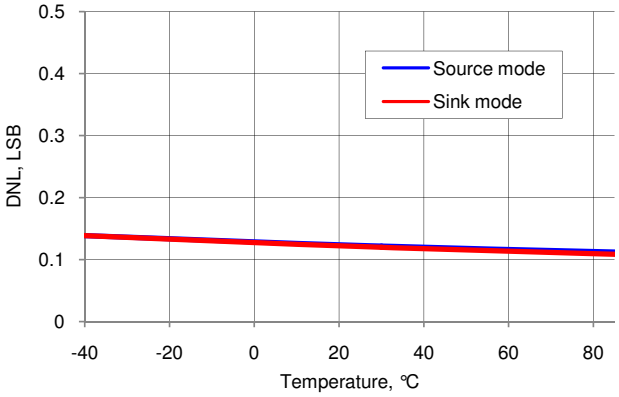


Figure 11-46. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

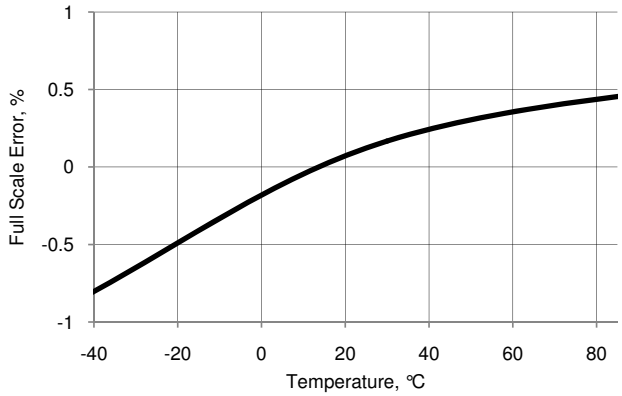


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

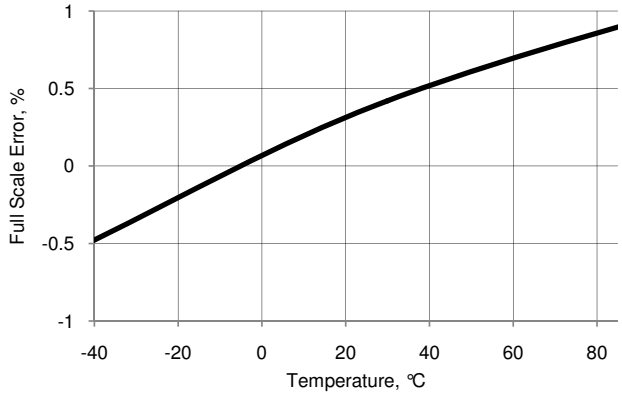


Figure 11-48. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

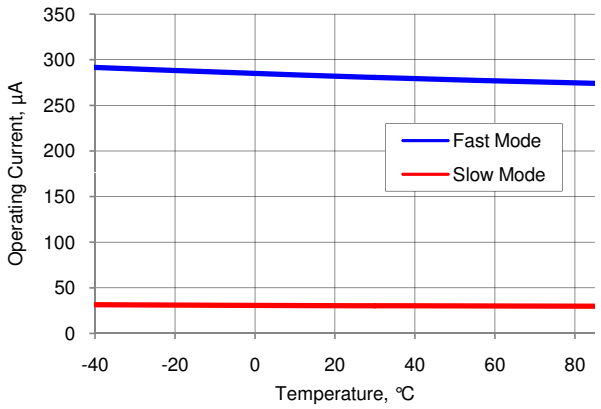


Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

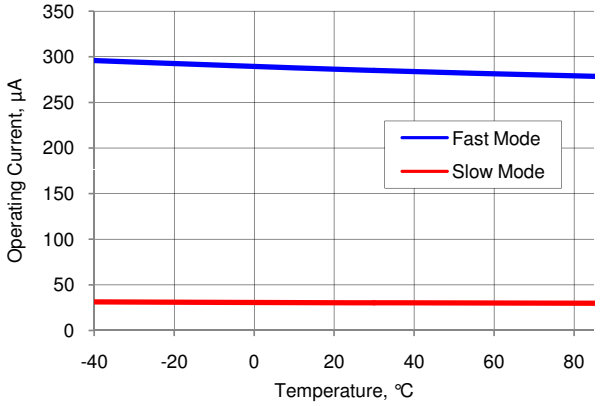


Table 11-31. IDAC AC Specifications[54]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
		Range = 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Note
54. Based on device characterization (Not production tested).

11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component datasheet in PSoC Creator for full electrical specifications and APIs.

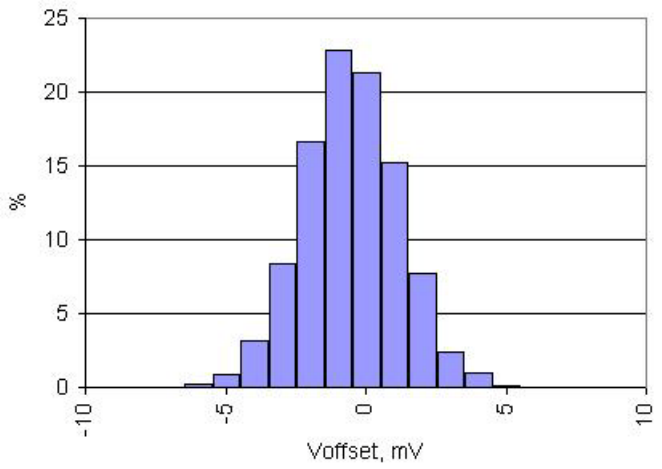
Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-38. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	V_{DDA}	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±0.15	%
Ge16	Gain error, gain = 16		–	–	±2.5	%
Ge50	Gain error, gain = 50		–	–	±5	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, $V_{DDA} \geq$ 2.7V, power mode = high	–	–	300	mV
IDD	Operating current[60]	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Figure 11-66. PGA Voffset Histogram, 4096 samples/ 1024 parts



Note
60. Based on device characterization (Not production tested).

Table 11-46. Counter AC Specifications[64]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	80.01	MHz
	Capture pulse[65]		15	–	–	ns
	Resolution[65]		15	–	–	ns
	Pulse width[65]		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width[65]		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width[65]		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component datasheet in PSoC Creator.

Table 11-47. PWM DC Specifications[64]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	80 MHz		–	360	–	µA

Table 11-48. PWM AC Specifications[64]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	80.01	MHz
	Pulse width[65]		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width[65]		15	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width[65]		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width[65]		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

Notes
64. Based on device characterization (Not production tested).
65. For correct operation, the minimum Timer/Counter/PWM input pulse width is the period of bus clock.

11.7.3 Nonvolatile Latches (NVL)

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1 K	–	–	Program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	Program/ erase cycles
	NVL data retention time	Average ambient temp. $T_A \le 55$ °C	20	–	–	Years
		Average ambient temp. $T_A \le 85$ °C	10	–	–	Years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage[70]		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	80.01	MHz

Note
70. Based on device characterization (Not production tested).

11.8.5 SWD Interface

Figure 11-73. SWD Interface Timing

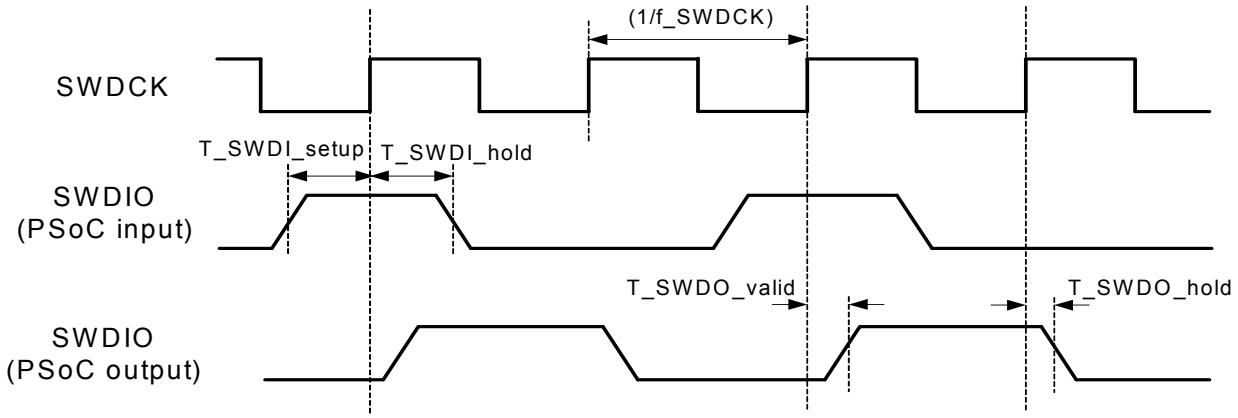


Table 11-69. SWD Interface AC Specifications[82]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[83]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[83]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5.5[83]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCK max	–	–	T/2	
T_SWDO_hold	SWDIO output hold after SWDCK high	T = 1/f_SWDCK max	1	–	–	ns

11.8.6 TPIU Interface

Table 11-70. TPIU Interface AC Specifications[82]

Parameter	Description	Conditions	Min	Typ	Max	Units
	TRACEPORT (TRACECLK) frequency		–	–	33[84]	MHz
	SWV bit rate		–	–	33[84]	Mbit

Notes
82. Based on device characterization (Not production tested).
83. f_SWDCK must also be no more than 1/3 CPU clock frequency.
84. TRACEPORT signal frequency and bit rate are limited by GPIO output frequency, see Table 11-9 on page 74.

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 Internal Main Oscillator

Table 11-71. IMO DC Specifications[85]

Parameter	Description	Conditions	Min	Typ	Max	Units
Icc_imo	Supply current					
	74.7 MHz		–	–	730	µA
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-74. IMO Current vs. Frequency

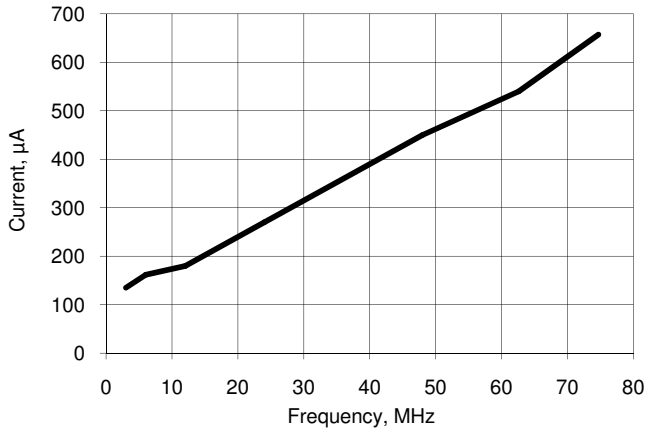
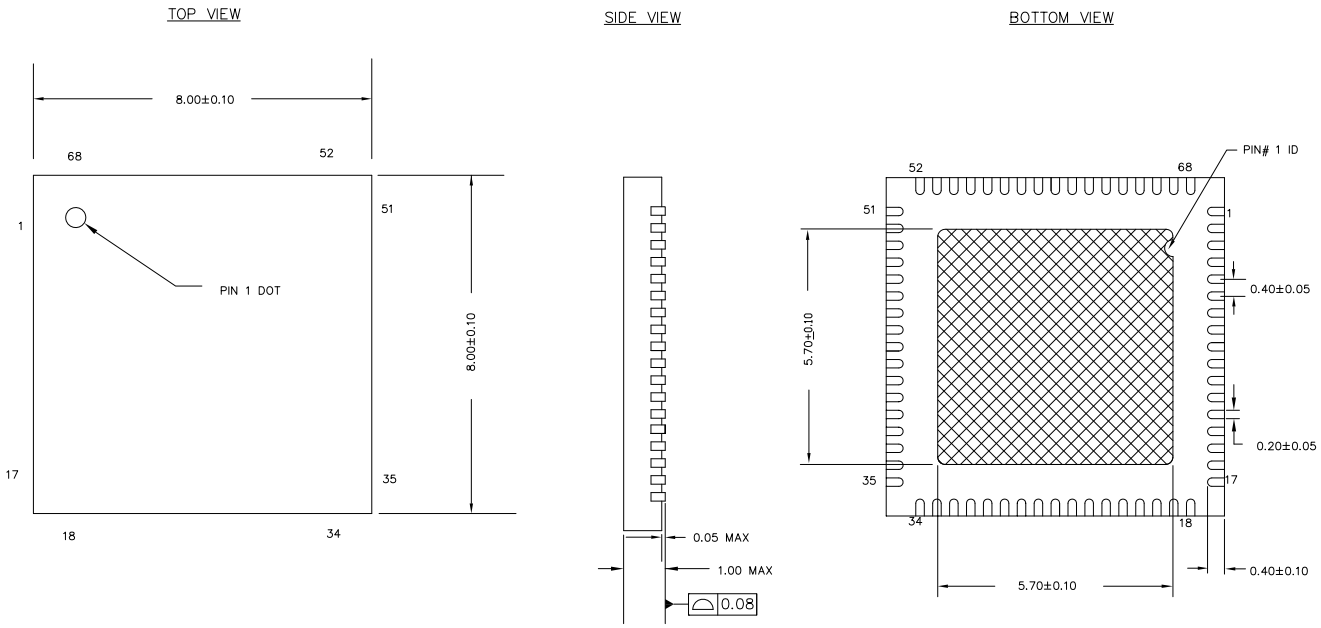


Table 11-72. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	74.7 MHz		–7	–	7	%
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz		–2	–	2	%
Tstart_imo	Startup time[85]	From enable (during normal system operation)	–	–	13	µs

Note
85. Based on device characterization (Not production tested).

Figure 13-1. 68-Pin QFN 8 × 8 with 0.4 mm Pitch Package Outline (Sawn Version)

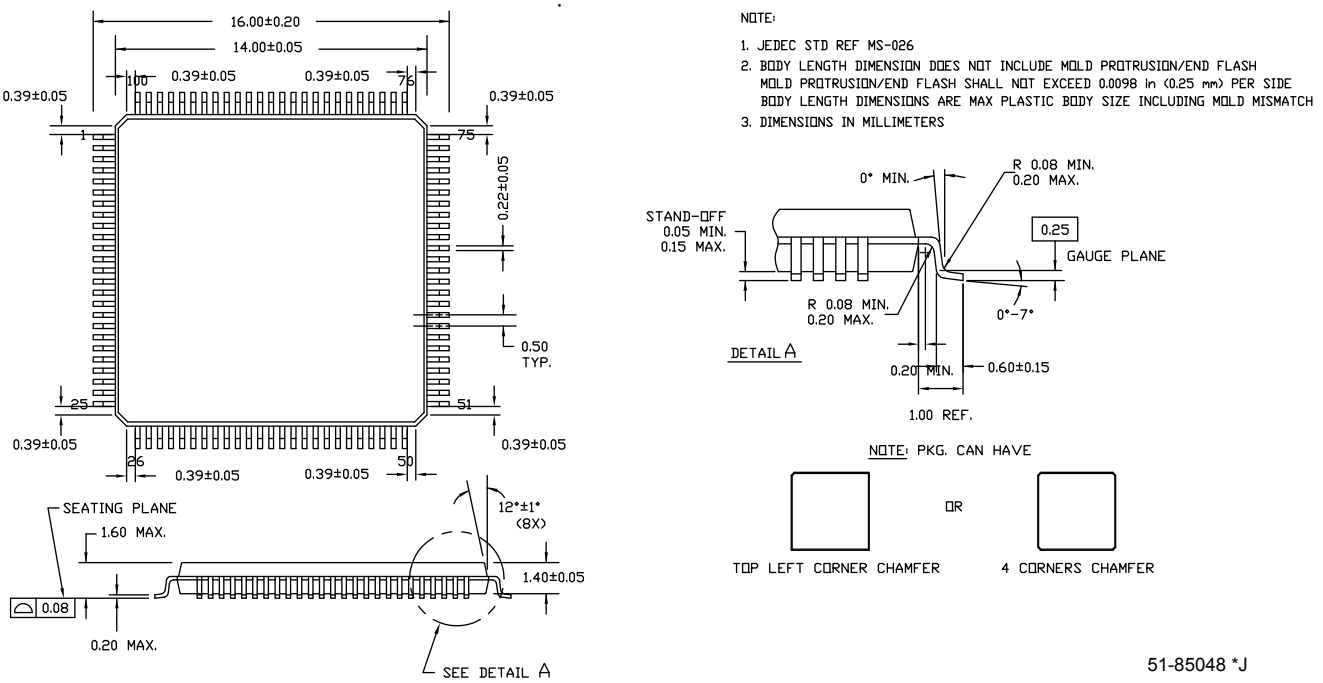


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 13-2. 100-Pin TQFP (14 × 14 × 1.4 mm) Package Outline



51-85048 *J