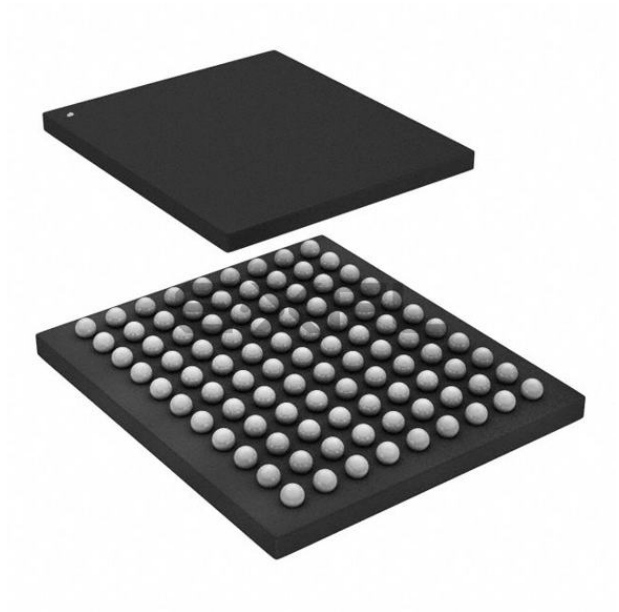
Infineon Technologies - CY8C5488FNI-LP212T Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	99-UFBGA, WLCSP
Supplier Device Package	99-WLCSP (5.19x5.94)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5488fni-lp212t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 5LP:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and code examples covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 5LP are:
  - AN77759: Getting Started With PSoC 5LP
  - AN77835: PSoC 3 to PSoC 5LP Migration Guide
  - AN61290: Hardware Design Considerations
  - AN57821: Mixed Signal Circuit Board Layout
  - AN58304: Pin Selection for Analog Designs
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
- Development Kits:
  - CY8CKIT-059 is a low-cost platform for prototyping, with a unique snap-away programmer and debugger on the USB connector.
  - CY8CKIT-050 is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - CY8CKIT-001 provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The MiniProg3 device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - Architecture TRM
  - Registers TRM
- Programming Specification

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator

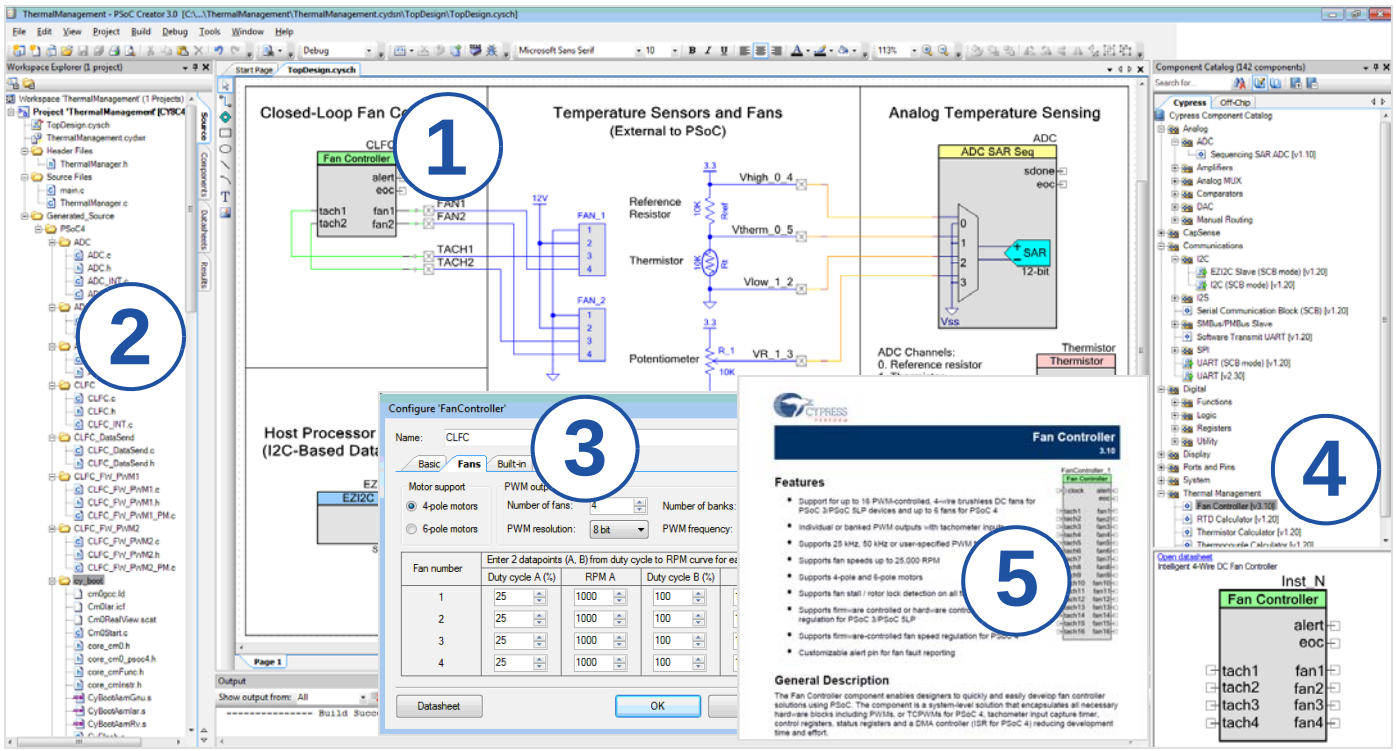


Table 2-2 shows the pinout for the 99-pin CSP package. Since there are four V_{DDIO} pins, the set of I/O pins associated with any V_{DDIO} may sink up to 100 mA total, same as for the 100-pin and 68-pin devices.

Table 2-2. CSP Pinout

Ball	Name	Ball	Name	Ball	Name	Ball	Name
E5	P2[5]	L2	VIO1	B2	P3[6]	C8	VIO0
G6	P2[6]	K2	P1[6]	B3	P3[7]	D7	P0[4]
G5	P2[7]	C9	P4[2]	C3	P12[0]	E7	P0[5]
H6	P12[4]	E8	P4[3]	C4	P12[1]	B9	P0[6]
K7	P12[5]	K1	P1[7]	E3	P15[2]	D8	P0[7]
L8	P6[4]	H2	P12[6]	E4	P15[3]	D9	P4[4]
J6	P6[5]	F4	P12[7]	A1	NC	F8	P4[5]
H5	P6[6]	J1	P5[4]	A9	NC	F7	P4[6]
J5	P6[7]	H1	P5[5]	L1	NC	E6	P4[7]
L7	VSSB	F3	P5[6]	L9	NC	E9	VCCD
K6	Ind	G1	P5[7]	A3	VCCA	F9	VSSD
L6	VBOOST	G2	P15[6]	A4	VSSA	G9	VDDD
K5	VBAT	F2	P15[7]	B7	VSSA	H9	P6[0]
L5	VSSD	E2	VDDD	B8	VSSA	G8	P6[1]
L4	XRES	F1	VSSD	C7	VSSA	H8	P6[2]
J4	P5[0]	E1	VCCD	A5	VDDA	J9	P6[3]
K4	P5[1]	D1	P15[0]	A6	VSSD	G7	P15[4]
K3	P5[2]	D2	P15[1]	B5	P12[2]	F6	P15[5]
L3	P5[3]	C1	P3[0]	A7	P12[3]	F5	P2[0]
H4	P1[0]	C2	P3[1]	C5	P4[0]	J7	P2[1]
J3	P1[1]	D3	P3[2]	D5	P4[1]	J8	P2[2]
H3	P1[2]	D4	P3[3]	B6	P0[0]	K9	P2[3]
J2	P1[3]	B4	P3[4]	C6	P0[1]	H7	P2[4]
G4	P1[4]	A2	P3[5]	A8	P0[2]	K8	VIO2
G3	P1[5]	B1	VIO3	D6	P0[3]		

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as the ADC. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

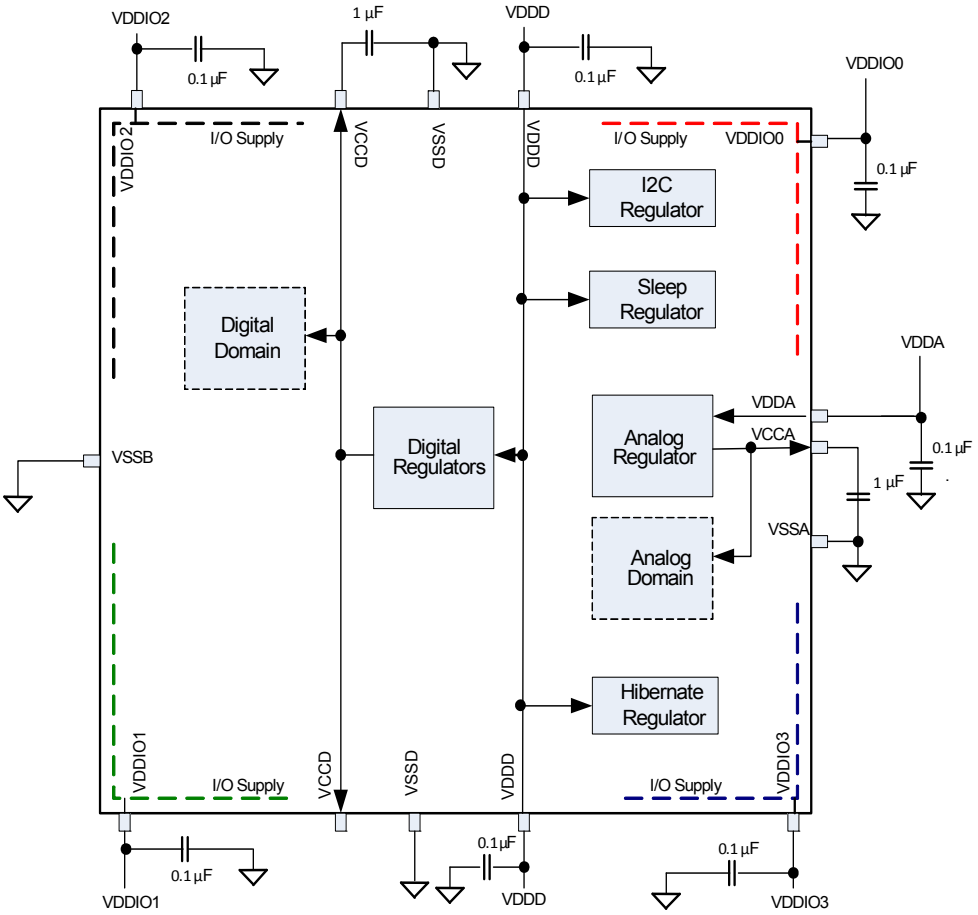
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (V_{CCD}) and analog (V_{CCA}) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4. The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1 µF ±10% X5R capacitor. The power system also contains a sleep regulator, an I^2C regulator, and a hibernate regulator.

Figure 6-4. PSoC Power System



Notes

- The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.
- You can power the device in internally regulated mode, where the voltage applied to the V_{DDx} pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the V_{CCx} pins, and do not tie the V_{DDx} pins to the V_{CCx} pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the V_{CCD} and V_{CCA} pins. In this configuration, the V_{DDD} pins should be shorted to the V_{CCD} pins and the V_{DDA} pin should be shorted to the V_{CCA} pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (V_{DDX} or V_{CCX} in Figure 6-4) is a significant percentage of the rated working voltage.

6.2.1 Power Modes

PSoC 5LP devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low power and portable devices.

PSoC 5LP power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and Real Time Clock functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all VDDIO supplies are at valid voltage levels.

Table 6-2. Power Modes

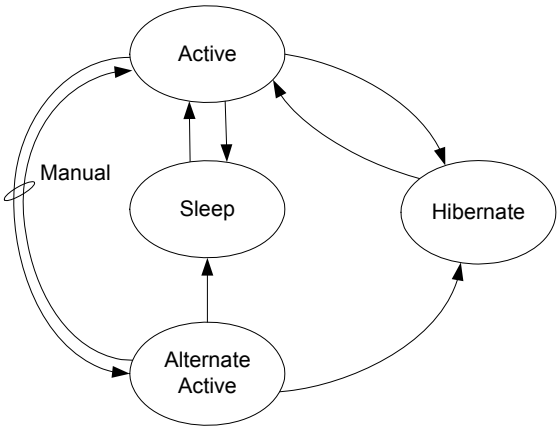
Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	3.1 mA[7]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<25 µs	2 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<200 µs	300 nA	No	None	None	None	PICU	XRES

Note
7. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See Table 11-2 on page 66.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 µs is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins; no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset pin (XRES), WDT, and Precision Reset (PRES).

6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar panels or single cell battery supplies, may use the on-chip boost converter to generate a minimum of 1.8 V supply voltage. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides such as driving 5.0 V LCD glass in a 3.3 V system. With the addition of an inductor, Schottky diode, and capacitors, it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage V_{BAT} from 0.5 V to 3.6 V, and can start up with V_{BAT} as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (V_{OUT}) in 100 mV increments. V_{BAT} is typically less than V_{OUT}; if V_{BAT} is greater than or equal to V_{OUT}, then V_{OUT} will be slightly less than V_{BAT} due to resistive losses in the boost converter. The block can deliver up to 50 mA (I_{BOOST}) depending on configuration to both the PSoC device and external components. The sum of all current sinks in the design including the PSoC device, PSoC I/O pin loads, and external component loads must be less than the I_{BOOST} specified maximum current.

Four pins are associated with the boost converter: V_{BAT}, V_{SSB}, V_{BOOST}, and IND. The boosted output voltage is sensed at the V_{BOOST} pin and must be connected directly to the chip's supply inputs; V_{DDA}, V_{DDD}, and V_{DDIO} if used to power the PSoC device.

The boost converter requires four components in addition to those required in a non-boost design, as shown in Figure 6-6 on page 30. A 22 µF capacitor (C_{BAT}) is required close to the V_{BAT} pin to provide local bulk storage of the battery voltage and provide regulator stability. A diode between the battery and V_{BAT} pin should not be used for reverse polarity protection because the diodes forward voltage drop reduces the V_{BAT} voltage. Between the V_{BAT} and IND pins, an inductor of 4.7 µH, 10 µH, or 22 µH is required. The inductor value can be optimized to increase the boost converter efficiency based on input voltage, output voltage, temperature, and current. Inductor size is determined by following the design guidance in this chapter and electrical specifications. The Inductor must be placed within 1 cm of the V_{BAT} and IND pins and have a minimum saturation current of 750 mA. Between the IND and V_{BOOST} pins a Schottky diode must be placed within 1 cm of the pins. The Schottky diode shall have a forward current rating of at least 1.0 A and a reverse voltage of at least 20 V. A 22 µF bulk capacitor (C_{BOOST}) must be connected close to V_{BOOST} to provide regulator output stability. It is important to sum the total capacitance connected to the V_{BOOST} pin and ensure the maximum C_{BOOST} specification is not exceeded. All capacitors must be rated for a minimum of 10 V to minimize capacitive losses due to voltage de-rating.

The switching frequency is set to 400 kHz using an oscillator integrated into the boost converter. The boost converter can be operated in two different modes: active and standby. Active mode is the normal mode of operation where the boost regulator actively generates a regulated output voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. Only minimal power is provided, typically < 5 µA to power the PSoC device in Sleep mode. The boost typically draws 250 µA in active mode and 25 µA in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize total power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

Table 6-4. Chip and Boost Power Modes Compatibility

Chip Power Modes	Boost Power Modes
Chip-active or alternate active mode	Boost must be operated in its active mode.
Chip-sleep mode	Boost can be operated in either active or standby mode. In boost standby mode, the chip must wake up periodically for boost active-mode refresh.
Chip-hibernate mode	Boost can be operated in its active mode. However, it is recommended not to use the boost in chip hibernate mode due to the higher current consumption in boost active mode.

6.2.2.1 Boost Firmware Requirements

To ensure boost inrush current is within specification at startup, the **Enable Fast IMO During Startup** value must be unchecked in the PSoC Creator IDE. The **Enable Fast IMO During Startup** option is found in PSoC Creator in the design wide resources (cydwr) file **System** tab. Un-checking this option configures the device to run at 12 MHz vs 48 MHz during startup while configuring the device. The slower clock speed results in reduced current draw through the boost circuit.

6.2.2.2 Boost Design Process

Correct operation of the boost converter requires specific component values determined for each designs unique operating conditions. The C_{BAT} capacitor, Inductor, Schottky diode, and C_{BOOST} capacitor components are required with the values specified in the electrical specifications, Table 11-7 on page 71. The only variable component value is the inductor L_{BOOST} which is primarily sized for correct operation of the boost across operating conditions and secondarily for efficiency. Additional operating region constraints exist for V_{OUT}, V_{BAT}, I_{OUT}, and T_A.

The following steps must be followed to determine boost converter operating parameters and L_{BOOST} value.

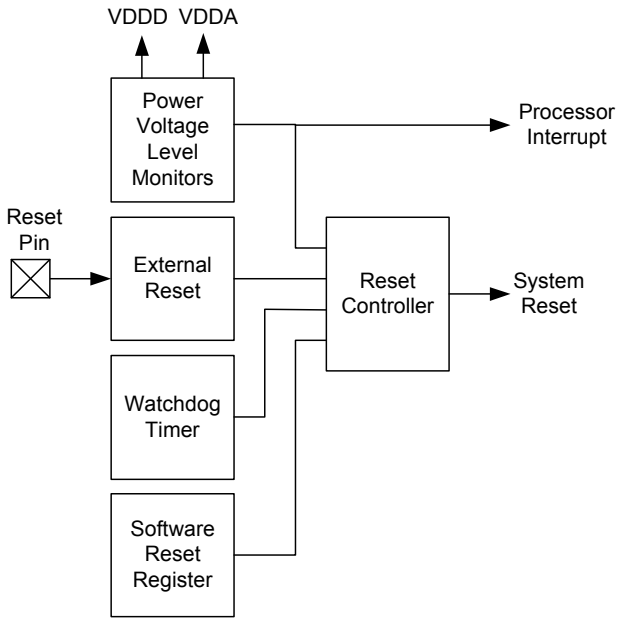
1. Choose desired V_{BAT}, V_{OUT}, T_A, and I_{OUT} operating condition ranges for the application.
2. Determine if V_{BAT} and V_{OUT} ranges fit the boost operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 71. If the operating ranges are not met, modify the operating conditions or use an external boost regulator.
3. Determine if the desired ambient temperature (T_A) range fits the ambient temperature operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 71. If the temperature range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
4. Determine if the desired output current (I_{OUT}) range fits the output current operating range based on the **I_{OUT} range over V_{BAT} and V_{OUT}** chart, Figure 11-9 on page 71. If the output current range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
5. Find the allowed inductor values based on the **L_{BOOST} values over V_{BAT} and V_{OUT}** chart, Figure 11-10 on page 71.
6. Based on the allowed inductor values, inductor dimensions, inductor cost, boost efficiency, and V_{RIPPLE} choose the optimum inductor value for the system. Boost efficiency and V_{RIPPLE} typical values are provided in the **Efficiency vs V_{BAT}** and **V_{RIPPLE} vs V_{BAT}** charts, Figure 11-11 on page 72 through Figure 11-14 on page 72. In general, if high efficiency and low V_{RIPPLE} are most important, then the highest allowed inductor value should be used. If low inductor cost or small inductor size are most important, then one of the smaller allowed inductor values should be used. If the allowed inductor(s) efficiency, V_{RIPPLE}, cost or dimensions are not acceptable for the application than an external boost regulator should be used.

6.3 Reset

CY8C54LP has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring - The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- External - The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer - A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- Software - The device can be reset under program control.

Figure 6-8. Resets



The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR - Initial Power-on-Reset

  At initial power on, IPOR monitors the power voltages V_{DDD}, V_{DDA}, V_{CCD} and V_{CCA}. The trip level is not precise. It is set to approximately 1 volt (0.75 V to 1.45 V). This is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES - Precise Low-Voltage Reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
ALVI	VDDA	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
AHVI	VDDA	1.71 V-5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES - External Reset

  PSoC 5LP has a dedicated XRES pin, which holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

- SRES - Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES - Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

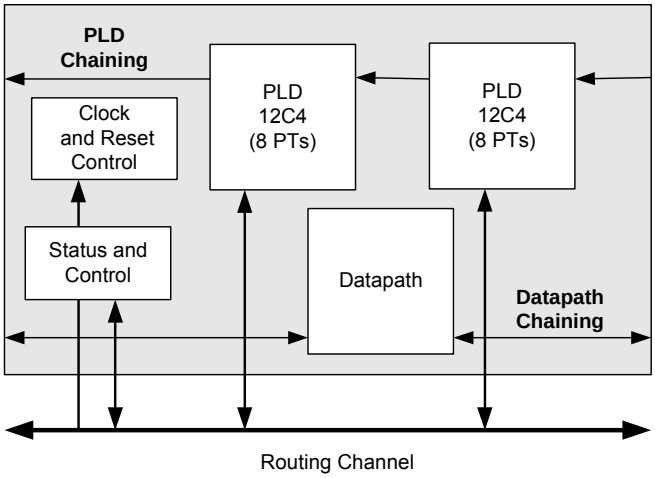
  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



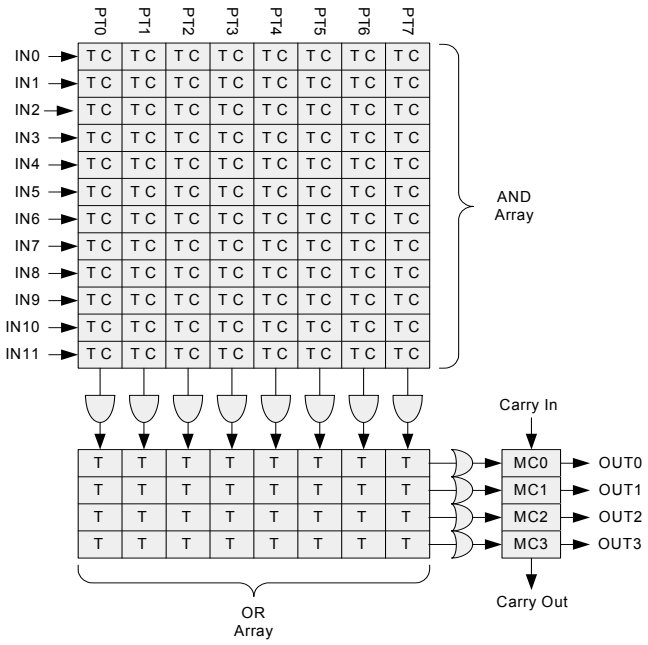
The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



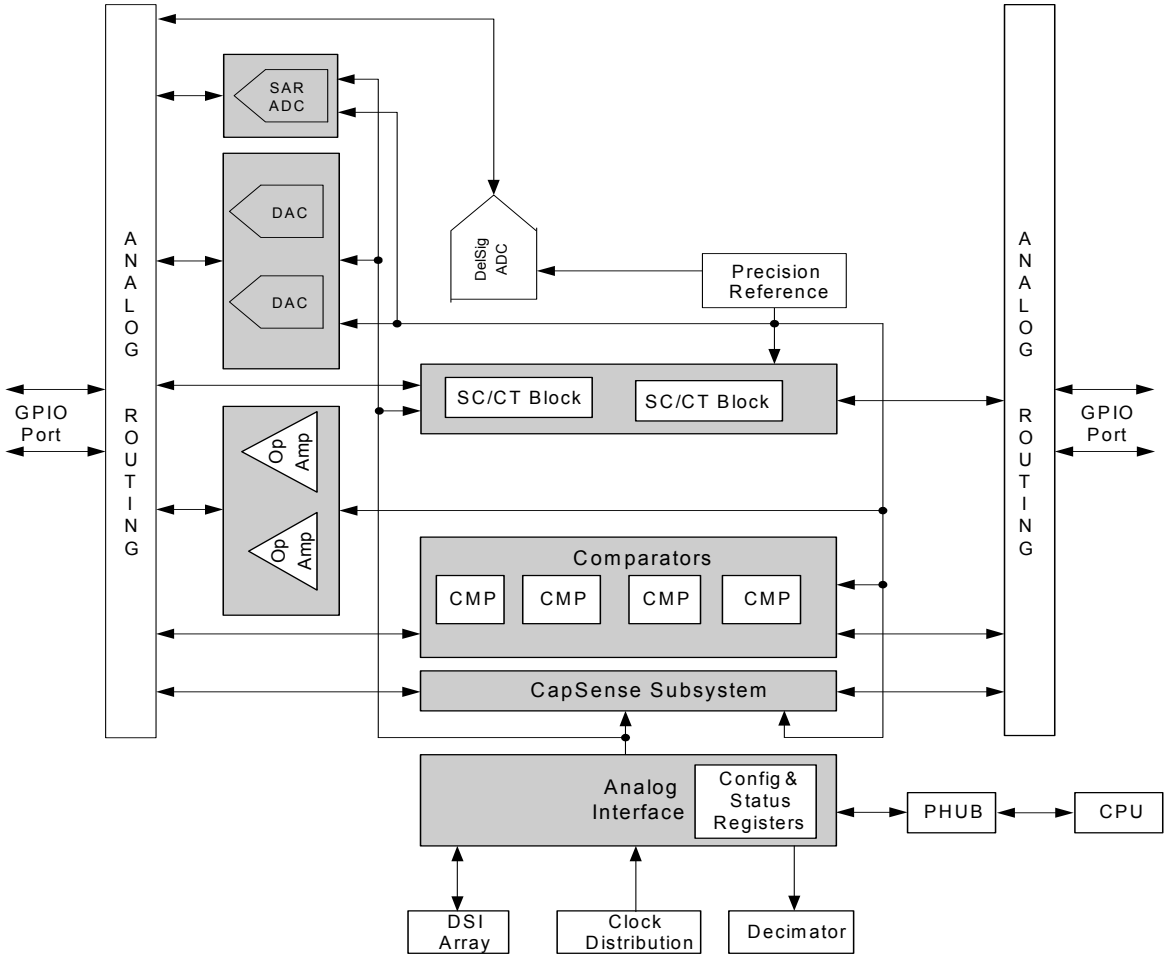
One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V 10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses
- High resolution Delta-Sigma ADC
- Successive approximation (SAR) ADC
- Two 8-bit DACs that provide either voltage or current output
- Four comparators with optional connection to configurable LUT outputs
- Two configurable switched capacitor/continuos time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer
- Two opamps for internal use and connection to GPIO that can be used as high current output buffers
- CapSense subsystem to enable capacitive touch sensing
- Precision reference for generating an accurate analog voltage for internal analog blocks

Figure 8-1. Analog Subsystem Block Diagram



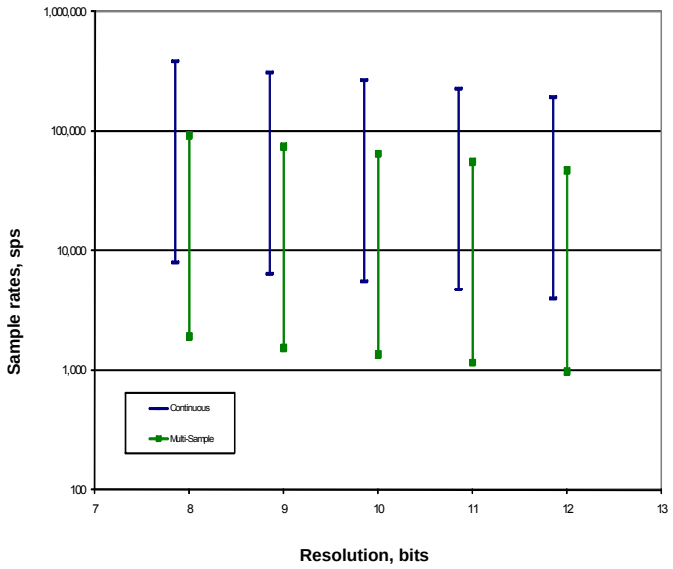
8.2 Delta-sigma ADC

Some CY8C36 devices offer a delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

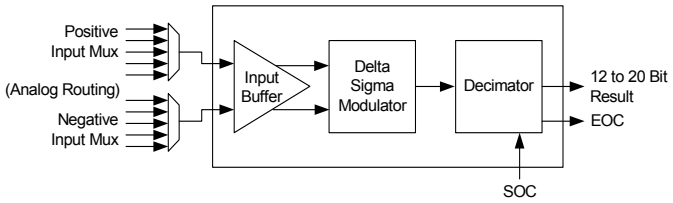
Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

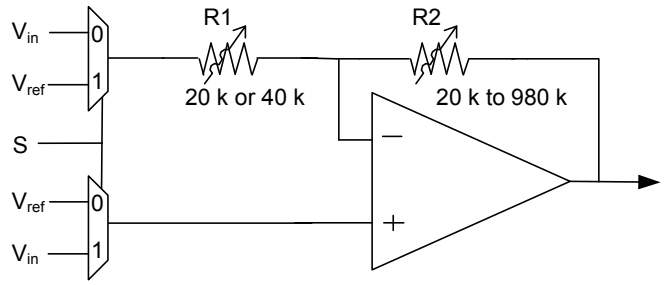
8.6.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

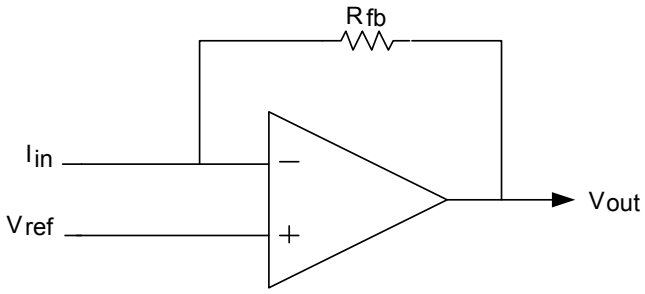
8.6.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.7 LCD Direct Drive

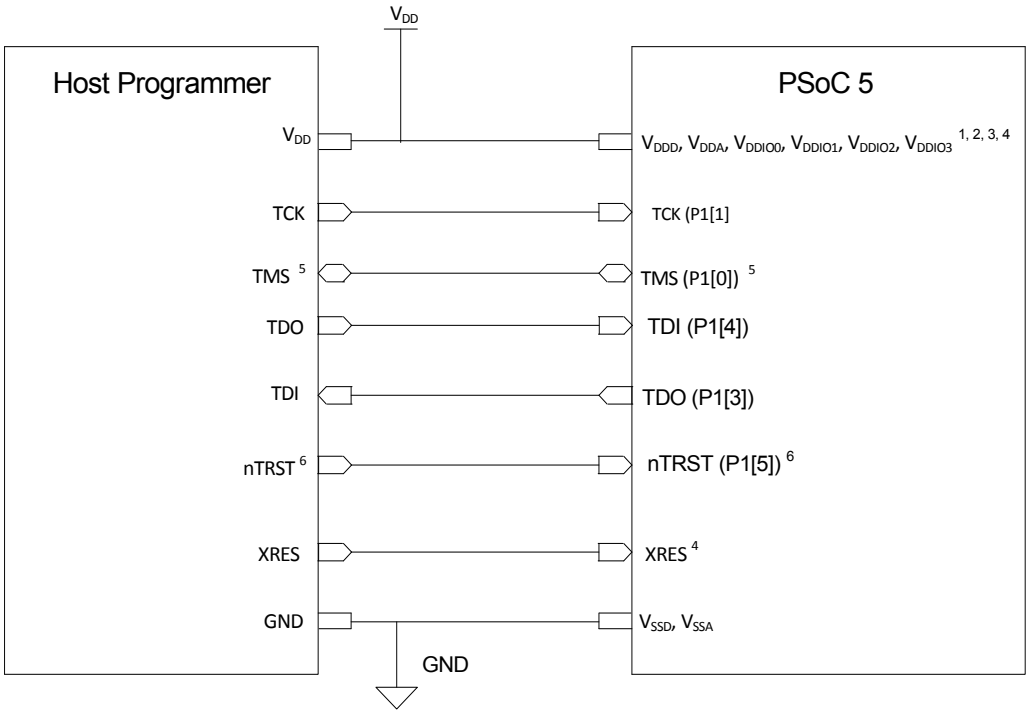
The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C54LP family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 12 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

Figure 9-1. JTAG Interface Connections between PSoC 5LP and Programmer



[1] The voltage levels of Host Programmer and the PSoC 5 voltage domains involved in Programming should be same. The Port 1 JTAG pins and XRES pin are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 5, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 5 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 5 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 5 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 27	0.9	1	1.1	µF

Figure 11-5. Analog and Digital Regulators, V_{CC} vs V_{DD}, 10 mA Load

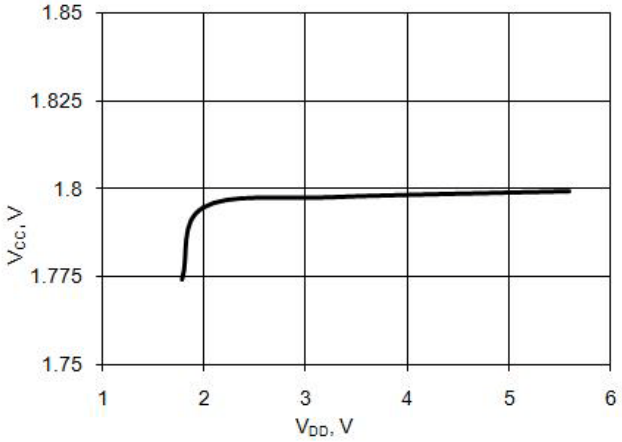
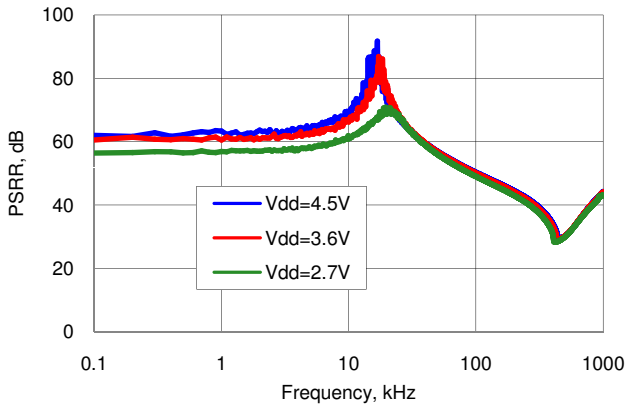


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}

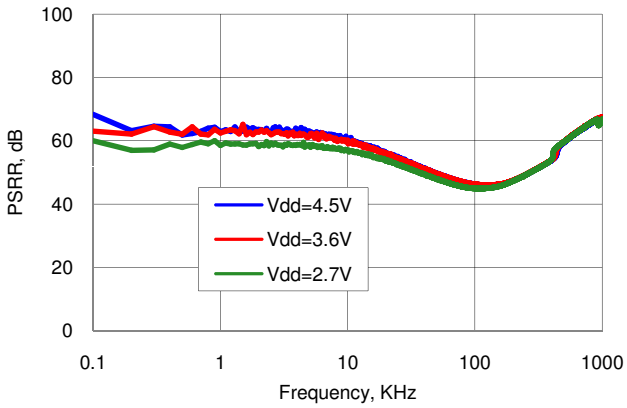


Figure 11-30. Opamp Noise vs Frequency, Power Mode = High, V_{DDA} = 5 V

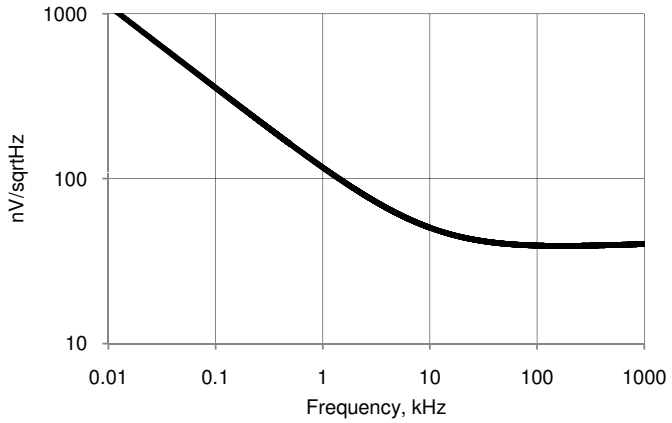


Figure 11-31. Opamp Step Response, Rising

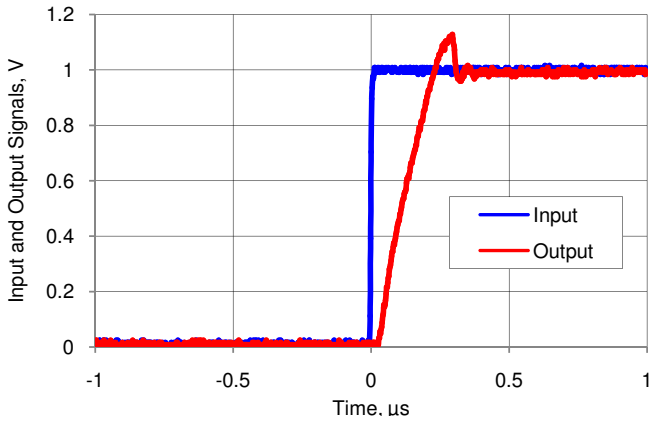


Figure 11-32. Opamp Step Response, Falling

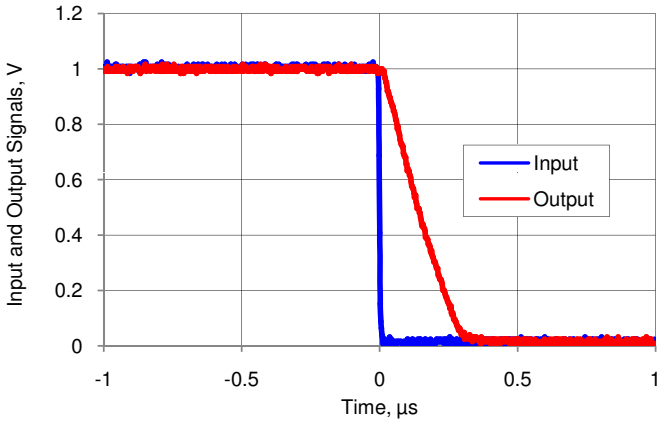


Figure 11-34. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

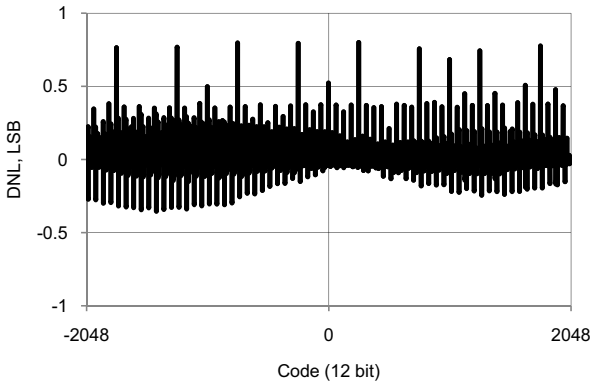


Figure 11-35. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode

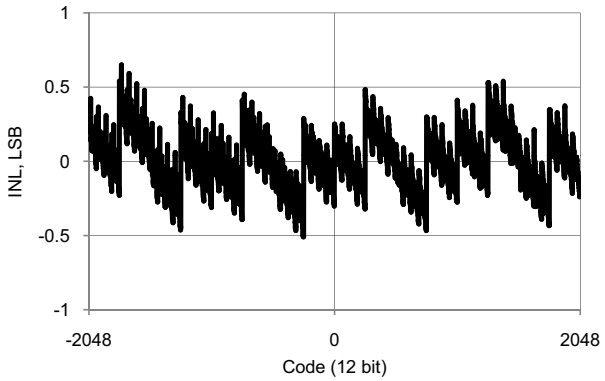


Figure 11-36. SAR ADC I_{DD} vs sps, V_{DDA} = 5 V, Continuous Sample Mode, External Reference Mode

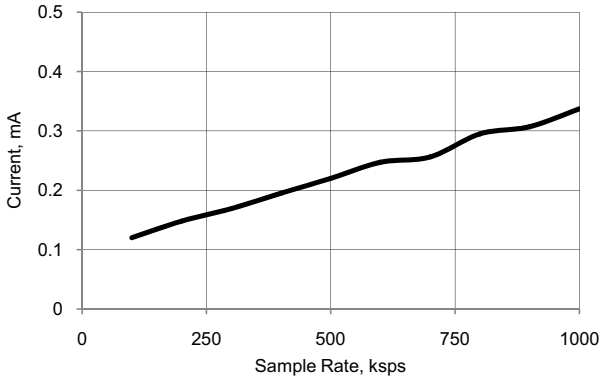


Table 11-25. SAR ADC AC Specifications[47]

Parameter	Description	Conditions	Min	Typ	Max	Units
A_SAMP_1	Sample rate with external reference bypass cap		–	–	1	Msps
A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}		–	–	500	Ksps
A_SAMP_3	Sample rate with no bypass cap. Internal reference		–	–	100	Ksps
	Startup time		–	–	10	µs
SINAD	Signal-to-noise ratio		68	–	–	dB
THD	Total harmonic distortion		–	–	0.02	%

Note
47. Based on device characterization (Not production tested).

Figure 11-37. SAR ADC Noise Histogram, 100 ksps, Internal Reference No Bypass

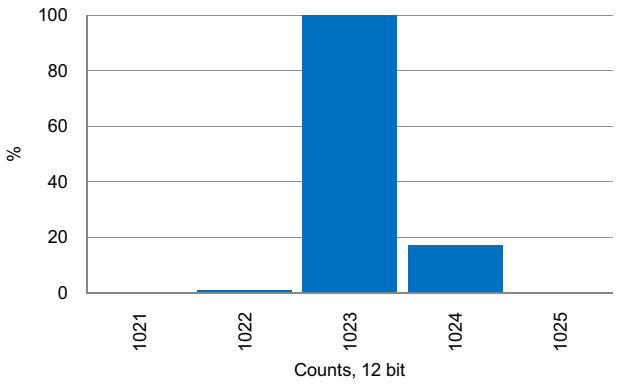


Figure 11-38. SAR ADC Noise Histogram, 1 msps, Internal Reference Bypassed

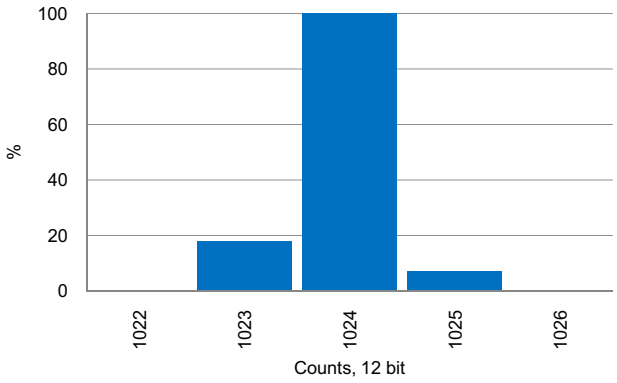


Figure 11-39. SAR ADC Noise Histogram, 1 msps, External Reference

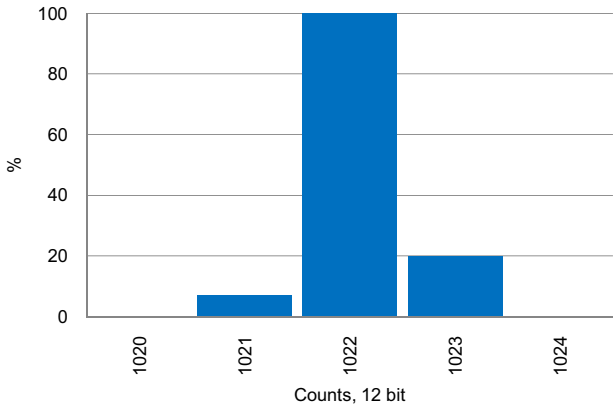


Figure 11-46. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

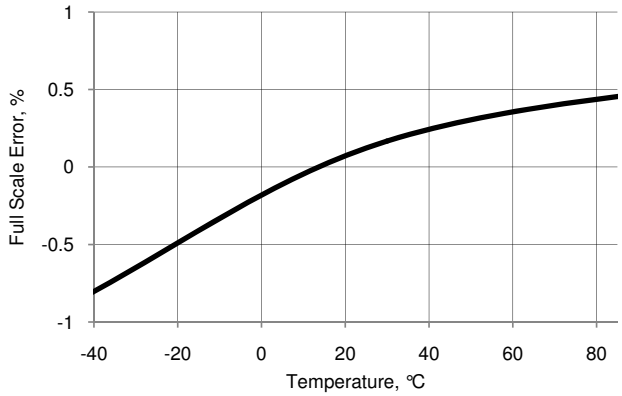


Figure 11-47. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

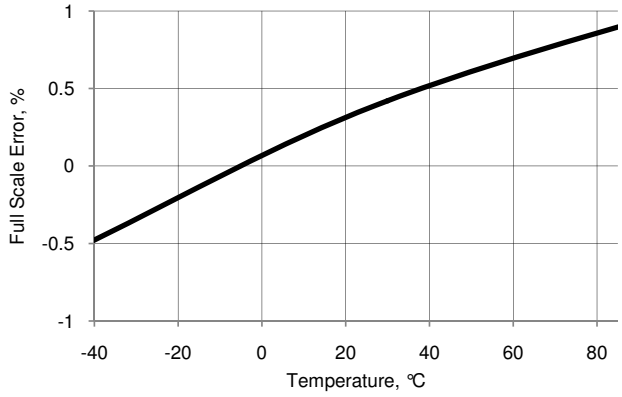


Figure 11-48. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

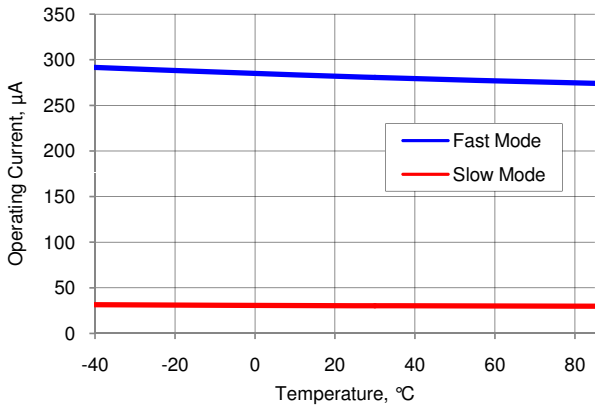


Figure 11-49. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

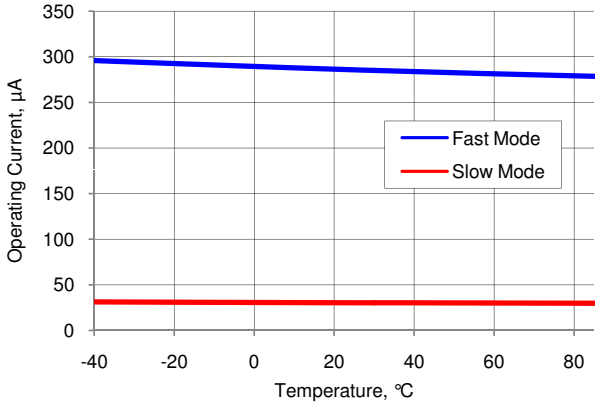


Table 11-31. IDAC AC Specifications[54]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
		Range = 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Note
54. Based on device characterization (Not production tested).

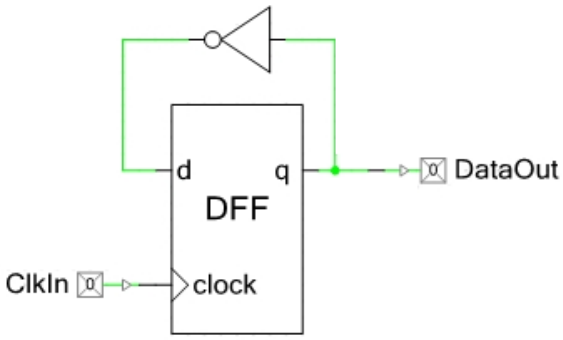
11.6.6 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-52. UDB AC Specifications[68]

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-69.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-69.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-69. Clock to Output Performance



Note
68. Based on device characterization (Not production tested).

Document History Page

Description Title: PSoC® 5LP: CY8C54LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84934				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3825653	MKEA	12/07/2012	Datasheet for new CY8C54LP family
*A	3897878	MKEA	02/07/2013	Removed Preliminary status. Updated characterization footnotes in Electrical Specifications. Updated conditions for SAR ADC INL and DNL specifications in Table 11-24 Updated Table 11-74 (ILO AC specifications). Changed “UDB Configuration" to "UDB Working Registers” in Table 5-5. Removed references to CAN. Updated INL VIDAC spec. Updated VREF accuracy. Removed drift specs from Voltage Reference Specifications.
*B	3902085	MKEA	02/12/2013	Changed Hibernate wakeup time from 125 µs to 200 µs in Table 6-3 and Table 11-3.
*C	4114902	MKEA	09/30/2013	Added information about 1 KB cache in Features. Updated SAR ADC graphs. Added warning on reset devices in the EEPROM section. Updated C_{IN} specs in GPIO DC Specifications and SIO DC Specifications. Added min and max values for the Regulator Output Capacitor parameter. Added I_{IB} parameter in Opamp DC Specifications
*D	4225729	MKEA	12/20/2013	Added SIO Comparator Specifications. Changed $T_{HIBERNATE}$ max value from 200 to 150. Updated CSP package and ordering information. Added 80 MHz parts in Table 12-1.
*E	4386988	MKEA	05/22/2014	Updated General Description and Features. Added More Information and PSoC Creator sections. Updated JTAG IDs in Ordering Information. Updated 100-TQFP package diagram.
*F	4587100	MKEA	12/08/2014	Added link to AN72845 in Note 4. Updated interrupt priority numbers in *Section 4.4*. Updated *Section 5.4* to clarify the factory default values of EEPROM. Corrected ECCEN settings in Table 5-3. Updated *Section 6.1.1* and *Section 6.1.2*. Added a note below Figure 6-4. Updated Figure 6-12. Changed ‘Control Store RAM’ to ‘Dynamic Configuration RAM’ in Figure 7-4 and changed *Section 7.2.2.2* heading to ‘Dynamic Configuration RAM’. Updated *Section 7.7*.