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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8543hxaqg

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NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

5 **RESET** Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of HRESET	100	—	μS	—
Minimum assertion time for SRESET	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before HRESET negation	100	—	μS	—
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs	1

Table 8. RESE1	Initialization	Timing	Specifications
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Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Мах	Unit
Core and platform PLL lock times	—	100	μS
Local bus PLL lock time	—	50	μS
PCI/PCI-X bus PLL lock time	—	50	μS

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements.

Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10.	Power	Supply	Ramp	Rate
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Parameter	Min	Мах	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	_	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.

2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, "PLL Power Supply Filtering," the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that $GV_{DD}(typ) = 2.5 \text{ V}$ for DDR SDRAM, and $GV_{DD}(typ) = 1.8 \text{ V}$ for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 \times GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	—
Output leakage current	I _{OZ}	-50	50	μΑ	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	—	mA	—
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 30	. TBI	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	_	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	_	—	ns
GTX_CLK rise (20%–80%)	t _{TTXR} ²		_	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} ²	_	_	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Ethernet Management Interface Electrical Characteristics

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum f_{MDC} = f_{CCB} ÷ 64 and minimum f_{MDC} = f_{CCB} ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram





Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

Local Bus



Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

14 GP_{OUT}/GP_{IN}

This section describes the DC and AC electrical specifications for the GP_{OUT}/GP_{IN} bus of the device.

14.1 GP_{OUT}/GP_{IN} Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP_{OUT} interface.

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level output voltage ($BV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	BV _{DD} – 0.2	_	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	_	0.2	V

 Table 47. GP_{OUT} DC Electrical Characteristics (3.3 V DC)

 Table 48. GP_{OUT} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level output voltage (BV _{DD} = min, I _{OH} = −1 mA)	V _{OH}	2.0	BV _{DD} + 0.3	V
Low-level output voltage (BV _{DD} min, I _{OL} = 1 mA)	V _{OL}	GND – 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP_{IN} interface.

Table 49. GP_{IN} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	—	±5	μΑ

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$, in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

High-Speed Serial Interfaces (HSSI)







Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

components are included in this requirement. The reference impedance for return loss measurements is $100-\Omega$ resistive for differential return loss and $25-\Omega$ resistive for common mode.

Characteristic	Symbol	Range		Unit	Notes	
onaraoteristic	Cymbol	Min	Мах	onit	Notes	
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver	
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver	
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver	
Multiple input skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit error rate	BER	_	10 ⁻¹²	—	—	
Unit interval	UI	800	800	ps	±100 ppm	

Table 66	. Receiver	AC	Timing	Specification	ns—1.25 GBaud
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Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notos	
Gharacteristic	Symbol	Min	Max	Unit	NOICS	
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver	
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver	
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver	
Multiple input skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit error rate	BER	—	10 ⁻¹²		_	
Unit interval	UI	400	400	ps	±100 ppm	

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	_
MRAS	L8	0	GV _{DD}	_
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	_
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	—
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	—
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
	Local Bus Controller Interface			•
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	_
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	0	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	ΒV _{DD}	
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1
LCS6/DMA_DACK2	G20	0	BV _{DD}	1
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9
LALE	H24	0	BV _{DD}	5, 8, 9
LBCTL	G27	0	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	_
LGPL5	E26	0	BV _{DD}	5, 9
LCKE	E24	0	BV _{DD}	_
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	I ² C interface			•
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
	SerDes			•
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—
SD_PLL_TPD	U28	0	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	3
SD_REF_CLK	T27	I	XV _{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	_	_	32
Reserved	M25, V27	—	_	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			·
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—
	System Control			
HRESET	AG17	I	OV _{DD}	_
HRESET_REQ	AG16	0	OV _{DD}	29
SRESET	AG20	I	OV _{DD}	
CKSTP_IN	AA9	I	OV _{DD}	—
CKSTP_OUT	AA8	0	OV _{DD}	2, 4
	Debug			
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29
MDVAL	AE5	0	OV _{DD}	6
CLK_OUT	AE21	0	OV _{DD}	11

Package Description

Table 72	. MPC8547E	Pinout	Listing ((continued)
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Signal	Signal Package Pin Number		Power Supply	Notes
	Local Bus Controller Interface		I	
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	_
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	0	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	—
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1
LCS6/DMA_DACK2	G20	0	BV _{DD}	1
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9
LALE	H24	0	BV _{DD}	5, 8, 9
LBCTL	G27	0	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—
LGPL5	E26	0	BV _{DD}	5, 9
LCKE	E24	0	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	0	BV _{DD}	_
	DMA		l	1
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 107
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	
	Programmable Interrupt Controller			
UDE	AH16	I	OV _{DD}	_
MCP	AG19	I	OV _{DD}	—

Table 72.	MPC8547E	Pinout Listing	(continued)
		i mout Listing	(continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DFT			
L1_TSTCLK	AC25	I	OV _{DD}	25
L2_TSTCLK	AE22	I	OV _{DD}	25
LSSD_MODE	AH20	I	OV _{DD}	25
TEST_SEL	AH14	I	OV _{DD}	25
	Thermal Management			
THERMO	AG1			14
THERM1	AH1			14
	Power Management			
ASLEEP	AH18	0	OV_{DD}	9, 19, 29
	Power and Ground Signals			
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 	_	_	_
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}	

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)	•	•
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	T7	0	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4			105

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
LSYNC_IN	F27	I	BV _{DD}	—			
LSYNC_OUT	F28	0	BV _{DD}	—			
	DMA		I				
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 108			
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	_			
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	_			
	Programmable Interrupt Controller		I				
UDE	AH16	I	OV _{DD}	_			
MCP	AG19	I	OV _{DD}	_			
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	Ι	OV _{DD}	—			
IRQ[8]	AF19	I	OV _{DD}	—			
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1			
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1			
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1			
IRQ_OUT	AD18	0	OV _{DD}	2, 4			
	Ethernet Management Interface						
EC_MDC	AB9	0	OV _{DD}	5, 9			
EC_MDIO	AC8	I/O	OV _{DD}	—			
Gigabit Reference Clock							
EC_GTX_CLK125	V11	I	LV _{DD}	—			
	Three-Speed Ethernet Controller (Gigabit Ether	rnet 1)					
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—			
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9			
TSEC1_COL	R4	I	LV _{DD}	—			
TSEC1_CRS	V5	I/O	LV _{DD}	20			
TSEC1_GTX_CLK	U7	0	LV _{DD}	—			
TSEC1_RX_CLK	U3	I	LV _{DD}	—			
TSEC1_RX_DV	V2	I	LV _{DD}	—			
TSEC1_RX_ER	T1	I	LV _{DD}	_			
TSEC1_TX_CLK	Т6	I	LV _{DD}	—			
TSEC1_TX_EN	U9	0	LV _{DD}	30			
TSEC1_TX_ER	Τ7	0	LV _{DD}	—			
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103			

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1		_	104
Reserved	R6	—	_	104
Reserved	P6		_	15
Reserved	N4	—	_	105
FIFO1_RXC2	P5	I	LV _{DD}	104
Reserved	R1	—	_	104
Reserved	P10	—	_	105
FIFO1_TXC2	P7	0	LV _{DD}	15
cfg_dram_type1	R10	0	LV _{DD}	5, 9
Thr	ee-Speed Ethernet Controller (Gigabit I	Ethernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_
TSEC3_GTX_CLK	W8	0	TV _{DD}	_
TSEC3_RX_CLK	W2	I	TV _{DD}	_
TSEC3_RX_DV	W1	I	TV _{DD}	_
TSEC3_RX_ER	Y2	I	TV _{DD}	_
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	0	TV _{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	_
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV _{DD}	—
TSEC3_CRS	AA3	I/O	TV _{DD}	31
TSEC3_TX_ER	AB6	0	TV _{DD}	—
	DUART	1		
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	_
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	_
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	—
	I ² C interface	1 1		
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27

Table 74. MPC8543E Pinout Listing (continued)

System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout

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