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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545ehxang

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	9 (,		
Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	

Table 1. Absolute Maximum Ratings ¹ (continued)

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. The -0.3 to 2.75 V range is for DDR and -0.3 to 1.98 V range is for DDR2.
- 3. The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
- 4. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

	Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltag	e	V _{DD}	1.1 V ± 55 mV	V	
PLL supply voltage		AV _{DD}	1.1 V ± 55 mV	V	1
Core power supply	for SerDes transceivers	SV _{DD}	1.1 V ± 55 mV	V	
Pad power supply	for SerDes transceivers	XV _{DD}	1.1 V ± 55 mV	V	
DDR and DDR2 DI	RAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O voltage		LV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	_	4
PCI/PCI-X, DUART Ethernet MII mana	F, system control and power management, I ² C, gement, and JTAG I/O voltage	OV _{DD}	3.3 V ± 165 mV	V	3
Local bus I/O volta	ge	BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	
	PCI, DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	^t ciskew	-300 -365 -390	300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ± (T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}. DUART

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD})$	I _{IN}	-	±5	μA
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	_	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f _{CCB} /1,048,576	baud	1, 2
Maximum baud rate	f _{CCB} /16	baud	1, 2, 3
Oversample rate	16		1, 4

Notes:

1. Guaranteed by design.

2. f_{CCB} refers to the internal platform clock.

3. Actual attainable baud rate is limited by the latency of interrupt processing.

4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

A summary of the FIFO AC specifications appears in Table 24 and Table 25.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
TX_CLK, GTX_CLK clock period	t _{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t _{FITH} /t _{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}	—	_	250	ps
Rise time TX_CLK (20%–80%)	t _{FITR}	—	_	0.75	ns
Fall time TX_CLK (80%–20%)	t _{FITF}	—	_	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t _{FITDV}	2.0	_	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	_	3.0	ns

Table 24. FIFO Mode Transmit AC Timing Specification

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t _{FIRH} /t _{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t _{FIRJ}	—		250	ps
Rise time RX_CLK (20%-80%)	t _{FIRR}	—	_	0.75	ns
Fall time RX_CLK (80%–20%)	t _{FIRF}	—	_	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{FIRDX}	0.5			ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 4.5, "Platform to FIFO Restrictions."

Timing diagrams for FIFO appear in Figure 6 and Figure 7.



Figure 6. FIFO Transmit AC Timing Diagram

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t _{RMRR}	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMRF}	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



Figure 34 shows the AC timing diagram for the I^2C bus.



Figure 34. I²C Bus AC Timing Diagram

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	Ι _{ΙΗ}	—	10	μΑ

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$ in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	2
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.

2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCIn_CLK when it is configured for asynchronous mode.

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 18.2, "AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK"

16.2.4.1 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK are designed to work with a spread spectrum clock (+0% to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 47. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, "PCI Express"
- Section 18, "Serial RapidIO"

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
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Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	_	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

components are included in this requirement. The reference impedance for return loss measurements is $100-\Omega$ resistive for differential return loss and $25-\Omega$ resistive for common mode.

Characteristic	Symbol	Range		Unit	Notes
onaraoteristic	Cymbol	Min	Мах	onit	Notes
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	_	10 ⁻¹²	—	—
Unit interval	UI	800	800	ps	±100 ppm

Table 66	. Receiver	AC	Timing	Specification	ns—1.25 GBaud
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Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Range		Unit	Notos	
Gharacteristic	Symbol	Min	Max	Unit	NOICS
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10 ⁻¹²		—
Unit interval	UI	400	400	ps	±100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Package Description

Table 72	. MPC8547E	Pinout	Listing ((continued)
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Signal	Package Pin Number		Power Supply	Notes				
Local Bus Controller Interface								
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	_				
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—				
LA[27]	H21	0	BV _{DD}	5, 9				
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9				
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	—				
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1				
LCS6/DMA_DACK2	G20	0	BV _{DD}	1				
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1				
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9				
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9				
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9				
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9				
LALE	H24	0	BV _{DD}	5, 8, 9				
LBCTL	G27	0	BV _{DD}	5, 8, 9				
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9				
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9				
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9				
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9				
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—				
LGPL5	E26	0	BV _{DD}	5, 9				
LCKE	E24	0	BV _{DD}	—				
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—				
LSYNC_IN	F27	I	BV _{DD}	—				
LSYNC_OUT	F28	0	BV _{DD}	_				
	DMA		l	1				
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 107				
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—				
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}					
	Programmable Interrupt Controller							
UDE	AH16	I	OV _{DD}	_				
MCP	AG19	I	OV _{DD}	—				

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER	R10	0	LV _{DD}	5, 9, 33
Three	e-Speed Ethernet Controller (Gigabit Ethe	ernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_
TSEC3_GTX_CLK	W8	0	TV _{DD}	_
TSEC3_RX_CLK	W2	I	TV _{DD}	_
TSEC3_RX_DV	W1	I	TV _{DD}	_
TSEC3_RX_ER	Y2	I	TV _{DD}	_
TSEC3_TX_CLK	V10	I	TV _{DD}	_
TSEC3_TX_EN	V9	0	TV _{DD}	30
Three	-Speed Ethernet Controller (Gigabit Ethe	ernet 4)		
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1
TSEC4_GTX_CLK	AA5	0	TV _{DD}	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV _{DD}	1, 30
· · ·	DUART			
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	_
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	_
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	_
· · ·	I ² C Interface			
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
· · · · · ·	SerDes	·		
SD_RX[0:3]	M28, N26, P28, R26	I	XV _{DD}	_
SD_RX[0:3]	M27, N25, P27, R25	I	XV _{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	0	XV _{DD}	_
SD_TX[0:3]	M23, N21, P23, R21	0	XV _{DD}	—
Reserved	W26, Y28, AA26, AB28	—	_	40
Reserved	W25, Y27, AA25, AB27	—	-	40

Table 72. MPC8547E Pinout Listing (continued)

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			1	
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17	
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17	
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17	
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17	
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35	
PCI1_GNT0	AG5	I/O	OV _{DD}	—	
PCI1_IRDY	AF11	I/O	OV _{DD}	2	
PCI1_PAR	AD12	I/O	OV _{DD}	—	
PCI1_PERR	AC12	I/O	OV _{DD}	2	
PCI1_SERR	V13	I/O	OV _{DD}	2, 4	
PCI1_STOP	W12	I/O	OV _{DD}	2	
PCI1_TRDY	AG11	I/O	OV _{DD}	2	
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—	
PCI1_REQ0	AH3	I/O	OV _{DD}	—	
PCI1_CLK	AH26	I	OV _{DD}	39	
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2	

Table 73. MPC8545E Pinout Listing

Package Description

Signal	Signal Package Pin Number		Power Supply	Notes
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)	•	
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	T7	0	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103
GPOUT[0:5]	GPOUT[0:5] N9, N10, P8, N7, R9, N5		LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	POUT7 N6		LV _{DD}	—
Reserved	Reserved P1		—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4			105

Package Description

Table 73	. MPC8545E	Pinout Listing	(continued)
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Signal Package Pin Number		Pin Type	Power Supply	Notes	
<u>SD_TX</u> [0:3]	SD_TX[0:3] M23, N21, P23, R21		XV _{DD}	—	
Reserved	W26, Y28, AA26, AB28	—	—	40	
Reserved	W25, Y27, AA25, AB27	—	—	40	
Reserved	U20, V22, W20, Y22	_	—	15	
Reserved	U21, V23, W21, Y23	—	—	15	
SD_PLL_TPD	U28	0	XV _{DD}	24	
SD_REF_CLK	T28	I	XV _{DD}	—	
SD_REF_CLK	T27	I	XV _{DD}	—	
Reserved	AC1, AC3	—	—	2	
Reserved	M26, V28	—	—	32	
Reserved	M25, V27	—	—	34	
Reserved	M20, M21, T22, T23	—	—	38	
General-Purpose Output					
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—	
	System Control				
HRESET	AG17	I	OV _{DD}	—	
HRESET_REQ	AG16	0	OV _{DD}	29	
SRESET	AG20	I	OV _{DD}	—	
CKSTP_IN	AA9	I	OV _{DD}	—	
CKSTP_OUT	AA8	0	OV _{DD}	2, 4	
	Debug				
TRIG_IN	AB2	I	OV _{DD}	—	
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29	
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9	
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29	
MDVAL	MDVAL AE5		OV _{DD}	6	
CLK_OUT	AE21	0	OV _{DD}	11	
Clock					
RTC AF16		I	OV _{DD}	—	
SYSCLK	AH17	I	OV _{DD}	—	
JTAG					
ТСК	AG28	I	OV _{DD}	—	
TDI	AH28	I	OV _{DD}	12	

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV

These capacitors must have a value of 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a $1-\mu F$ ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA_DACK[0:1], and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.