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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545ehxaqg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Overview



Figure 1. Device Block Diagram

# 1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
  - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - 36-bit real addressing
  - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
  - Enhanced hardware and software debug support

#### DDR and DDR2 SDRAM

#### Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
MDQS epilogue end	t <sub>DDKHME</sub>	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state)</sub> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t<sub>DDKHAS</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t<sub>DDKLDX</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t<sub>DDKHMH</sub> follows the symbol conventions described in note 1. For example, t<sub>DDKHMH</sub> describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t<sub>DDKHMH</sub> can be modified through control of the MDQS override bits (called WR\_DATA\_DELAY) in the TIMING\_CFG\_2 register. This is typically set to the same delay as in DDR\_SDRAM\_CLK\_CNTL[CLK\_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8548E PowerQUICC III Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t<sub>DDKHMP</sub> follows the symbol conventions described in note 1.

#### NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 3 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t<sub>DDKHMH</sub>).



Figure 4 shows the DDR SDRAM output timing diagram.+



Figure 4. DDR SDRAM Output Timing Diagram

Figure 5 provides the AC test load for the DDR bus.



Figure 5. DDR AC Test Load

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV <sub>DD</sub> /TV <sub>DD</sub>	2.37	2.63	V	1, 2
Output high voltage ( $LV_{DD}/TV_{DD} = Min$ , $I_{OH} = -1.0 \text{ mA}$ )	V <sub>OH</sub>	2.00	LV <sub>DD</sub> /TV <sub>DD</sub> + 0.3	V	
Output low voltage ( $LV_{DD}/TV_{DD} = Min$ , I <sub>OL</sub> = 1.0 mA)	V <sub>OL</sub>	GND –0.3	0.40	V	
Input high voltage	V <sub>IH</sub>	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	
Input low voltage	V <sub>IL</sub>	-0.3	0.90	V	
Input high current ( $V_{IN} = LV_{DD}$ , $V_{IN} = TV_{DD}$ )	Ι <sub>ΙΗ</sub>	_	10	μΑ	1, 2, 3
Input low current (V <sub>IN</sub> = GND)	۱ <sub>IL</sub>	-15	_	μÂ	3

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Notes:

1.  $LV_{DD}$  supports eTSECs 1 and 2.

2.  $\mathsf{TV}_{\mathsf{DD}}$  supports eTSECs 3 and 4.

3. Note that the symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  and  $TV_{IN}$  symbols referenced in Table 1 and Table 2.

# 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*\_TX\_CLK, while the receive clock must be applied to pin TSEC*n*\_RX\_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*\_GTX\_CLK pin (while transmit data appears on TSEC*n*\_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*\_GTX\_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."



Figure 7. FIFO Receive AC Timing Diagram

### 8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 26.	GMII	Transmit	AC	Timing	<b>Specifications</b>
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t <sub>GTKHDV</sub>	2.5	_	_	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t <sub>GTKHDX</sub>	0.5	_	5.0	ns
GTX_CLK data clock rise time (20%–80%)	t <sub>GTXR</sub> <sup>2</sup>	_	_	1.0	ns
GTX_CLK data clock fall time (80%–20%)	t <sub>GTXF</sub> 2	—		1.0	ns

Notes:

The symbols used for timing specifications follow the pattern t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>GTKHDV</sub> symbolizes GMII transmit timing (GT) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t<sub>GTKHDX</sub> symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>GTX</sub> represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

#### Enhanced Three-Speed Ethernet (eTSEC)

Figure 10 shows the GMII receive AC timing diagram.



Figure 10. GMII Receive AC Timing Diagram

### 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

fable 2	28.	MII	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t <sub>MTX</sub> <sup>2</sup>	_	400	_	ns
TX_CLK clock period 100 Mbps	t <sub>MTX</sub>		40	_	ns
TX_CLK duty cycle	t <sub>MTXH/</sub> t <sub>MTX</sub>	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t <sub>MTKHDX</sub>	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t <sub>MTXR</sub> <sup>2</sup>	1.0	_	4.0	ns
TX_CLK data clock fall (80%–20%)	t <sub>MTXF</sub> <sup>2</sup>	1.0		4.0	ns

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>MTKHDX</sub> symbolizes MII transmit timing (MT) for the time t<sub>MTX</sub> clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t<sub>MTX</sub> represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

# **10.2 Local Bus AC Electrical Specifications**

This table describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	12	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.3	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.5	ns	5

#### Table 40. Local Bus Timing Parameters (BV<sub>DD</sub> = 3.3 V)—PLL Enabled

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

# 14 GP<sub>OUT</sub>/GP<sub>IN</sub>

This section describes the DC and AC electrical specifications for the GP<sub>OUT</sub>/GP<sub>IN</sub> bus of the device.

# 14.1 GP<sub>OUT</sub>/GP<sub>IN</sub> Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP<sub>OUT</sub> interface.

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV <sub>DD</sub>	3.13	3.47	V
High-level output voltage ( $BV_{DD} = min, I_{OH} = -2 mA$ )	V <sub>OH</sub>	BV <sub>DD</sub> – 0.2	_	V
Low-level output voltage (BV <sub>DD</sub> = min, I <sub>OL</sub> = 2 mA)	V <sub>OL</sub>	_	0.2	V

 Table 47. GP<sub>OUT</sub> DC Electrical Characteristics (3.3 V DC)

 Table 48. GP<sub>OUT</sub> DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV <sub>DD</sub>	2.37	2.63	V
High-level output voltage (BV <sub>DD</sub> = min, I <sub>OH</sub> = −1 mA)	V <sub>OH</sub>	2.0	BV <sub>DD</sub> + 0.3	V
Low-level output voltage (BV <sub>DD</sub> min, I <sub>OL</sub> = 1 mA)	V <sub>OL</sub>	GND – 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP<sub>IN</sub> interface.

Table 49. GP<sub>IN</sub> DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV <sub>DD</sub>	3.13	3.47	V
High-level input voltage	V <sub>IH</sub>	2	BV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current ( $BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$ )	I <sub>IN</sub>	—	±5	μΑ

Note:

1. The symbol  $\mathsf{BV}_{\mathsf{IN}}$ , in this case, represents the  $\mathsf{BV}_{\mathsf{IN}}$  symbol referenced in Table 1.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
L <sub>TX-SKEW</sub>	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

#### Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in Figure 49). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T<sub>RX-EYE</sub> = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T<sub>RX-EYE-MEDIAN-to-MAX-JITTER</sub> specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to  $-{300 \text{ mV}}$  and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50  $\Omega$  to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- $\Omega$  probes—see Figure 50). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

# 17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 50) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 49) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

# 18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and  $\overline{TD}$ ) or a receiver input (RD and  $\overline{RD}$ ). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD,  $\overline{\text{TD}}$ , RD, and  $\overline{\text{RD}}$  each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter,  $V_{OD}$ , is defined as  $V_{TD} V_{\overline{TD}}$ .
- 3. The differential input signal of the receiver,  $V_{ID}$ , is defined as  $V_{RD} V_{\overline{RD}}$ .
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is  $2 \times (A B)$  volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

# 18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

#### Serial RapidIO

Characteristic	Symbol	Rai	nge	Unit	Netas
Characteristic	Symbol	Min	Max	Onit	NOICES
Output voltage	V <sub>O</sub>	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V <sub>DIFFPP</sub>	800	1600	mVp-p	_
Deterministic jitter	J <sub>D</sub>	—	0.17	UI p-p	_
Total jitter	J <sub>T</sub>	—	0.35	UI p-p	_
Multiple output skew	S <sub>MO</sub>	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 63. Long Run Transmitter AC Timing Specifications—2.5 GBaud

#### Table 64. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notos
	Symbol	Min	Max	Onic	NOIES
Output voltage	V <sub>O</sub>	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V <sub>DIFFPP</sub>	800	1600	mVp-p	_
Deterministic jitter	J <sub>D</sub>	—	0.17	UI p-p	_
Total jitter	J <sub>T</sub>	—	0.35	UI p-p	_
Multiple output skew	S <sub>MO</sub>	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 52 with the parameters specified in Table 65 when measured at the output pins of the device and the device is driving a  $100-\Omega \pm 5\%$  differential resistive load. The output eye pattern of an LP-serial

This section details package parameters, pin assignments, and dimensions.

### **19.1 Package Parameters**

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are provided in Table 70.

Parameter	CBGA <sup>1</sup>	PBGA <sup>2</sup>
Package outline	29 mm × 29 mm	29 mm × 29 mm
Interconnects	783	783
Ball pitch	1 mm	1 mm
Ball diameter (typical)	0.6 mm	0.6 mm
Solder ball	63% Sn	63% Sn
	37% Pb	37% Pb
	0% Ag	0% Ag
Solder ball (lead-free)	95% Sn	96.5% Sn
	4.5% Ag	3.5% Ag
	0.5% Cu	

Table 70. Package Parameters

Notes:

1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

2. The FC-PBGA package is available on only versions 2.1.1 and 2.1.2, and 3.0 of the device.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	l	OV <sub>DD</sub>	—
				_
				_
				_
				_
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	—
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2
PCI1_FRAME	AE11	I/O	OV <sub>DD</sub>	2
PCI1_IDSEL	AG9	I	OV <sub>DD</sub>	—
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV <sub>DD</sub>	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV <sub>DD</sub>	2
PCI2_CLK	AE28	I	OV <sub>DD</sub>	39
PCI2_IRDY	AD26	I/O	OV <sub>DD</sub>	2
PCI2_PERR	AD25	I/O	OV <sub>DD</sub>	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	0	OV <sub>DD</sub>	5, 9, 35
PCI2_GNT0	AG25	I/O	OV <sub>DD</sub>	_
PCI2_SERR	AD24	I/O	OV <sub>DD</sub>	2, 4
PCI2_STOP	AF24	I/O	OV <sub>DD</sub>	2
PCI2_TRDY	AD27	I/O	OV <sub>DD</sub>	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV <sub>DD</sub>	—
PCI2_REQ0	AH25	I/O	OV <sub>DD</sub>	—
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV <sub>DD</sub>	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV <sub>DD</sub>	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV <sub>DD</sub>	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	_
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV <sub>DD</sub>	_
MBA[0:2]	F7, J7, M11	0	GV <sub>DD</sub>	_

### Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Thr	ee-Speed Ethernet Controller (Gigabit Ethe	rnet 2)		
TSEC2 RXDI7:01	P2. R2. N1. N2. P3. M2. M1. N3		LVpp	_
TSEC2 TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	0		5, 9, 33
	P1			
	R6			20
TSEC2 GTX CLK	P6	0		20
TSEC2 BX CLK	NA			
	P5			
TSEC2 BX ER	R1			
	P10			
	P7			20
	P10	0		5 0 22
13L02_1A_EN	RIU	rnot 2)	∟v DD	5, 9, 55
				5 0 00
		0		5, 9, 29
	¥1, VV3, VV5, VV4	1		
ISEC3_GIX_CLK	W8	0		
TSEC3_RX_CLK	W2		TV <sub>DD</sub>	—
TSEC3_RX_DV	W1		TV <sub>DD</sub>	
TSEC3_RX_ER	Y2		TV <sub>DD</sub>	—
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	—
TSEC3_TX_EN	V9	0	TV <sub>DD</sub>	30
Thr	ee-Speed Ethernet Controller (Gigabit Ethe	rnet 4)		
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV <sub>DD</sub>	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	1
TSEC4_GTX_CLK	AA5	0	TV <sub>DD</sub>	—
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV <sub>DD</sub>	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV <sub>DD</sub>	1, 30
· · · ·	DUART		•	•
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	—
UART_RTS[0:1]	AC6, AD7	0	OV <sub>DD</sub>	—
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	—
UART_SOUT[0:1]	AB7, AD8	0	OV <sub>DD</sub>	—

### Table 71. MPC8548E Pinout Listing (continued)

#### Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

#### NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)		1	
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV <sub>DD</sub>	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV <sub>DD</sub>	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV <sub>DD</sub>	5, 9, 35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	—
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	—
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2, 4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2
PCI1_TRDY	AG11	I/O	OV <sub>DD</sub>	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV <sub>DD</sub>	—
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	—
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2

#### Table 73. MPC8545E Pinout Listing

Table 73.	<b>MPC8545E</b>	Pinout	Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_TX[0:3]	M23, N21, P23, R21	0	XV <sub>DD</sub>	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	_	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	0	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	—
SD_REF_CLK	T27	I	XV <sub>DD</sub>	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			•
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV <sub>DD</sub>	—
	System Control			•
HRESET	AG17	I	OV <sub>DD</sub>	—
HRESET_REQ	AG16	0	OV <sub>DD</sub>	29
SRESET	AG20	I	OV <sub>DD</sub>	—
CKSTP_IN	AA9	I	OV <sub>DD</sub>	—
CKSTP_OUT	AA8	0	OV <sub>DD</sub>	2, 4
	Debug			
TRIG_IN	AB2	I	OV <sub>DD</sub>	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV <sub>DD</sub>	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV <sub>DD</sub>	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV <sub>DD</sub>	6, 19, 29
MDVAL	AE5	0	OV <sub>DD</sub>	6
CLK_OUT	AE21	0	OV <sub>DD</sub>	11
	Clock			
RTC	AF16	I	OV <sub>DD</sub>	—
SYSCLK	AH17	I	OV <sub>DD</sub>	_
	JTAG	•	•	·
ТСК	AG28	I	OV <sub>DD</sub>	-
TDI	AH28	I	OV <sub>DD</sub>	12

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4, 27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4, 27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4, 27
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV <sub>DD</sub>	—
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV <sub>DD</sub>	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV <sub>DD</sub>	—
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV <sub>DD</sub>	—
SD_PLL_TPD	U28	0	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	—
SD_REF_CLK	T27	I	XV <sub>DD</sub>	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	_	32
Reserved	M25, V27	_	_	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV <sub>DD</sub>	—
	System Control			
HRESET	AG17	I	OV <sub>DD</sub>	—
HRESET_REQ	AG16	0	OV <sub>DD</sub>	29
SRESET	AG20	I	OV <sub>DD</sub>	—
CKSTP_IN	AA9	I	OV <sub>DD</sub>	—
CKSTP_OUT	AA8	0	OV <sub>DD</sub>	2, 4
	Debug			
TRIG_IN	AB2	I	OV <sub>DD</sub>	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV <sub>DD</sub>	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV <sub>DD</sub>	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV <sub>DD</sub>	6, 19, 29
MDVAL	AE5	0	OV <sub>DD</sub>	6
CLK_OUT	AE21	0	OV <sub>DD</sub>	11
	Clock			
RTC	AF16	I	OV <sub>DD</sub>	
SYSCLK	AH17		OV <sub>DD</sub>	

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TV <sub>DD</sub>	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV <sub>DD</sub>	_
GV <sub>DD</sub>	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V,2.5 V)	GV <sub>DD</sub>	_
BV <sub>DD</sub>	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV <sub>DD</sub>	—
V <sub>DD</sub>	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V <sub>DD</sub>	_
SV <sub>DD</sub>	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV <sub>DD</sub>	_
XV <sub>DD</sub>	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV <sub>DD</sub>	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	Ι	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	_	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	_	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	0	V <sub>DD</sub>	13

### Table 74. MPC8543E Pinout Listing (continued)

#### System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

# 22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

# 22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system