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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545ehxatg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

## 8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	<b>AC</b> Timing	Specifications
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t <sub>TRX</sub>	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t <sub>SKTRX</sub>	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t <sub>TRXH</sub> /t <sub>TRX</sub>	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDVKH</sub>	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDXKH</sub>	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t <sub>TRXR</sub> <sup>2</sup>	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t <sub>TRXF</sub> <sup>2</sup>	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).</sub>

2. Guaranteed by design.

## **10.2 Local Bus AC Electrical Specifications**

This table describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	12	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.3	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.5	ns	5

### Table 40. Local Bus Timing Parameters (BV<sub>DD</sub> = 3.3 V)—PLL Enabled

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

## NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.



This table describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V with PLL disabled.

Table 42. Local Bus Timing	Parameters—PLL Bypassed
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Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	12	—	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
Internal launch/capture clock to LCLK delay	t <sub>lbkhkt</sub>	2.3	4.4	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	6.2	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKL2</sub>	6.1	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	-1.8	—	ns	4, 5

3.	The maximum t <sub>I2DXKL</sub>	has only to be met if the device does not stretch the LOW period $(t_{\text{I2CL}})$ of the SCL signal	al.

For the detail of I<sup>2</sup>C frequency calculation, see Determining the I<sup>2</sup>C Frequency Divider Ratio for SCL (AN2919). Note that the

200 MHz

390 kHz

0x26

512

133 MHz

346 kHz

0x00

384

#### 4. Guaranteed by design.

FDR bit setting

I<sup>2</sup>C source clock frequency

Actual FDR divider selected

Actual I<sup>2</sup>C SCL frequency generated

Figure 33 provides the AC test load for the  $I^2C$ .



Figure 33. I<sup>2</sup>C AC Test Load

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### Table 46. I<sup>2</sup>C AC Electrical Specifications (continued)

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	$0.2 \times OV_{DD}$	—	V	_

#### Notes:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>12DVKH</sub> symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>12SXKL</sub> symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t<sub>12C</sub> clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V<sub>IH</sub>(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I<sup>2</sup>C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I<sup>2</sup>C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I<sup>2</sup>C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

266 MHz

378 kHz

0x05

704

333 MHz

0x2A

371 kHz

896

I<sup>2</sup>C source clock frequency is half of the CCB clock frequency for the device.

## 16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD\_TX and  $\overline{SD}_TX$ ) or a receiver input (SD\_RX and  $\overline{SD}_RX$ ). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

• Single-ended swing

The transmitter output signals and the receiver input signals SD\_TX,  $\overline{SD}_TX$ ,  $\overline{SD}_RX$  and  $\overline{SD}_RX$  each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

- Differential output voltage,  $V_{OD}$  (or differential output swing): The differential output voltage (or swing) of the transmitter,  $V_{OD}$ , is defined as the difference of the two complimentary output voltages:  $V_{SD_TX} - V_{\overline{SD_TX}}$ . The  $V_{OD}$  value can be either positive or negative.
- Differential input voltage, V<sub>ID</sub> (or differential input swing): The differential input voltage (or swing) of the receiver, V<sub>ID</sub>, is defined as the difference of the two complimentary input voltages: V<sub>SD\_RX</sub> – V<sub>SD\_RX</sub>. The V<sub>ID</sub> value can be either positive or negative.
- Differential peak voltage,  $V_{DIFFp}$ The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage,  $V_{DIFFp} = |A - B|$  volts.
- Differential peak-to-peak,  $V_{DIFFp-p}$ Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage,  $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$  volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as  $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$ .
- Common mode voltage,  $V_{cm}$ The common mode voltage is equal to one half of the sum of the voltages between each conductor

of a balanced interchange circuit and ground. In this example, for SerDes output,  $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$ , which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V<sub>OD</sub>) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V<sub>OD</sub> is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V<sub>DIFFp</sub>) is 500 mV. The peak-to-peak differential voltage (V<sub>DIFFp</sub>) is 1000 mVp-p.

## 16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD\_REF\_CLK and SD\_REF\_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

## 16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for  $XV_{DD SRDS2}$  are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

#### High-Speed Serial Interfaces (HSSI)

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.





Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50- $\Omega$  termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50  $\Omega$ . R1 is used to DC-bias the LVPECL outputs prior

Table 56. Differential Transmitter	· (TX) Output	<b>Specifications</b>	(continued)
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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V <sub>TX-DC-CM</sub>	The TX DC common mode voltage	0	_	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I <sub>TX-SHORT</sub>	TX short circuit current limit	_	_	90	mA	The total current the transmitter can provide when shorted to its ground
T <sub>TX-IDLE-MIN</sub>	Minimum time spent in electrical idle	50	_		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
RL <sub>TX-DIFF</sub>	Differential return loss	12	_	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL <sub>TX-CM</sub>	Common mode return loss	6		—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z <sub>TX-DIFF-DC</sub>	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z <sub>TX-DC</sub>	Transmitter DC impedance	40	_	_	Ω	Required TX D+ as well as D– DC impedance during all states
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	_	_	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C <sub>TX</sub>	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

Symbol	Parameter	Min	Nom	Max	Unit	Comments
T <sub>crosslink</sub>	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.

- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in Figure 48.)
- 3. A T<sub>TX-EYE</sub> = 0.70 UI provides for a total sum of deterministic and random jitter budget of T<sub>TX-JITTER-MAX</sub> = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The T<sub>TX-EYE-MEDIAN-to-MAX-JITTER</sub> median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50  $\Omega$  to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50- $\Omega$  probes—see Figure 50). Note that the series capacitors C<sub>TX</sub> is optional for the return loss measurement.
- 5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 50 for both V<sub>TX-D+</sub> and V<sub>TX-D-</sub>.
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
- 8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

## 17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 48 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

## NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

#### PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

## NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- $\Omega$  probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

## 17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

## NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 50. Compliance Test/Measurement Load

#### Serial RapidIO

Table 60. Short Run Transmitter	AC Timing Specifications-	–2.5 GBaud
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Characteristic	Symbol	Ra	nge	Unit	Notos
Characteristic	Symbol	Min	Max	Unit	Notes
Output voltage	V <sub>O</sub>	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V <sub>DIFFPP</sub>	500	1000	mV p-p	_
Deterministic jitter	J <sub>D</sub>	—	0.17	UI p-p	_
Total jitter	J <sub>T</sub>	—	0.35	UI p-p	_
Multiple output skew	S <sub>MO</sub>	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

### Table 61. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Rai	Range		Notos	
Characteristic	Symbol	Min	Max	Onic	NOIES	
Output voltage	V <sub>O</sub>	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair	
Differential output voltage	V <sub>DIFFPP</sub>	500	1000	mVp-p	_	
Deterministic jitter	J <sub>D</sub>	_	0.17	UI p-p	_	
Total jitter	J <sub>T</sub>	_	0.35	UI p-p	_	
Multiple output skew	S <sub>MO</sub>		1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit interval	UI	320	320	ps	±100 ppm	

## Table 62. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Netos	
	Symbol	Min	Max	Onic	Notes	
Output voltage	V <sub>O</sub>	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair	
Differential output voltage	V <sub>DIFFPP</sub>	800	1600	mVp-p	_	
Deterministic jitter	J <sub>D</sub>	—	0.17	UI p-p	_	
Total jitter	J <sub>T</sub>	—	0.35	UI p-p	_	
Multiple output skew	S <sub>MO</sub>	—	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit interval	UI	800	800	ps	±100 ppm	

**Package Description** 



- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
- 7. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 8. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

### Figure 56. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	_
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	0	—	24

#### Table 71. MPC8548E Pinout Listing (continued)

#### Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA\_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA\_REQ2.

- 2. Recommend a weak pull-up resistor (2-10 kΩ) be placed on this pin to OV<sub>DD</sub>.
- 3. A valid clock must be provided at POR if TSEC4\_TXD[2] is set = 1.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- 10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V<sub>DD</sub>/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 14.Internal thermally sensitive resistor.
- 15.No connections must be made to these pins if they are not used.
- 16. These pins are not connected for any use.
- 17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV<sub>DD</sub> when using 64-bit buffer mode (pins PCI\_AD[63:32] and PCI1\_C\_BE[7:4]).
- 19.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 20. This pin is only an output in FIFO mode when used as Rx flow control.

24.Do not connect.

#### Package Description

Table 72	. MPC8547E	<b>Pinout</b>	Listing (	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes			
Local Bus Controller Interface							
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	_			
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	—			
LA[27]	H21	0	BV <sub>DD</sub>	5, 9			
LA[28:31]	H20, A27, D26, A28	0	BV <sub>DD</sub>	5, 7, 9			
LCS[0:4]	J25, C20, J24, G26, A26	0	BV <sub>DD</sub>	—			
LCS5/DMA_DREQ2	D23	I/O	BV <sub>DD</sub>	1			
LCS6/DMA_DACK2	G20	0	BV <sub>DD</sub>	1			
LCS7/DMA_DDONE2	E21	0	BV <sub>DD</sub>	1			
LWE0/LBS0/LSDDQM[0]	G25	0	BV <sub>DD</sub>	5, 9			
LWE1/LBS1/LSDDQM[1]	C23	0	BV <sub>DD</sub>	5, 9			
LWE2/LBS2/LSDDQM[2]	J21	0	BV <sub>DD</sub>	5, 9			
LWE3/LBS3/LSDDQM[3]	A24	0	BV <sub>DD</sub>	5, 9			
LALE	H24	0	BV <sub>DD</sub>	5, 8, 9			
LBCTL	G27	0	BV <sub>DD</sub>	5, 8, 9			
LGPL0/LSDA10	F23	0	BV <sub>DD</sub>	5, 9			
LGPL1/LSDWE	G22	0	BV <sub>DD</sub>	5, 9			
LGPL2/LOE/LSDRAS	B27	0	BV <sub>DD</sub>	5, 8, 9			
LGPL3/LSDCAS	F24	0	BV <sub>DD</sub>	5, 9			
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV <sub>DD</sub>	—			
LGPL5	E26	0	BV <sub>DD</sub>	5, 9			
LCKE	E24	0	BV <sub>DD</sub>	—			
LCLK[0:2]	E23, D24, H22	0	BV <sub>DD</sub>	—			
LSYNC_IN	F27	I	BV <sub>DD</sub>	—			
LSYNC_OUT	F28	0	BV <sub>DD</sub>	_			
	DMA		l	1			
DMA_DACK[0:1]	AD3, AE1	0	OV <sub>DD</sub>	5, 9, 107			
DMA_DREQ[0:1]	AD4, AE2	I	OV <sub>DD</sub>	—			
DMA_DDONE[0:1]	AD2, AD1	0	OV <sub>DD</sub>				
	Programmable Interrupt Controller						
UDE	AH16	I	OV <sub>DD</sub>	_			
MCP	AG19	I	OV <sub>DD</sub>	—			

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
Reserved	U20, V22, W20, Y22	_	—	15			
Reserved	U21, V23, W21, Y23	—	—	15			
SD_PLL_TPD	U28	0	XV <sub>DD</sub>	24			
SD_REF_CLK	T28	I	XV <sub>DD</sub>	—			
SD_REF_CLK	T27	I	XV <sub>DD</sub>	—			
Reserved	AC1, AC3	—	—	2			
Reserved	M26, V28	—	—	32			
Reserved	M25, V27	—	—	34			
Reserved	M20, M21, T22, T23	—	—	38			
	General-Purpose Output						
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV <sub>DD</sub>	_			
	System Control						
HRESET	AG17	I	OV <sub>DD</sub>	_			
HRESET_REQ	AG16	0	OV <sub>DD</sub>	29			
SRESET	AG20	I	OV <sub>DD</sub>	_			
CKSTP_IN	AA9	I	OV <sub>DD</sub>	_			
CKSTP_OUT	AA8	0	OV <sub>DD</sub>	2, 4			
	Debug						
TRIG_IN	AB2	I	OV <sub>DD</sub>	—			
TRIG_OUT/READY/QUIESCE	AB1	0	OV <sub>DD</sub>	6, 9, 19, 29			
MSRCID[0:1]	AE4, AG2	0	OV <sub>DD</sub>	5, 6, 9			
MSRCID[2:4]	AF3, AF1, AF2	0	OV <sub>DD</sub>	6, 19, 29			
MDVAL	AE5	0	OV <sub>DD</sub>	6			
CLK_OUT	AE21	0	OV <sub>DD</sub>	11			
	Clock						
RTC	AF16	I	OV <sub>DD</sub>	—			
SYSCLK	AH17	I	OV <sub>DD</sub>	—			
JTAG							
ТСК	AG28	Ι	OV <sub>DD</sub>	—			
TDI	AH28	Ι	OV <sub>DD</sub>	12			
TDO	AF28	0	OV <sub>DD</sub>	_			
TMS	AH27	I	OV <sub>DD</sub>	12			
TRST	AH23	I	OV <sub>DD</sub>	12			

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV <sub>DD</sub>	_
cfg_dram_type0/GPOUT6	R8	0	LV <sub>DD</sub>	5, 9
GPOUT7	N6	0	LV <sub>DD</sub>	—
Reserved	P1		_	104
Reserved	R6		_	104
Reserved	P6	—	_	15
Reserved	N4		_	105
FIFO1_RXC2	P5	I	LV <sub>DD</sub>	104
Reserved	R1	—	—	104
Reserved	P10	—	_	105
FIFO1_TXC2	P7	0	LV <sub>DD</sub>	15
cfg_dram_type1	R10	0	LV <sub>DD</sub>	5, 9
Thr	ee-Speed Ethernet Controller (Gigabit I	Ethernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	-
TSEC3_GTX_CLK	W8	0	TV <sub>DD</sub>	
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	-
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	_
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	—
TSEC3_TX_EN	V9	0	TV <sub>DD</sub>	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	_
Reserved	AA5		_	15
TSEC3_COL	Y5	I	TV <sub>DD</sub>	—
TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	31
TSEC3_TX_ER	AB6	0	TV <sub>DD</sub>	—
I	DUART			
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	—
UART_RTS[0:1]	AC6, AD7	0	OV <sub>DD</sub>	—
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	_
UART_SOUT[0:1]	AB7, AD8	0	OV <sub>DD</sub>	—
	I <sup>2</sup> C interface	1 1		
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4, 27

## Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
JTAG								
ТСК	AG28	I	OV <sub>DD</sub>	_				
TDI	AH28	I	OV <sub>DD</sub>	12				
TDO	AF28	0	OV <sub>DD</sub>	—				
TMS	AH27	I	OV <sub>DD</sub>	12				
TRST	AH23	I	OV <sub>DD</sub>	12				
	DFT	I						
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25				
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25				
LSSD_MODE	AH20	I	OV <sub>DD</sub>	25				
TEST_SEL	AH14	I	OV <sub>DD</sub>	109				
	Thermal Management	•						
THERM0	AG1		—	14				
THERM1	AH1		—	14				
	Power Management	I						
ASLEEP	AH18	0	OV <sub>DD</sub>	9, 19, 29				
	Power and Ground Signals							
GND	<ul> <li>A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17,</li> <li>F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27,</li> <li>L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13,</li> <li>U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27,</li> <li>K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25,</li> <li>AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27</li> </ul>	_						
OV <sub>DD</sub>	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV <sub>DD</sub>	—				
LV <sub>DD</sub>	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV <sub>DD</sub>	_				

### System Design Information



Figure 61. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

**Table 86. Impedance Characteristics** 

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R <sub>N</sub>	43 Target	25 Target	20 Target	Z <sub>0</sub>	W
R <sub>P</sub>	43 Target	25 Target	20 Target	Z <sub>0</sub>	W

**Note:** Nominal supply voltages. See Table 1,  $T_i = 105^{\circ}C$ .

## 22.8 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of  $4.7 \text{ k}\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k $\Omega$ . This value must permit the 4.7-k $\Omega$  resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform/system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor minimizes the disruption of signal quality or speed for output pins thus configured.

#### System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

## 22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k $\Omega$  isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

Rev. Number	Date	Substantive Change(s)	
4	04/2009	<ul> <li>In Table 1, "Absolute Maximum Ratings <sup>1</sup>," and in Table 2, "Recommended Operating Conditions," moved text, "MII management voltage" from LV<sub>DD</sub>/TV<sub>DD</sub> to OV<sub>DD</sub>, added "Ethernet management" to OVDD row of input voltage section.</li> <li>In Table 5, "SYSCLK AC Timing Specifications," added notes 7 and 8 to SYSCLK frequency and cycle</li> </ul>	
		<ul> <li>time.</li> <li>In Table 36, "MII Management DC Electrical Characteristics," changed all instances of LV<sub>DD</sub>/OV<sub>DD</sub> to OV<sub>DD</sub>.</li> <li>Modified Section 16, "High-Speed Serial Interfaces (HSSI)," to reflect that there is only one SerDes.</li> <li>Modified DDR clk rate min from 133 to 166 MHz.</li> <li>Modified note in Table 75, "Processor Core Clocking Specifications (MPC8548E and MPC8547E), "."</li> <li>In Table 56, "Differential Transmitter (TX) Output Specifications," modified equations in Comments column, and changed all instances of "LO" to "LO." Also added note 8.</li> <li>In Table 57, "Differential Receiver (RX) Input Specifications," modified equations in Comments column, and in note 3, changed "TRX-EYE-MEDIAN-to-MAX-JITTER," to "T<sub>RX-EYE-MEDIAN-to-MAX-JITTER</sub>."</li> <li>Modified Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."</li> <li>Added a note on Section 4.1, "System Clock Timing," to limit the SYSCLK to 100 MHz if the core</li> </ul>	
		<ul> <li>frequency is less than 1200 MHz</li> <li>In Table 71, "MPC8548E Pinout ListingTable 72, "MPC8547E Pinout ListingTable 73, "MPC8545E Pinout ListingTable 74, "MPC8543E Pinout Listing," added note 5 to LA[28:31].</li> <li>Added note to Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."</li> </ul>	
3	01/2009	<ul> <li>[Section 4.6, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." Changed minimum frequency equation to be 527 MHz for PCI x8.</li> <li>In Table 5, added note 7.</li> <li>Section 4.5, "Platform to FIFO Restrictions." Changed platform clock frequency to 4.2.</li> <li>Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." Added MII after GMII and add 'or 2.5 V' after 3.3 V.</li> <li>In Table 23, modified table title to include GMII, MII, RMII, and TBI.</li> <li>In Table 24 and Table 25, changed clock period minimum to 5.3.</li> <li>In Table 25, added a note</li> </ul>	
		<ul> <li>In Table 25, added a hole.</li> <li>In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title.</li> <li>In Table 30 and Figure 15, changed all instances of PMA to TSEC<i>n</i>.</li> <li>In Section 8.2.5, "TBI Single-Clock Mode AC Specifications." Replaced first paragraph.</li> <li>In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC<i>n</i>_TX_CLK.</li> <li>In Table 36, changed all instances of OVer to LVer/TVer</li> </ul>	
		<ul> <li>In Table 37, "MII Management AC Timing Specifications," changed MDC minimum clock pulse width high from 32 to 48 ns.</li> <li>Added new section, Section 16, "High-Speed Serial Interfaces (HSSI)."</li> <li>Section 16.1, "DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK." Added new paragraph.</li> <li>Section 17.1, "DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK." Added new paragraph.</li> <li>Added information to Figure 63, both in figure and in note.</li> <li>Section 22.3, "Decoupling Recommendations." Modified the recommendation</li> </ul>	
		Table 87, "Part Numbering Nomenclature." In Silicon Version column added Ver. 2.1.2.	

## Table 88. Document Revision History (continued)