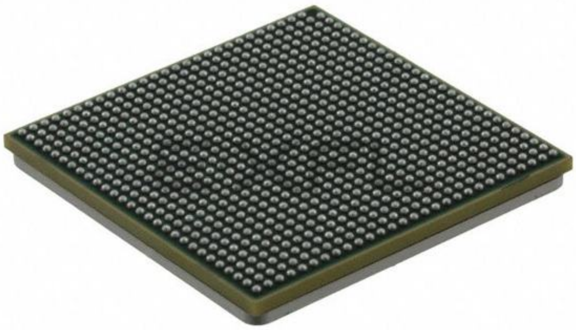




## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 800MHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545evuanj |

— Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
  — Flexible configuration.
  — Full ECC support on 64-bit boundary in both cache and SRAM modes
  — Cache mode supports instruction caching, data caching, or both.
  — External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
  — 1, 2, or 4 ways can be configured for stashing only.
  — Eight-way set-associative cache organization (32-byte cache lines)
  — Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  — Global locking and Flash clearing done through writes to L2 configuration registers
  — Instruction and data locks can be Flash cleared separately.
  — SRAM features include the following:
    – I/O devices access SRAM regions by marking transactions as snoopable (global).
    – Regions can reside at any aligned location in the memory map.
    – Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  — Eight local access windows define mapping within local 36-bit address space.
  — Inbound and outbound ATMUs map to larger external address spaces.
    – Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
    – Four inbound windows plus a default window on RapidIO™
    – Four outbound windows plus default translation for PCI/PCI-X and PCI Express
    – Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
  — Programmable timing supporting DDR and DDR2 SDRAM
  — 64-bit data interface
  — Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
  — DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
  — Full ECC support
  — Page mode support
    – Up to 16 simultaneous open pages for DDR

  - Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

• Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers designed to comply with IEEE Std. 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses

### 2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25<br>25 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V | 1 |
| | 45(default)<br>45(default) | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V | |
| PCI signals | 25 | $OV_{DD}$ = 3.3 V | 2 |
| | 45(default) | | |
| DDR signal | 18<br>36 (half strength mode) | $GV_{DD}$ = 2.5 V | 3 |
| DDR2 signal | 18<br>36 (half strength mode) | $GV_{DD}$ = 1.8 V | 3 |
| TSEC/10/100 signals | 45 | $L/TV_{DD}$ = 2.5/3.3 V | — |
| DUART, system control, JTAG | 45 | $OV_{DD}$ = 3.3 V | — |
| I2C | 150 | $OV_{DD}$ = 3.3 V | — |

**Notes:**
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.
3. The drive strength of the DDR interface in half-strength mode is at $T_j$ = 105°C and at $GV_{DD}$ (min).

## 2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

1. $V_{DD}$, $AV_{DD}$_*n*, $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD}$, $TV_{DD}$, $XV_{DD}$
2. $GV_{DD}$

All supplies must be at their stable values within 50 ms.

**NOTE**

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

**NOTE**

In order to guarantee MCKE low during power-up, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for $GV_{DD}$ is not required.

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

## 7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 20. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$[1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 21. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | $f_{CCB}$/1,048,576 | baud | 1, 2 |
| Maximum baud rate | $f_{CCB}$/16 | baud | 1, 2, 3 |
| Oversample rate | 16 | — | 1, 4 |

**Notes:**
1. Guaranteed by design.
2. $f_{CCB}$ refers to the internal platform clock.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the $8^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each $16^{th}$ sample.

**Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | –1.3 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | –0.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | –0.1 | ns | 4 |
| Local bus clock to address valid for LAD | $t_{LBKLOV3}$ | — | 0 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –3.7 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –3.7 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.2 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.2 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[*n*]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

**Table 56. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{TX\text{-}DC\text{-}CM}$ | The TX DC common mode voltage | 0 | — | 3.6 | V | The allowed DC common mode voltage under any conditions. See Note 6. |
| $I_{TX\text{-}SHORT}$ | TX short circuit current limit | — | — | 90 | mA | The total current the transmitter can provide when shorted to its ground |
| $T_{TX\text{-}IDLE\text{-}MIN}$ | Minimum time spent in electrical idle | 50 | — | | UI | Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set |
| $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ | Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set | — | — | 20 | UI | After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0. |
| $T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$ | Maximum time to transition to valid TX specifications after leaving an electrical idle condition | — | — | 20 | UI | Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle |
| $RL_{TX\text{-}DIFF}$ | Differential return loss | 12 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4. |
| $RL_{TX\text{-}CM}$ | Common mode return loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4. |
| $Z_{TX\text{-}DIFF\text{-}DC}$ | DC differential TX impedance | 80 | 100 | 120 | Ω | TX DC differential mode low impedance |
| $Z_{TX\text{-}DC}$ | Transmitter DC impedance | 40 | — | — | Ω | Required TX D+ as well as D– DC impedance during all states |
| $L_{TX\text{-}SKEW}$ | Lane-to-lane output skew | — | — | 500 + 2 UI | ps | Static skew between any two transmitter lanes within a single Link |
| $C_{TX}$ | AC coupling capacitor | 75 | — | 200 | nF | All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8. |

## 18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- –10 dB for (baud frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ baud frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

**Table 59. Short Run Transmitter AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output voltage | $V_O$ | –0.40 | 2.30 | V | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential output voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | ±100 ppm |

**Table 63. Long Run Transmitter AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output voltage | $V_O$ | –0.40 | 2.30 | V | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential output voltage | $V_{DIFFPP}$ | 800 | 1600 | mVp-p | — |
| Deterministic jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit interval | UI | 400 | 400 | ps | ±100 ppm |

**Table 64. Long Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output voltage | $V_O$ | –0.40 | 2.30 | V | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential output voltage | $V_{DIFFPP}$ | 800 | 1600 | mVp-p | — |
| Deterministic jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit interval | UI | 320 | 320 | ps | ±100 ppm |

For each baud rate at which an LP-serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 52 with the parameters specified in Table 65 when measured at the output pins of the device and the device is driving a 100-Ω ± 5% differential resistive load. The output eye pattern of an LP-serial components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

**Table 66. Receiver AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential input voltage | $V_{IN}$ | 200 | 1600 | mVp-p | Measured at receiver |
| Deterministic jitter tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total jitter tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple input skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit error rate | BER | — | $10^{-12}$ | — | — |
| Unit interval | UI | 800 | 800 | ps | ±100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

**Table 67. Receiver AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential input voltage | $V_{IN}$ | 200 | 1600 | mVp-p | Measured at receiver |
| Deterministic jitter tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total jitter tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple input skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit error rate | BER | — | $10^{-12}$ | | — |
| Unit interval | UI | 400 | 400 | ps | ±100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

# 19 Package Description

This section details package parameters, pin assignments, and dimensions.

## 19.1 Package Parameters

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are provided in Table 70.

**Table 70. Package Parameters**

| Parameter | CBGA[1] | PBGA[2] |
|---|---|---|
| Package outline | 29 mm × 29 mm | 29 mm × 29 mm |
| Interconnects | 783 | 783 |
| Ball pitch | 1 mm | 1 mm |
| Ball diameter (typical) | 0.6 mm | 0.6 mm |
| Solder ball | 63% Sn<br>37% Pb<br>0% Ag | 63% Sn<br>37% Pb<br>0% Ag |
| Solder ball (lead-free) | 95% Sn<br>4.5% Ag<br>0.5% Cu | 96.5% Sn<br>3.5% Ag |

**Notes:**
1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
2. The FC-PBGA package is available on only versions 2.1.1 and 2.1.2, and 3.0 of the device.

### Table 71. MPC8548E Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_RXD[7:0] | P2, R2, N1, N2, P3, M2, M1, N3 | I | $LV_{DD}$ | — |
| TSEC2_TXD[7:0] | N9, N10, P8, N7, R9, N5, R8, N6 | O | $LV_{DD}$ | 5, 9, 33 |
| TSEC2_COL | P1 | I | $LV_{DD}$ | — |
| TSEC2_CRS | R6 | I/O | $LV_{DD}$ | 20 |
| TSEC2_GTX_CLK | P6 | O | $LV_{DD}$ | |
| TSEC2_RX_CLK | N4 | I | $LV_{DD}$ | — |
| TSEC2_RX_DV | P5 | I | $LV_{DD}$ | — |
| TSEC2_RX_ER | R1 | I | $LV_{DD}$ | — |
| TSEC2_TX_CLK | P10 | I | $LV_{DD}$ | — |
| TSEC2_TX_EN | P7 | O | $LV_{DD}$ | 30 |
| TSEC2_TX_ER | R10 | O | $LV_{DD}$ | 5, 9, 33 |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 3)** | | | | |
| TSEC3_TXD[3:0] | V8, W10, Y10, W7 | O | $TV_{DD}$ | 5, 9, 29 |
| TSEC3_RXD[3:0] | Y1, W3, W5, W4 | I | $TV_{DD}$ | — |
| TSEC3_GTX_CLK | W8 | O | $TV_{DD}$ | — |
| TSEC3_RX_CLK | W2 | I | $TV_{DD}$ | — |
| TSEC3_RX_DV | W1 | I | $TV_{DD}$ | — |
| TSEC3_RX_ER | Y2 | I | $TV_{DD}$ | — |
| TSEC3_TX_CLK | V10 | I | $TV_{DD}$ | — |
| TSEC3_TX_EN | V9 | O | $TV_{DD}$ | 30 |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 4)** | | | | |
| TSEC4_TXD[3:0]/TSEC3_TXD[7:4] | AB8, Y7, AA7, Y8 | O | $TV_{DD}$ | 1, 5, 9, 29 |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4] | AA1, Y3, AA2, AA4 | I | $TV_{DD}$ | 1 |
| TSEC4_GTX_CLK | AA5 | O | $TV_{DD}$ | — |
| TSEC4_RX_CLK/TSEC3_COL | Y5 | I | $TV_{DD}$ | 1 |
| TSEC4_RX_DV/TSEC3_CRS | AA3 | I/O | $TV_{DD}$ | 1, 31 |
| TSEC4_TX_EN/TSEC3_TX_ER | AB6 | O | $TV_{DD}$ | 1, 30 |
| **DUART** | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | AB3, AC5 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | AC6, AD7 | O | $OV_{DD}$ | — |
| UART_SIN[0:1] | AB5, AC7 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | AB7, AD8 | O | $OV_{DD}$ | — |

**Table 72. MPC8547E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| TSEC2_TX_ER | R10 | O | $LV_{DD}$ | 5, 9, 33 |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 3)** | | | | |
| TSEC3_TXD[3:0] | V8, W10, Y10, W7 | O | $TV_{DD}$ | 5, 9, 29 |
| TSEC3_RXD[3:0] | Y1, W3, W5, W4 | I | $TV_{DD}$ | — |
| TSEC3_GTX_CLK | W8 | O | $TV_{DD}$ | — |
| TSEC3_RX_CLK | W2 | I | $TV_{DD}$ | — |
| TSEC3_RX_DV | W1 | I | $TV_{DD}$ | — |
| TSEC3_RX_ER | Y2 | I | $TV_{DD}$ | — |
| TSEC3_TX_CLK | V10 | I | $TV_{DD}$ | — |
| TSEC3_TX_EN | V9 | O | $TV_{DD}$ | 30 |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 4)** | | | | |
| TSEC4_TXD[3:0]/TSEC3_TXD[7:4] | AB8, Y7, AA7, Y8 | O | $TV_{DD}$ | 1, 5, 9, 29 |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4] | AA1, Y3, AA2, AA4 | I | $TV_{DD}$ | 1 |
| TSEC4_GTX_CLK | AA5 | O | $TV_{DD}$ | |
| TSEC4_RX_CLK/TSEC3_COL | Y5 | I | $TV_{DD}$ | 1 |
| TSEC4_RX_DV/TSEC3_CRS | AA3 | I/O | $TV_{DD}$ | 1, 31 |
| TSEC4_TX_EN/TSEC3_TX_ER | AB6 | O | $TV_{DD}$ | 1, 30 |
| **DUART** | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | AB3, AC5 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | AC6, AD7 | O | $OV_{DD}$ | — |
| UART_SIN[0:1] | AB5, AC7 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | AB7, AD8 | O | $OV_{DD}$ | — |
| **$I^2C$ Interface** | | | | |
| IIC1_SCL | AG22 | I/O | $OV_{DD}$ | 4, 27 |
| IIC1_SDA | AG21 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SCL | AG15 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SDA | AG14 | I/O | $OV_{DD}$ | 4, 27 |
| **SerDes** | | | | |
| SD_RX[0:3] | M28, N26, P28, R26 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX}}$[0:3] | M27, N25, P27, R25 | I | $XV_{DD}$ | — |
| SD_TX[0:3] | M22, N20, P22, R20 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX}}$[0:3] | M23, N21, P23, R21 | O | $XV_{DD}$ | — |
| Reserved | W26, Y28, AA26, AB28 | — | — | 40 |
| Reserved | W25, Y27, AA25, AB27 | — | — | 40 |

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{UDE}}$ | AH16 | I | $OV_{DD}$ | — |
| $\overline{\text{MCP}}$ | AG19 | I | $OV_{DD}$ | — |
| IRQ[0:7] | AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20 | I | $OV_{DD}$ | — |
| IRQ[8] | AF19 | I | $OV_{DD}$ | — |
| IRQ[9]/$\overline{\text{DMA\_DREQ3}}$ | AF21 | I | $OV_{DD}$ | 1 |
| IRQ[10]/$\overline{\text{DMA\_DACK3}}$ | AE19 | I/O | $OV_{DD}$ | 1 |
| IRQ[11]/$\overline{\text{DMA\_DDONE3}}$ | AD20 | I/O | $OV_{DD}$ | 1 |
| $\overline{\text{IRQ\_OUT}}$ | AD18 | O | $OV_{DD}$ | 2, 4 |
| **Ethernet Management Interface** | | | | |
| EC_MDC | AB9 | O | $OV_{DD}$ | 5, 9 |
| EC_MDIO | AC8 | I/O | $OV_{DD}$ | — |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | V11 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_RXD[7:0] | R5, U1, R3, U2, V3, V1, T3, T2 | I | $LV_{DD}$ | — |
| TSEC1_TXD[7:0] | T10, V7, U10, U5, U4, V6, T5, T8 | O | $LV_{DD}$ | 5, 9 |
| TSEC1_COL | R4 | I | $LV_{DD}$ | — |
| TSEC1_CRS | V5 | I/O | $LV_{DD}$ | 20 |
| TSEC1_GTX_CLK | U7 | O | $LV_{DD}$ | — |
| TSEC1_RX_CLK | U3 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | V2 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | T1 | I | $LV_{DD}$ | — |
| TSEC1_TX_CLK | T6 | I | $LV_{DD}$ | — |
| TSEC1_TX_EN | U9 | O | $LV_{DD}$ | 30 |
| TSEC1_TX_ER | T7 | O | $LV_{DD}$ | — |
| GPIN[0:7] | P2, R2, N1, N2, P3, M2, M1, N3 | I | $LV_{DD}$ | 103 |
| GPOUT[0:5] | N9, N10, P8, N7, R9, N5 | O | $LV_{DD}$ | — |
| cfg_dram_type0/GPOUT6 | R8 | O | $LV_{DD}$ | 5, 9 |
| GPOUT7 | N6 | O | $LV_{DD}$ | — |
| Reserved | P1 | — | — | 104 |
| Reserved | R6 | — | — | 104 |
| Reserved | P6 | — | — | 15 |
| Reserved | N4 | — | — | 105 |

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $GV_{DD}$ | B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V) | $GV_{DD}$ | — |
| $BV_{DD}$ | C21, C24, C27, E20, E25, G19, G23, H26, J20 | Power for local bus (1.8 V, 2.5 V, 3.3 V) | $BV_{DD}$ | — |
| $V_{DD}$ | M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19 | Power for core (1.1 V) | $V_{DD}$ | — |
| $SV_{DD}$ | L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27 | Core power for SerDes transceivers (1.1 V) | $SV_{DD}$ | — |
| $XV_{DD}$ | L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20 | Pad power for SerDes transceivers (1.1 V) | $XV_{DD}$ | — |
| AVDD_LBIU | J28 | Power for local bus PLL (1.1 V) | — | 26 |
| AVDD_PCI1 | AH21 | Power for PCI1 PLL (1.1 V) | — | 26 |
| AVDD_PCI2 | AH22 | Power for PCI2 PLL (1.1 V) | — | 26 |
| AVDD_CORE | AH15 | Power for e500 PLL (1.1 V) | — | 26 |
| AVDD_PLAT | AH19 | Power for CCB PLL (1.1 V) | — | 26 |
| AVDD_SRDS | U25 | Power for SRDSPLL (1.1 V) | — | 26 |
| SENSEVDD | M14 | O | $V_{DD}$ | 13 |
| SENSEVSS | M16 | — | — | 13 |
| **Analog Signals** | | | | |
| MVREF | A18 | I Reference voltage signal for DDR | MVREF | — |

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| SD_IMP_CAL_RX | L28 | I | 200 Ω to GND | — |
| SD_IMP_CAL_TX | AB26 | I | 100 Ω to GND | — |
| SD_PLL_TPA | U26 | O | — | 24 |

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

## NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

**Table 74. MPC8543E Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 (One 32-Bit)** | | | | |
| Reserved | AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, | — | — | 110 |
| GPOUT[8:15] | AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22 | O | $OV_{DD}$ | — |
| GPIN[8:15] | AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24 | I | $OV_{DD}$ | 111 |
| PCI1_AD[31:0] | AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15 | I/O | $OV_{DD}$ | 17 |
| Reserved | AF15, AD14, AE15, AD15 | — | — | 110 |
| PCI1_C_$\overline{\text{BE}}$[3:0] | AF9, AD11, Y12, Y13 | I/O | $OV_{DD}$ | 17 |
| Reserved | W15 | — | — | 110 |
| $\overline{\text{PCI1\_GNT}}$[4:1] | AG6, AE6, AF5, AH5 | O | $OV_{DD}$ | 5, 9, 35 |
| $\overline{\text{PCI1\_GNT0}}$ | AG5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_IRDY}}$ | AF11 | I/O | $OV_{DD}$ | 2 |
| PCI1_PAR | AD12 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_PERR}}$ | AC12 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1\_SERR}}$ | V13 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI1\_STOP}}$ | W12 | I/O | $OV_{DD}$ | 2 |

**Table 74. MPC8543E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| IIC1_SDA | AG21 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SCL | AG15 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SDA | AG14 | I/O | $OV_{DD}$ | 4, 27 |
| **SerDes** | | | | |
| SD_RX[0:7] | M28, N26, P28, R26, W26, Y28, AA26, AB28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX}}$[0:7] | M27, N25, P27, R25, W25, Y27, AA25, AB27 | I | $XV_{DD}$ | — |
| SD_TX[0:7] | M22, N20, P22, R20, U20, V22, W20, Y22 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX}}$[0:7] | M23, N21, P23, R21, U21, V23, W21, Y23 | O | $XV_{DD}$ | — |
| SD_PLL_TPD | U28 | O | $XV_{DD}$ | 24 |
| SD_REF_CLK | T28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK}}$ | T27 | I | $XV_{DD}$ | — |
| Reserved | AC1, AC3 | — | — | 2 |
| Reserved | M26, V28 | — | — | 32 |
| Reserved | M25, V27 | — | — | 34 |
| Reserved | M20, M21, T22, T23 | — | — | 38 |
| **General-Purpose Output** | | | | |
| GPOUT[24:31] | K26, K25, H27, G28, H25, J26, K24, K23 | O | $BV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | AG17 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET\_REQ}}$ | AG16 | O | $OV_{DD}$ | 29 |
| $\overline{\text{SRESET}}$ | AG20 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_IN}}$ | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_OUT}}$ | AA8 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | |
| TRIG_IN | AB2 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY/$\overline{\text{QUIESCE}}$ | AB1 | O | $OV_{DD}$ | 6, 9, 19, 29 |
| MSRCID[0:1] | AE4, AG2 | O | $OV_{DD}$ | 5, 6, 9 |
| MSRCID[2:4] | AF3, AF1, AF2 | O | $OV_{DD}$ | 6, 19, 29 |
| MDVAL | AE5 | O | $OV_{DD}$ | 6 |
| CLK_OUT | AE21 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | |
| RTC | AF16 | I | $OV_{DD}$ | — |
| SYSCLK | AH17 | I | $OV_{DD}$ | — |

# 20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

**Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)**

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 1000 MHz | | 1200 MHz | | 1333 MHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 800 | 1000 | 800 | 1200 | 800 | 1333 | MHz | 1, 2 |

**Notes**:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

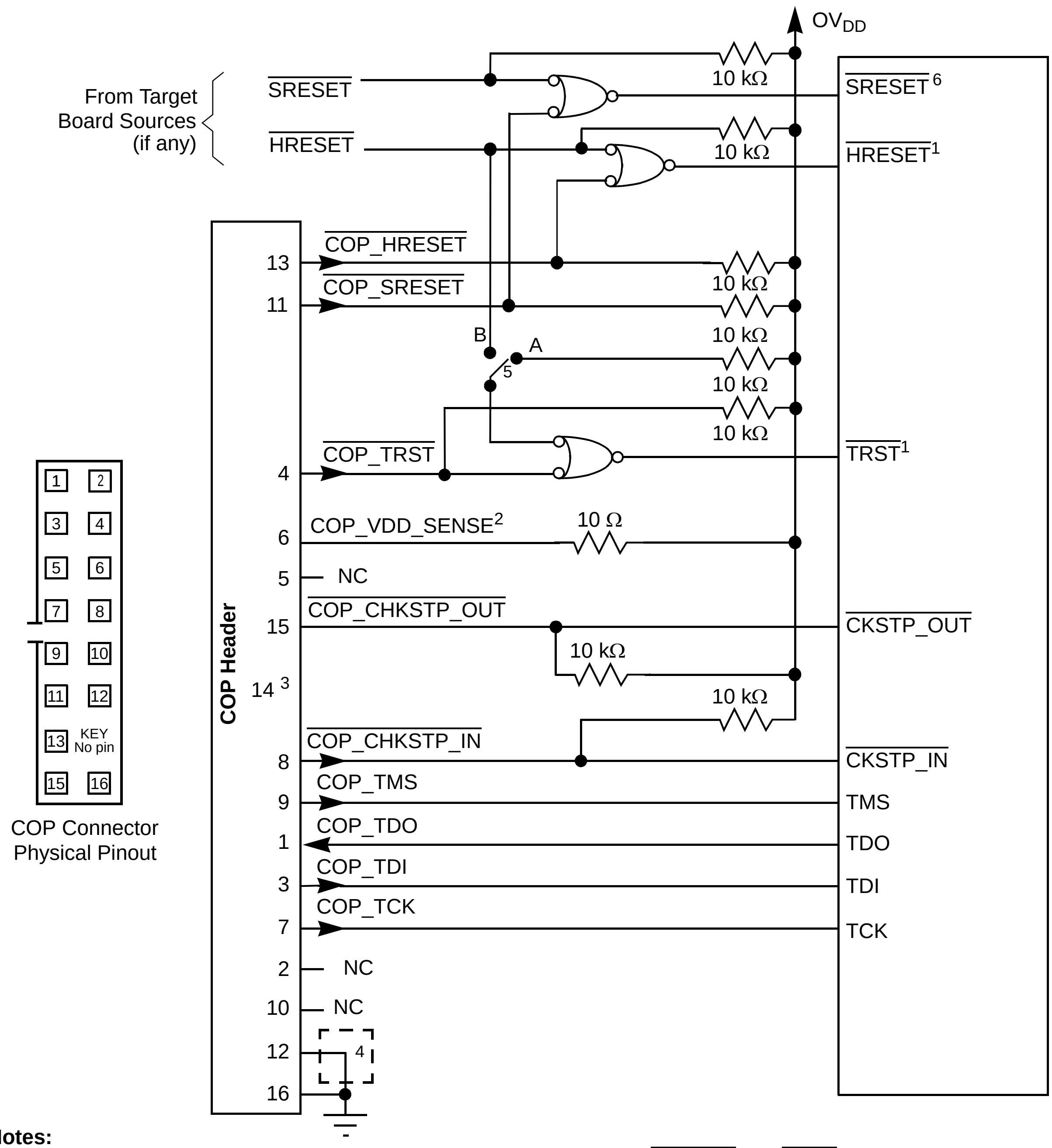
2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

**Table 76. Processor Core Clocking Specifications (MPC8545E)**

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 800 MHz | | 1000 MHz | | 1200 MHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 800 | 800 | 800 | 1000 | 800 | 1200 | MHz | 1, 2 |

**Notes**:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.




**Notes:**

1. The COP port and target board must be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10–Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

**Figure 63. JTAG Interface Connection**

**Table 87. Part Numbering Nomenclature (continued)**

| MPC | *nnnnn* | *t* | *pp* | *ff* | *c* | *r* |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Temperature** | **Package[1, 2, 3]** | **Processor Frequency[4]** | **Core Frequency** | **Silicon Version** |
| MPC | 8545E | Blank = 0 to 105°C<br>C = –40° to 105°C | HX = CBGA<br>VU = Pb-free CBGA<br>PX = PBGA<br>VT = Pb-free PBGA | AT = 1200<br>AQ = 1000<br>AN = 800 | G = 400 | Blank = Ver. 2.0<br>(SVR = 0x80390220)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x<br>(SVR = 0x80390231) |
| | 8545 | | | | | Blank = Ver. 2.0<br>(SVR = 0x80310220)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x<br>(SVR = 0x80310231) |
| | 8543E | | | AQ = 1000<br>AN = 800 | | Blank = Ver. 2.0<br>(SVR = 0x803A0020)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x<br>(SVR = 0x803A0031) |
| | 8543 | | | | | Blank = Ver. 2.0<br>(SVR = 0x80320020)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x<br>(SVR = 0x80320031) |

**Notes:**

1. See Section 19, "Package Description," for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

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