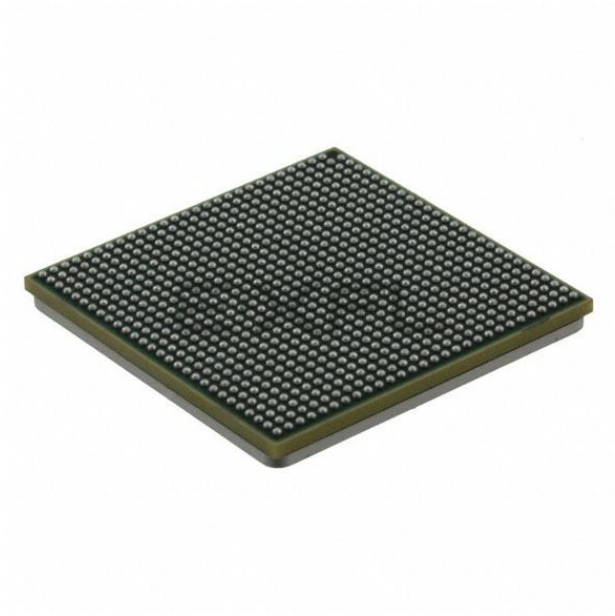

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.2GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545evuatg |

  - Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers designed to comply with IEEE Std. 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses

## 4.5 Platform to FIFO Restrictions

Note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency ≤ platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 167 MHz.

## 4.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527\ \text{MHz} \times (\text{PCI-Express link width})}{8}$$

See *MPC8548ERM, Rev. 2, PowerQUICC III Integrated Processor Family Reference Manual*, Section 18.1.3.2, “Link Width,” for PCI Express interface width details.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

See *MPC8548ERM, Rev. 2, PowerQUICC III Integrated Processor Family Reference Manual*, Section 17.4, “1x/4x LP-Serial Signal Descriptions,” for serial RapidIO interface width and frequency details.

## 4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform see the specific section of this document.

Figure 17 shows the RGMII and RTBI AC timing and multiplexing diagrams.

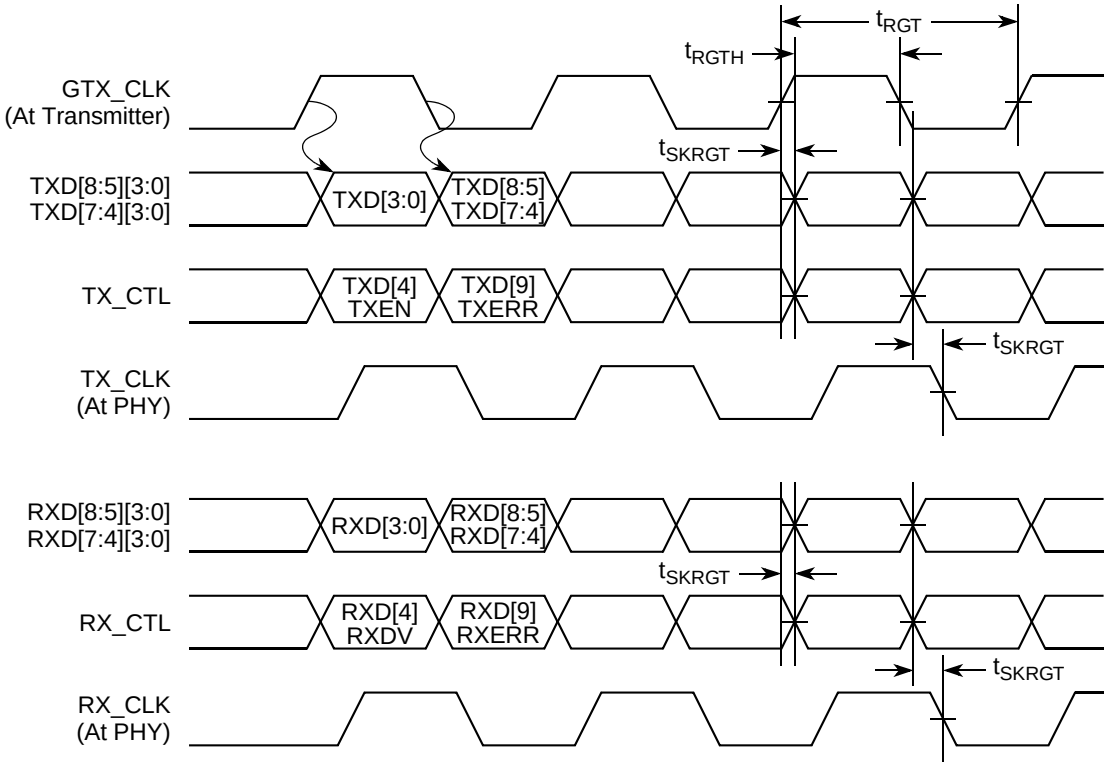


**Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

**Table 34. RMII Transmit AC Timing Specifications**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSEC*n*_TX_CLK clock period | $t_{RMT}$ | 15.0 | 20.0 | 25.0 | ns |
| TSEC*n*_TX_CLK duty cycle | $t_{RMTH}$ | 35 | 50 | 65 | % |
| TSEC*n*_TX_CLK peak-to-peak jitter | $t_{RMTJ}$ | — | — | 250 | ps |
| Rise time TSEC*n*_TX_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSEC*n*_TX_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 2.0 | ns |

Figure 19 provides the AC test load for eTSEC.

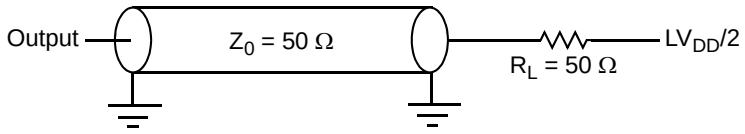


**Figure 19. eTSEC AC Test Load**

Figure 20 shows the RMII receive AC timing diagram.

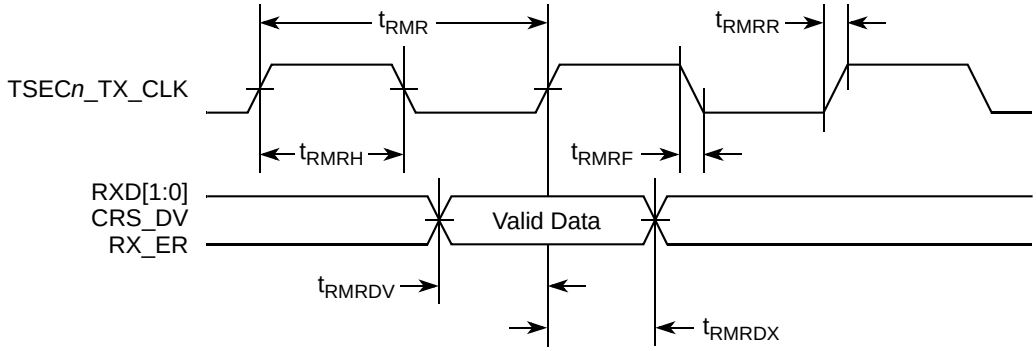


**Figure 20. RMII Receive AC Timing Diagram**

Table 41 describes the timing parameters of the local bus interface at $BV_{DD}$ = 2.5 V.

**Table 41. Local Bus Timing Parameters ($BV_{DD}$ = 2.5 V)—PLL Enabled**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/UPWAIT) | $t_{LBIVKH1}$ | 1.9 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.8 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.1 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.3 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.4 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.4 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.8 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

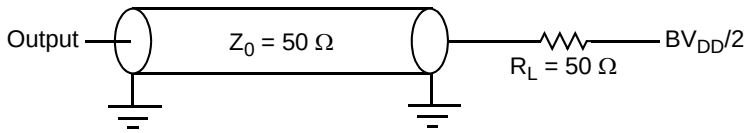


**Figure 22. Local Bus AC Test Load**

Figure 34 shows the AC timing diagram for the I²C bus.

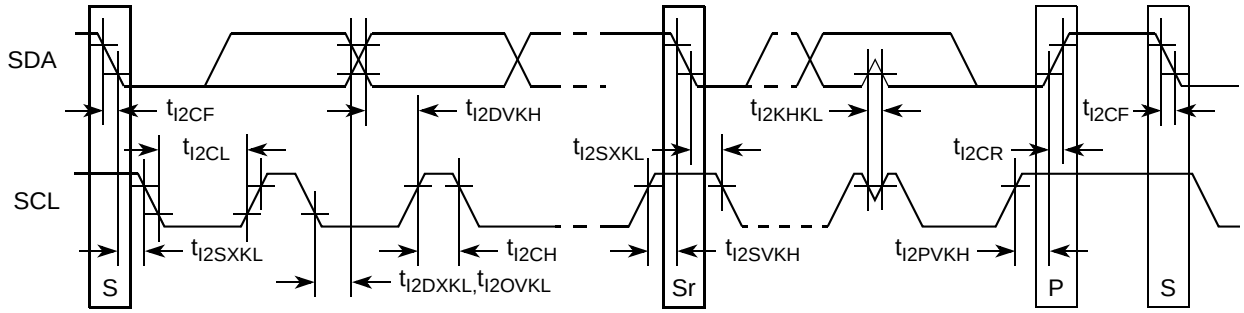


**Figure 34. I²C Bus AC Timing Diagram**

Figure 36 shows the PCI/PCI-X input AC timing conditions.

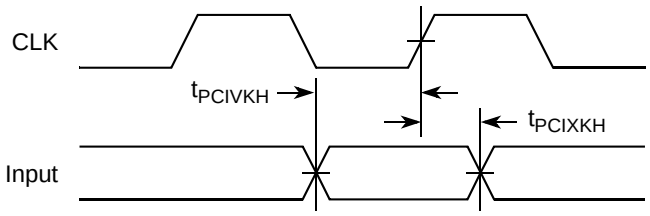


**Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions**

Figure 37 shows the PCI/PCI-X output AC timing conditions.

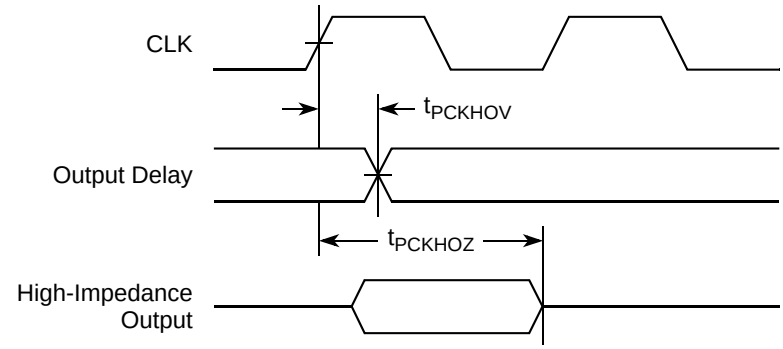


**Figure 37. PCI/PCI-X Output AC Timing Measurement Condition**

Table 53 provides the PCI-X AC timing specifications at 66 MHz.

**Table 53. PCI-X AC Timing Specifications at 66 MHz**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SYSCLK to signal valid delay | $t_{PCKHOV}$ | — | 3.8 | ns | 1, 2, 3, 7, 8 |
| Output hold from SYSCLK | $t_{PCKHOX}$ | 0.7 | — | ns | 1, 10 |
| SYSCLK to output high impedance | $t_{PCKHOZ}$ | — | 7 | ns | 1, 4, 8, 11 |
| Input setup time to SYSCLK | $t_{PCIVKH}$ | 1.7 | — | ns | 3, 5 |
| Input hold time from SYSCLK | $t_{PCIXKH}$ | 0.5 | — | ns | 10 |
| $\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time | $t_{PCRVRH}$ | 10 | — | clocks | 11 |
| $\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time | $t_{PCRHRX}$ | 0 | 50 | ns | 11 |
| $\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion | $t_{PCRHFV}$ | 10 | — | clocks | 9, 11 |
| PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time | $t_{PCIVRH}$ | 10 | — | clocks | 11 |

# 16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- Single-ended swing
  The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.
- Differential output voltage, $V_{OD}$ (or differential output swing):
  The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The $V_{OD}$ value can be either positive or negative.
- Differential input voltage, $V_{ID}$ (or differential input swing):
  The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The $V_{ID}$ value can be either positive or negative.
- Differential peak voltage, $V_{DIFFp}$
  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- Differential peak-to-peak, $V_{DIFFp-p}$
  Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
- Common mode voltage, $V_{cm}$
  The common mode voltage is equal to one half of the sum of the voltages between each conductor

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

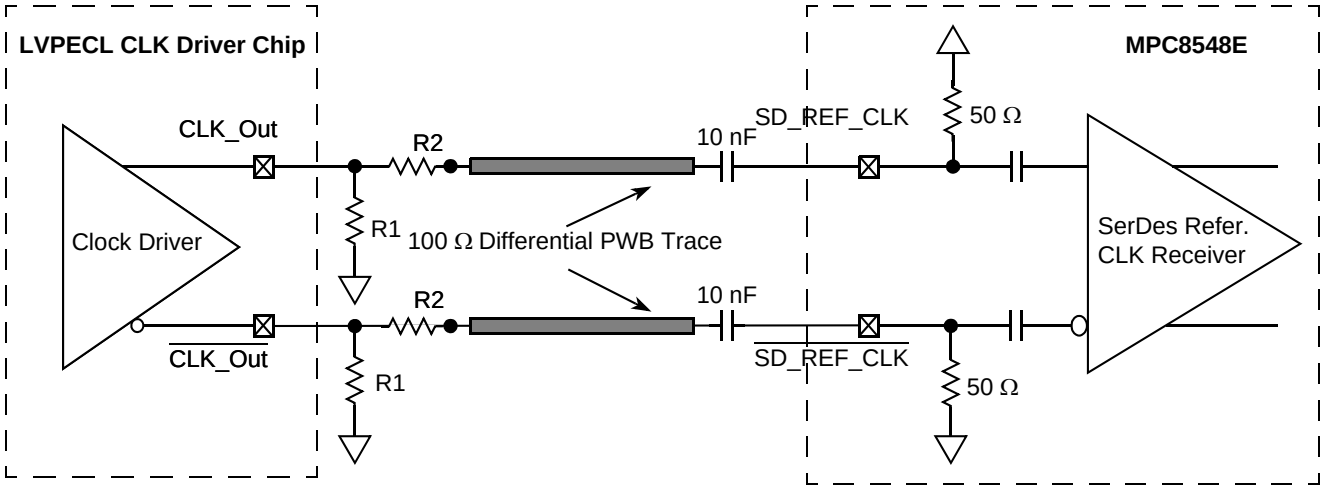


**Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.

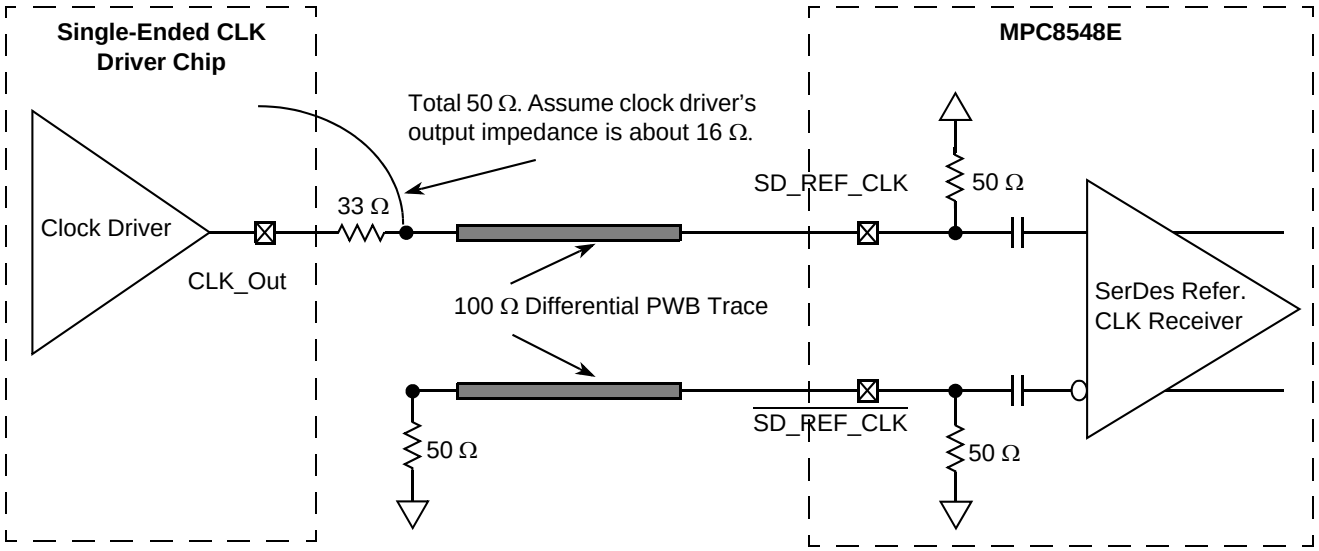


**Figure 46. Single-Ended Connection (Reference Only)**

**Table 57. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{RX-CM-ACp}$ | AC peak common mode input voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 + V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert \div 2$. See Note 2. |
| $RL_{RX-DIFF}$ | Differential return loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4. |
| $RL_{RX-CM}$ | Common mode return loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4. |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | 80 | 100 | 120 | Ω | RX DC differential mode impedance. See Note 5. |
| $Z_{RX-DC}$ | DC input impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered down DC input impedance | 200 k | — | — | Ω | Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical idle detect threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$. Measured at the package pins of the receiver |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected electrical idle enter detect threshold integration time | — | — | 10 | ms | An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |

## 18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B volts.
2. The differential output signal of the transmitter, $V_{OD}$, is defined as $V_{TD} - V_{\overline{TD}}$.
3. The differential input signal of the receiver, $V_{ID}$, is defined as $V_{RD} - V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

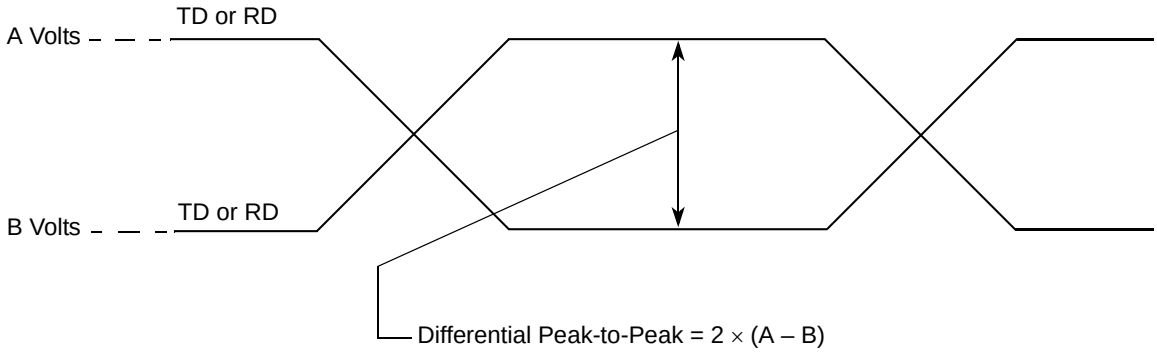


**Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mVp-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

## 18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 19.3 Pinout Listings

**NOTE**

The $\overline{\text{DMA\_DACK}}$[0:1] and TEST_SEL/$\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on PCI1_AD[63:32]/PC2_AD[31:0] pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

**Table 71. MPC8548E Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 and PCI2 (One 64-Bit or Two 32-Bit)** | | | | |
| PCI1_AD[63:32]/PCI2_AD[31:0] | AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24 | I/O | $OV_{DD}$ | 17 |
| PCI1_AD[31:0] | AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{\text{BE}}$[7:4]/PCI2_C_$\overline{\text{BE}}$[3:0] | AF15, AD14, AE15, AD15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{\text{BE}}$[3:0] | AF9, AD11, Y12, Y13 | I/O | $OV_{DD}$ | 17 |
| PCI1_PAR64/PCI2_PAR | W15 | I/O | $OV_{DD}$ | |
| $\overline{\text{PCI1\_GNT}}$[4:1] | AG6, AE6, AF5, AH5 | O | $OV_{DD}$ | 5, 9, 35 |
| $\overline{\text{PCI1\_GNT0}}$ | AG5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_IRDY}}$ | AF11 | I/O | $OV_{DD}$ | 2 |
| PCI1_PAR | AD12 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_PERR}}$ | AC12 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1\_SERR}}$ | V13 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI1\_STOP}}$ | W12 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1\_TRDY}}$ | AG11 | I/O | $OV_{DD}$ | 2 |

**Table 71. MPC8548E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| PCI1_REQ[4:1] | AH2, AG4, AG3, AH4 | I | $OV_{DD}$ | — |
| | | | | — |
| | | | | — |
| | | | | — |
| | | | | — |
| PCI1_REQ0 | AH3 | I/O | $OV_{DD}$ | — |
| PCI1_CLK | AH26 | I | $OV_{DD}$ | 39 |
| PCI1_DEVSEL | AH11 | I/O | $OV_{DD}$ | 2 |
| PCI1_FRAME | AE11 | I/O | $OV_{DD}$ | 2 |
| PCI1_IDSEL | AG9 | I | $OV_{DD}$ | — |
| PCI1_REQ64/PCI2_FRAME | AF14 | I/O | $OV_{DD}$ | 2, 5, 10 |
| PCI1_ACK64/PCI2_DEVSEL | V15 | I/O | $OV_{DD}$ | 2 |
| PCI2_CLK | AE28 | I | $OV_{DD}$ | 39 |
| PCI2_IRDY | AD26 | I/O | $OV_{DD}$ | 2 |
| PCI2_PERR | AD25 | I/O | $OV_{DD}$ | 2 |
| PCI2_GNT[4:1] | AE26, AG24, AF25, AE25 | O | $OV_{DD}$ | 5, 9, 35 |
| PCI2_GNT0 | AG25 | I/O | $OV_{DD}$ | — |
| PCI2_SERR | AD24 | I/O | $OV_{DD}$ | 2, 4 |
| PCI2_STOP | AF24 | I/O | $OV_{DD}$ | 2 |
| PCI2_TRDY | AD27 | I/O | $OV_{DD}$ | 2 |
| PCI2_REQ[4:1] | AD28, AE27, W17, AF26 | I | $OV_{DD}$ | — |
| PCI2_REQ0 | AH25 | I/O | $OV_{DD}$ | — |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | H13, F13, F11, C11, J13, G13, D12, M12 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | M17, C16, K17, E16, B6, C4, H4, K1, E13 | O | $GV_{DD}$ | — |
| MDQS[0:8] | M15, A16, G17, G14, A5, D3, H1, L2, C13 | I/O | $GV_{DD}$ | — |
| MDQS[0:8] | L17, B16, J16, H14, C6, C2, H3, L4, D13 | I/O | $GV_{DD}$ | — |
| MA[0:15] | A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11 | O | $GV_{DD}$ | — |
| MBA[0:2] | F7, J7, M11 | O | $GV_{DD}$ | — |

**Table 71. MPC8548E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $LV_{DD}$ | N8, R7, T9, U6 | Power for TSEC1 and TSEC2 (2.5 V, 3.3 V) | $LV_{DD}$ | — |
| $TV_{DD}$ | W9, Y6 | Power for TSEC3 and TSEC4 (2,5 V, 3.3 V) | $TV_{DD}$ | — |
| $GV_{DD}$ | B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5) | $GV_{DD}$ | — |
| $BV_{DD}$ | C21, C24, C27, E20, E25, G19, G23, H26, J20 | Power for local bus (1.8 V, 2.5 V, 3.3 V) | $BV_{DD}$ | — |
| $V_{DD}$ | M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19 | Power for core (1.1 V) | $V_{DD}$ | — |
| $SV_{DD}$ | L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27 | Core Power for SerDes transceivers (1.1 V) | $SV_{DD}$ | — |
| $XV_{DD}$ | L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20 | Pad Power for SerDes transceivers (1.1 V) | $XV_{DD}$ | — |
| AVDD_LBIU | J28 | Power for local bus PLL (1.1 V) | — | 26 |
| AVDD_PCI1 | AH21 | Power for PCI1 PLL (1.1 V) | — | 26 |
| AVDD_PCI2 | AH22 | Power for PCI2 PLL (1.1 V) | — | 26 |
| AVDD_CORE | AH15 | Power for e500 PLL (1.1 V) | — | 26 |
| AVDD_PLAT | AH19 | Power for CCB PLL (1.1 V) | — | 26 |
| AVDD_SRDS | U25 | Power for SRDSPLL (1.1 V) | — | 26 |
| SENSEVDD | M14 | O | $V_{DD}$ | 13 |

**Table 72. MPC8547E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| Reserved | AE26 | — | — | 2 |
| cfg_pci1_clk | AG24 | I | $OV_{DD}$ | 5 |
| Reserved | AF25 | — | — | 101 |
| Reserved | AE25 | — | — | 2 |
| Reserved | AG25 | — | — | 2 |
| Reserved | AD24 | — | — | 2 |
| Reserved | AF24 | — | — | 2 |
| Reserved | AD27 | — | — | 2 |
| Reserved | AD28, AE27, W17, AF26 | — | — | 2 |
| Reserved | AH25 | — | — | 2 |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | H13, F13, F11, C11, J13, G13, D12, M12 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | M17, C16, K17, E16, B6, C4, H4, K1, E13 | O | $GV_{DD}$ | — |
| MDQS[0:8] | M15, A16, G17, G14, A5, D3, H1, L2, C13 | I/O | $GV_{DD}$ | — |
| $\overline{\text{MDQS}}$[0:8] | L17, B16, J16, H14, C6, C2, H3, L4, D13 | I/O | $GV_{DD}$ | — |
| MA[0:15] | A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11 | O | $GV_{DD}$ | — |
| MBA[0:2] | F7, J7, M11 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | E7 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | H7 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | L8 | O | $GV_{DD}$ | — |
| MCKE[0:3] | F10, C10, J11, H11 | O | $GV_{DD}$ | 11 |
| $\overline{\text{MCS}}$[0:3] | K8, J8, G8, F8 | O | $GV_{DD}$ | — |
| MCK[0:5] | H9, B15, G2, M9, A14, F1 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | J9, A15, G1, L9, B14, F2 | O | $GV_{DD}$ | — |
| MODT[0:3] | E6, K6, L7, M7 | O | $GV_{DD}$ | — |
| MDIC[0:1] | A19, B19 | I/O | $GV_{DD}$ | 36 |

**Table 72. MPC8547E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| Reserved | U20, V22, W20, Y22 | — | — | 15 |
| Reserved | U21, V23, W21, Y23 | — | — | 15 |
| SD_PLL_TPD | U28 | O | $XV_{DD}$ | 24 |
| SD_REF_CLK | T28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK}}$ | T27 | I | $XV_{DD}$ | — |
| Reserved | AC1, AC3 | — | — | 2 |
| Reserved | M26, V28 | — | — | 32 |
| Reserved | M25, V27 | — | — | 34 |
| Reserved | M20, M21, T22, T23 | — | — | 38 |
| **General-Purpose Output** | | | | |
| GPOUT[24:31] | K26, K25, H27, G28, H25, J26, K24, K23 | O | $BV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | AG17 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET\_REQ}}$ | AG16 | O | $OV_{DD}$ | 29 |
| $\overline{\text{SRESET}}$ | AG20 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_IN}}$ | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_OUT}}$ | AA8 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | |
| TRIG_IN | AB2 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY/$\overline{\text{QUIESCE}}$ | AB1 | O | $OV_{DD}$ | 6, 9, 19, 29 |
| MSRCID[0:1] | AE4, AG2 | O | $OV_{DD}$ | 5, 6, 9 |
| MSRCID[2:4] | AF3, AF1, AF2 | O | $OV_{DD}$ | 6, 19, 29 |
| MDVAL | AE5 | O | $OV_{DD}$ | 6 |
| CLK_OUT | AE21 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | |
| RTC | AF16 | I | $OV_{DD}$ | — |
| SYSCLK | AH17 | I | $OV_{DD}$ | — |
| **JTAG** | | | | |
| TCK | AG28 | I | $OV_{DD}$ | — |
| TDI | AH28 | I | $OV_{DD}$ | 12 |
| TDO | AF28 | O | $OV_{DD}$ | — |
| TMS | AH27 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | AH23 | I | $OV_{DD}$ | 12 |

**Table 74. MPC8543E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| IIC1_SDA | AG21 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SCL | AG15 | I/O | $OV_{DD}$ | 4, 27 |
| IIC2_SDA | AG14 | I/O | $OV_{DD}$ | 4, 27 |
| **SerDes** | | | | |
| SD_RX[0:7] | M28, N26, P28, R26, W26, Y28, AA26, AB28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX}}$[0:7] | M27, N25, P27, R25, W25, Y27, AA25, AB27 | I | $XV_{DD}$ | — |
| SD_TX[0:7] | M22, N20, P22, R20, U20, V22, W20, Y22 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX}}$[0:7] | M23, N21, P23, R21, U21, V23, W21, Y23 | O | $XV_{DD}$ | — |
| SD_PLL_TPD | U28 | O | $XV_{DD}$ | 24 |
| SD_REF_CLK | T28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK}}$ | T27 | I | $XV_{DD}$ | — |
| Reserved | AC1, AC3 | — | — | 2 |
| Reserved | M26, V28 | — | — | 32 |
| Reserved | M25, V27 | — | — | 34 |
| Reserved | M20, M21, T22, T23 | — | — | 38 |
| **General-Purpose Output** | | | | |
| GPOUT[24:31] | K26, K25, H27, G28, H25, J26, K24, K23 | O | $BV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | AG17 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET\_REQ}}$ | AG16 | O | $OV_{DD}$ | 29 |
| $\overline{\text{SRESET}}$ | AG20 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_IN}}$ | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_OUT}}$ | AA8 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | |
| TRIG_IN | AB2 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY/$\overline{\text{QUIESCE}}$ | AB1 | O | $OV_{DD}$ | 6, 9, 19, 29 |
| MSRCID[0:1] | AE4, AG2 | O | $OV_{DD}$ | 5, 6, 9 |
| MSRCID[2:4] | AF3, AF1, AF2 | O | $OV_{DD}$ | 6, 19, 29 |
| MDVAL | AE5 | O | $OV_{DD}$ | 6 |
| CLK_OUT | AE21 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | |
| RTC | AF16 | I | $OV_{DD}$ | — |
| SYSCLK | AH17 | I | $OV_{DD}$ | — |

level must always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.

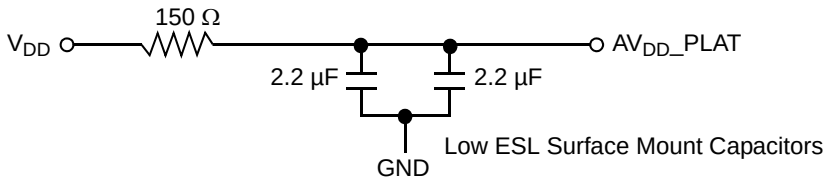


**Figure 57. PLL Power Supply Filter Circuit with PLAT Pins**

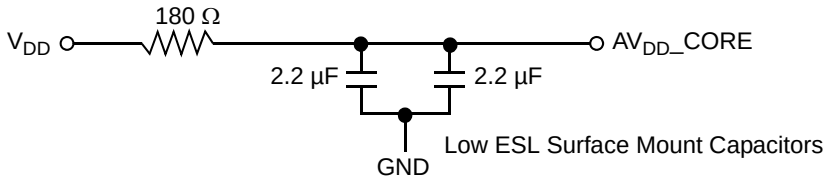


**Figure 58. PLL Power Supply Filter Circuit with CORE Pins**

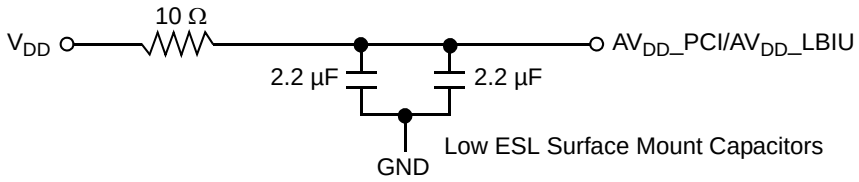


**Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins**

The $AV_{DD}$_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the $AV_{DD}$_SRDS ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDS to

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

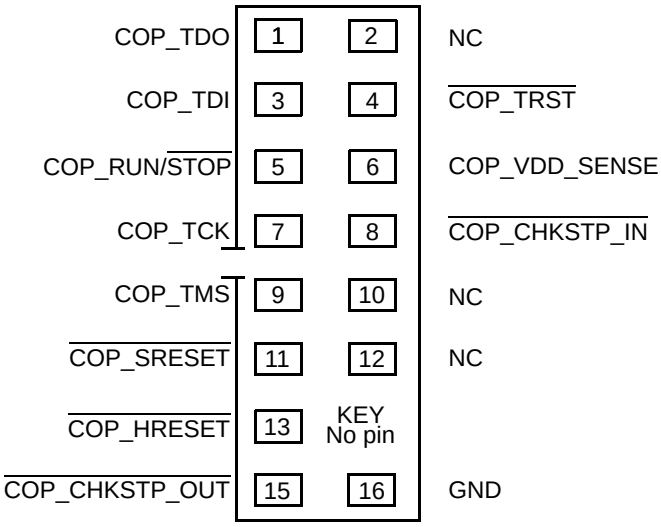


**Figure 62. COP Connector Physical Pinout**

**Table 88. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 4 | 04/2009 | • In Table 1, "Absolute Maximum Ratings [1]," and in Table 2, "Recommended Operating Conditions," moved text, "MII management voltage" from $LV_{DD}/TV_{DD}$ to $OV_{DD}$, added "Ethernet management" to OVDD row of input voltage section.<br>• In Table 5, "SYSCLK AC Timing Specifications," added notes 7 and 8 to SYSCLK frequency and cycle time.<br>• In Table 36, "MII Management DC Electrical Characteristics," changed all instances of $LV_{DD}/OV_{DD}$ to $OV_{DD}$.<br>• Modified Section 16, "High-Speed Serial Interfaces (HSSI)," to reflect that there is only one SerDes.<br>• Modified DDR clk rate min from 133 to 166 MHz.<br>• Modified note in Table 75, "Processor Core Clocking Specifications (MPC8548E and MPC8547E), "."<br>• In Table 56, "Differential Transmitter (TX) Output Specifications," modified equations in Comments column, and changed all instances of "LO" to "L0." Also added note 8.<br>• In Table 57, "Differential Receiver (RX) Input Specifications," modified equations in Comments column, and in note 3, changed "TRX-EYE-MEDIAN-to-MAX-JITTER," to "$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$."<br>• Modified Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."<br>• Added a note on Section 4.1, "System Clock Timing," to limit the SYSCLK to 100 MHz if the core frequency is less than 1200 MHz<br>• In Table 71, "MPC8548E Pinout ListingTable 72, "MPC8547E Pinout ListingTable 73, "MPC8545E Pinout ListingTable 74, "MPC8543E Pinout Listing," added note 5 to LA[28:31].<br>• Added note to Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds." |
| 3 | 01/2009 | • [Section 4.6, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." Changed minimum frequency equation to be 527 MHz for PCI x8.<br>• In Table 5, added note 7.<br>• Section 4.5, "Platform to FIFO Restrictions." Changed platform clock frequency to 4.2.<br>• Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." Added MII after GMII and add 'or 2.5 V' after 3.3 V.<br>• In Table 23, modified table title to include GMII, MII, RMII, and TBI.<br>• In Table 24 and Table 25, changed clock period minimum to 5.3.<br>• In Table 25, added a note.<br>• In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title.<br>• In Table 30 and Figure 15, changed all instances of PMA to TSEC*n*.<br>• In Section 8.2.5, "TBI Single-Clock Mode AC Specifications." Replaced first paragraph.<br>• In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC*n*_TX_CLK.<br>• In Table 36, changed all instances of $OV_{DD}$ to $LV_{DD}/TV_{DD}$.<br>• In Table 37, "MII Management AC Timing Specifications," changed MDC minimum clock pulse width high from 32 to 48 ns.<br>• Added new section, Section 16, "High-Speed Serial Interfaces (HSSI)."<br>• Section 16.1, "DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK." Added new paragraph.<br>• Section 17.1, "DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK." Added new paragraph.<br>• Added information to Figure 63, both in figure and in note.<br>• Section 22.3, "Decoupling Recommendations." Modified the recommendation.<br>• Table 87, "Part Numbering Nomenclature." In Silicon Version column added Ver. 2.1.2. |