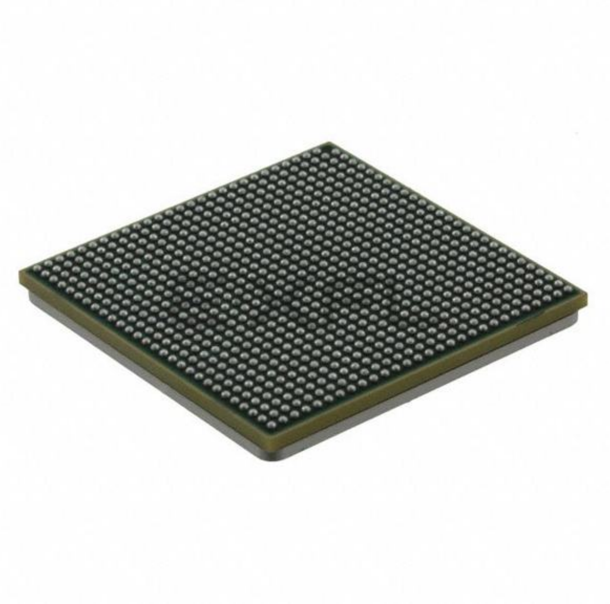

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8545hxatg

4.3 eTSEC Gigabit Reference Clock Timing

The following table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

Table 6. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TV_{DD} = 3.3 V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock TSEC*n*_GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_ GTX_CLK. See Section 8.2.6, “RGMII and RTBI AC Timing Specifications,” for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCI*n*_CLK. The following table provides the PCI/PCI-X reference clock AC timing specifications for the device.

Table 7. PCI*n*_CLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
PCI*n*_CLK frequency	f_{PCICLK}	16	—	133	MHz	—
PCI*n*_CLK cycle time	t_{PCICLK}	7.5	—	60	ns	—
PCI*n*_CLK rise and fall time	t_{PCIKH}, t_{PCIKL}	0.6	1.0	2.1	ns	1, 2
PCI*n*_CLK duty cycle	$t_{PCIKHKL}/t_{PCICLK}$	40	—	60	%	2

Notes:

1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
2. Timing is guaranteed by design and characterization.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	 1.48 1.95 2.40	 — — —	ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	 1.48 1.95 2.40	 — — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	 1.48 1.95 2.40	 — — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCX}	 1.48 1.95 2.40	 — — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDS}, t_{DDKLDS}	 538 700 900	 — — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDX}, t_{DDKLDX}	 538 700 900	 — — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Figure 11 shows the MII transmit AC timing diagram.

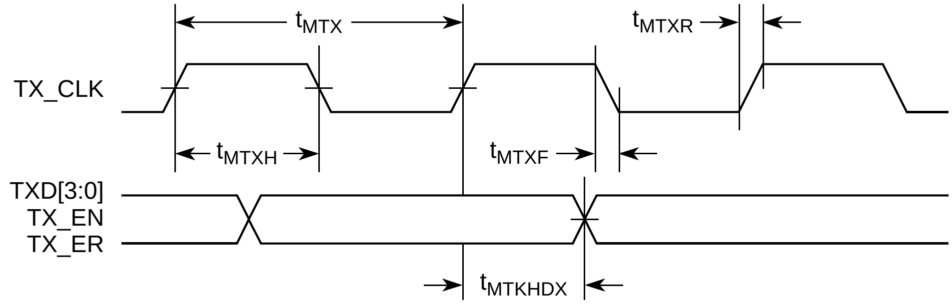

Figure 11. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

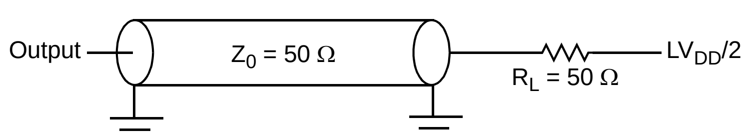

Figure 12. eTSEC AC Test Load

Figure 15 shows the TBI receive AC timing diagram.

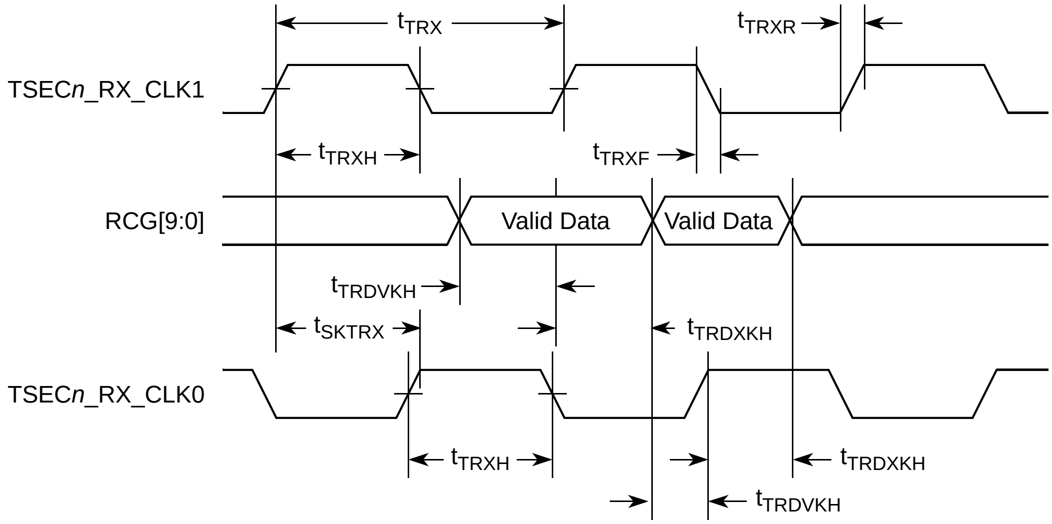

Figure 15. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Table 32. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	$t_{TRRH/TRRX}$	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	—	—	ns

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC).""

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 36. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN}[1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t_{MDC}	120.5	—	1389	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	16 × t_{CCB}	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	(16 × t_{CCB}× 8) – 3	—	(16 × t_{CCB} × 8) + 3	ns	5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4

10.2 Local Bus AC Electrical Specifications

This table describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus, see Section 20.1, “Clock Ranges.”

Table 40. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[*n*]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 2	20 10	ns	5
Output hold times: Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	30 30	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.

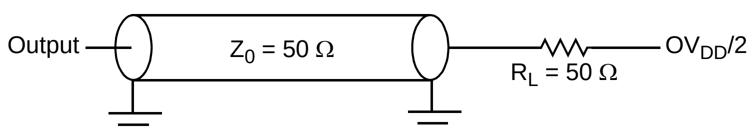

Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.

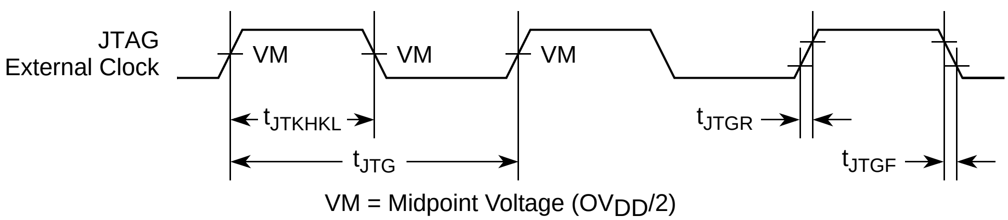

Figure 30. JTAG Clock Input Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the device.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 45. I²C DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	0.7 × OV_{DD}	OV_{DD} + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × OV_{DD}	V	—
Low level output voltage	V_{OL}	0	0.2 × OV_{DD}	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. See the *MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual*, for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 46. I²C AC Electrical Specifications

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	—
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	4
High period of the SCL clock	t_{I2CH}	0.6	—	μs	4
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	4
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	4
Data setup time	t_{I2DVKH}	100	—	ns	4
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	2
Data output delay time:	t_{I2OVKL}	—	0.9	—	3
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

Table 46. I^2C AC Electrical Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I^2C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I^2C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I^2C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I^2C source clock frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR bit setting	0x2A	0x05	0x26	0x00
Actual FDR divider selected	896	704	512	384
Actual I^2C SCL frequency generated	371 kHz	378 kHz	390 kHz	346 kHz

   For the detail of I^2C frequency calculation, see *Determining the I^2C Frequency Divider Ratio for SCL* (AN2919). Note that the I^2C source clock frequency is half of the CCB clock frequency for the device.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 33 provides the AC test load for the I^2C.

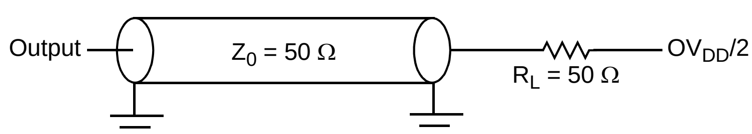

Figure 33. I^2C AC Test Load

Figure 36 shows the PCI/PCI-X input AC timing conditions.

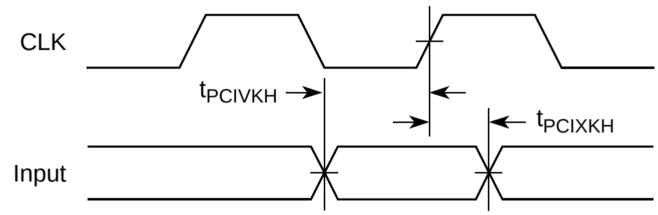

Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.

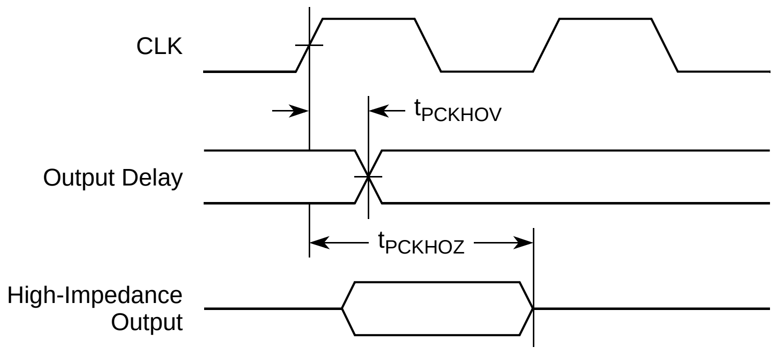

Figure 37. PCI/PCI-X Output AC Timing Measurement Condition

Table 53 provides the PCI-X AC timing specifications at 66 MHz.

Table 53. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV_{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV_{DD}	—
LA[27]	H21	O	BV_{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV_{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	O	BV_{DD}	—
LCS5/DMA_DREQ2	D23	I/O	BV_{DD}	1
LCS6/DMA_DACK2	G20	O	BV_{DD}	1
LCS7/DMA_DDONE2	E21	O	BV_{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	O	BV_{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	O	BV_{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	O	BV_{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	O	BV_{DD}	5, 9
LALE	H24	O	BV_{DD}	5, 8, 9
LBCTL	G27	O	BV_{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV_{DD}	5, 9
LGPL1/LSDWE	G22	O	BV_{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	O	BV_{DD}	5, 8, 9
LGPL3/LSDCAS	F24	O	BV_{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV_{DD}	—
LGPL5	E26	O	BV_{DD}	5, 9
LCKE	E24	O	BV_{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV_{DD}	—
LSYNC_IN	F27	I	BV_{DD}	—
LSYNC_OUT	F28	O	BV_{DD}	—
DMA				
DMA_DACK[0:1]	AD3, AE1	O	OV_{DD}	5, 9, 107
DMA_DREQ[0:1]	AD4, AE2	I	OV_{DD}	—
DMA_DDONE[0:1]	AD2, AD1	O	OV_{DD}	—
Programmable Interrupt Controller				
UDE	AH16	I	OV_{DD}	—
MCP	AG19	I	OV_{DD}	—

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PCI1\_FRAME}}$	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ64}}$/$\overline{\text{PCI2\_FRAME}}$	AF14	I/O	OV_{DD}	2, 5, 10
$\overline{\text{PCI1\_ACK64}}$/$\overline{\text{PCI2\_DEVSEL}}$	V15	I/O	OV_{DD}	2
PCI2_CLK	AE28	I	OV_{DD}	39
$\overline{\text{PCI2\_IRDY}}$	AD26	I/O	OV_{DD}	2
$\overline{\text{PCI2\_PERR}}$	AD25	I/O	OV_{DD}	2
$\overline{\text{PCI2\_GNT}}$[4:1]	AE26, AG24, AF25, AE25	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI2\_GNT0}}$	AG25	I/O	OV_{DD}	—
$\overline{\text{PCI2\_SERR}}$	AD24	I/O	OV_{DD}	2,4
$\overline{\text{PCI2\_STOP}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI2\_TRDY}}$	AD27	I/O	OV_{DD}	2
$\overline{\text{PCI2\_REQ}}$[4:1]	AD28, AE27, W17, AF26	I	OV_{DD}	—
$\overline{\text{PCI2\_REQ0}}$	AH25	I/O	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV_{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11
Clock				
RTC	AF16	I	OV_{DD}	—
SYSCLK	AH17	I	OV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
TEST_SEL	AH14	I	OV_{DD}	109
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	O	AVDD_SRDS	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 85. Package Thermal Characteristics for FC-PBGA (continued)

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-board	N/A	$R_{\theta JB}$	5	°C/W	3
Die junction-to-case	N/A	$R_{\theta JC}$	0.8	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed-circuit board is the recommended procedure using a maximum of 10 lbs force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

22 System Design Information

This section provides electrical design recommendations for successful application of the device.

22.1 System Clocking

This device includes five PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 20.2, “CCB/SYSCLK PLL Ratio.”
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 20.3, “e500 Core PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus.
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS, respectively). The AV_{DD}

Table 87. Part Numbering Nomenclature (continued)

MPC	*nnnnn*	*t*	*pp*	*ff*	*c*	*r*
Product Code	**Part Identifier**	**Temperature**	**Package**[1, 2, 3]	**Processor Frequency**[4]	**Core Frequency**	**Silicon Version**
MPC	8545E	Blank = 0 to 105°C C = –40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Notes:
1. See Section 19, “Package Description,” for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	• Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. • Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." • Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. • Removed Note from Section 5.1, "Power-On Ramp Rate". • Changed the Table 10 title to "Power Supply Ramp Rate". • Removed table 11. • Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. • Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" • Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. • Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)[1]" from 4 and 25 to 2 and 10 respectively .
8	04/2011	• Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." • Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. • Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	• In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." • Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	• In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. • In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. • In Table 13 deleted ramp rate requirement for XVDD/SVDD. • In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. • In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	• In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. • Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." • Added a reference to Revision 2.1.2. • Updated Table 55, "MII Management AC Timing Specifications." • Added Section 5.1, "Power-On Ramp Rate."