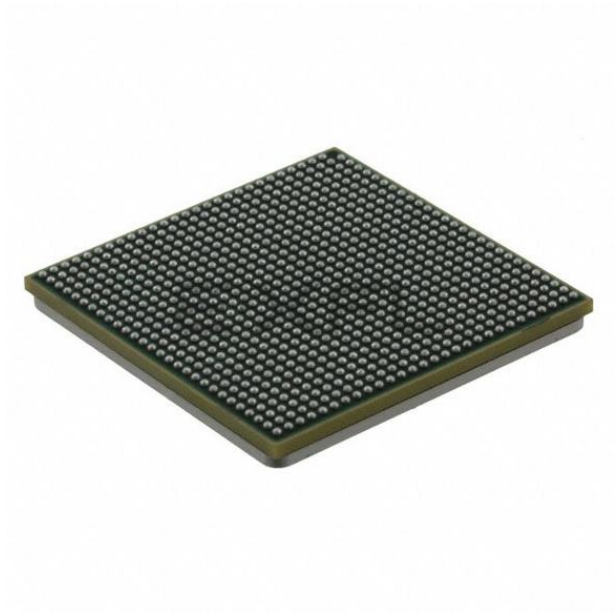

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8547ehxaqg |

  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

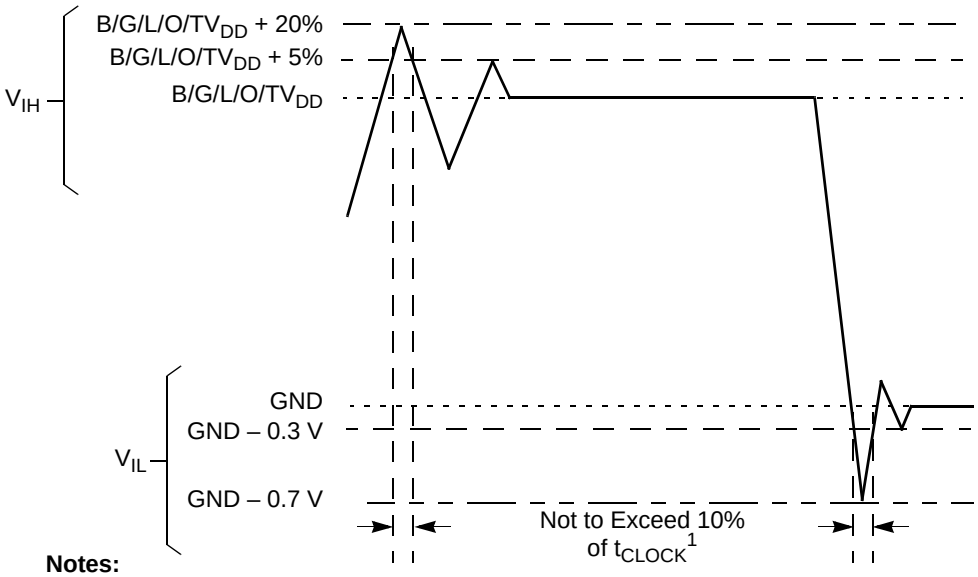
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  - PCI 2.2 and PCI-X 1.0 compatible
  - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming

**Table 2. Recommended Operating Conditions (continued)**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Junction temperature range | Tj | 0 to 105 | °C | — |

**Notes:**
1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the $AV_{DD}$ pin, which may be reduced from $V_{DD}$ by the filter.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $L/TV_{IN}$ must not exceed $L/TV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.




**Notes:**
1. $t_{CLOCK}$ refers to the clock period associated with the respective interface:
   For $I^2C$ and JTAG, $t_{CLOCK}$ references SYSCLK.
   For DDR, $t_{CLOCK}$ references MCLK.
   For eTSEC, $t_{CLOCK}$ references EC_GTX_CLK125.
   For LBIU, $t_{CLOCK}$ references LCLK.
   For PCI, $t_{CLOCK}$ references PCI*n*_CLK or SYSCLK.
   For SerDes, $t_{CLOCK}$ references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$**

The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied $MV_{REF}$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that $GV_{DD}$(typ) = 2.5 V for DDR SDRAM, and $GV_{DD}$(typ) = 1.8 V for DDR2 SDRAM.

## 6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when $GV_{DD}$(typ) = 1.8 V.

**Table 11. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF} - 0.04$ | $MV_{REF} + 0.04$ | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF} + 0.125$ | $GV_{DD} + 0.3$ | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF} - 0.125$ | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $V_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to $0.5 \times GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$. This rail must track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when $GV_{DD}$(typ) = 1.8 V.

**Table 12. DDR2 SDRAM Capacitance for $GV_{DD}$(typ)=1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT} = GV_{DD}/2$, $V_{OUT}$ (peak-to-peak) = 0.2 V.

# 8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 22. GMII, MII, RMII, and TBI DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$<br>$TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1, 2, 3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | — |

**Notes:**
1. $LV_{DD}$ supports eTSECs 1 and 2.
2. $TV_{DD}$ supports eTSECs 3 and 4.
3. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2.

A summary of the FIFO AC specifications appears in Table 24 and Table 25.

**Table 24. FIFO Mode Transmit AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK | $t_{FITDV}$ | 2.0 | — | — | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$ | 0.5 | — | 3.0 | ns |

**Table 25. FIFO Mode Receive AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{FIR}$ | 5.3 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIR}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

**Note:**
1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of t he speed bins the part belongs to as well as the FIFO mode under operation. See Section 4.5, “Platform to FIFO Restrictions.”

Timing diagrams for FIFO appear in Figure 6 and Figure 7.

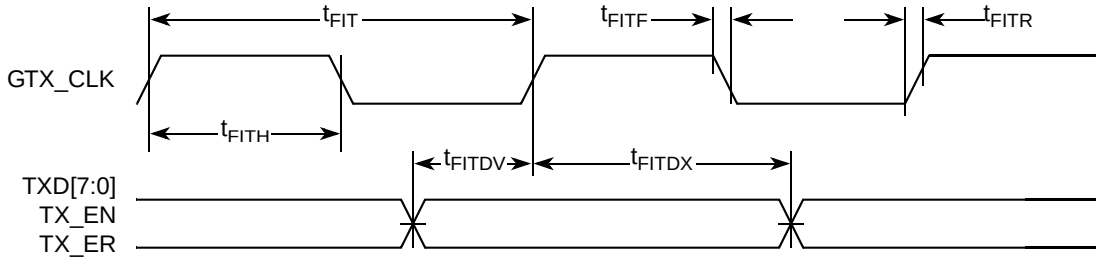



**Figure 6. FIFO Transmit AC Timing Diagram**

Figure 10 shows the GMII receive AC timing diagram.

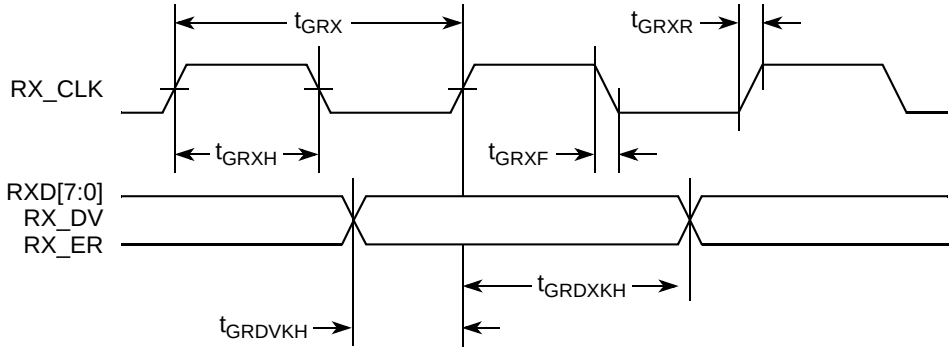



**Figure 10. GMII Receive AC Timing Diagram**

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

**Table 28. MII Transmit AC Timing Specifications**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$[2] | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%–80%) | $t_{MTXR}$[2] | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%–20%) | $t_{MTXF}$[2] | 1.0 | — | 4.0 | ns |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 11 shows the MII transmit AC timing diagram.

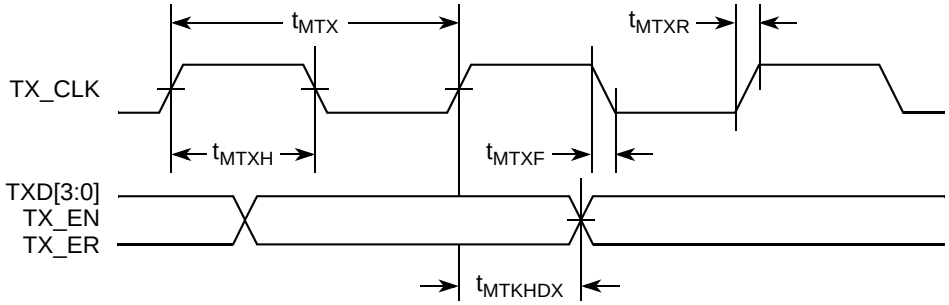



**Figure 11. MII Transmit AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

**Table 29. MII Receive AC Timing Specifications**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$[2] | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise (20%–80%) | $t_{MRXR}$[2] | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%–20%) | $t_{MRXF}$[2] | 1.0 | — | 4.0 | ns |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

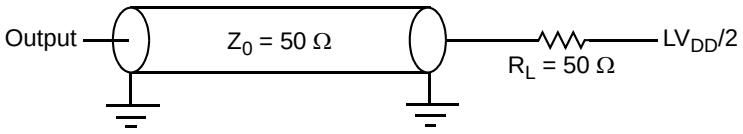



**Figure 12. eTSEC AC Test Load**

**Table 34. RMII Transmit AC Timing Specifications (continued)**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 1.0 | — | 10.0 | ns |

**Note:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 18 shows the RMII transmit AC timing diagram.

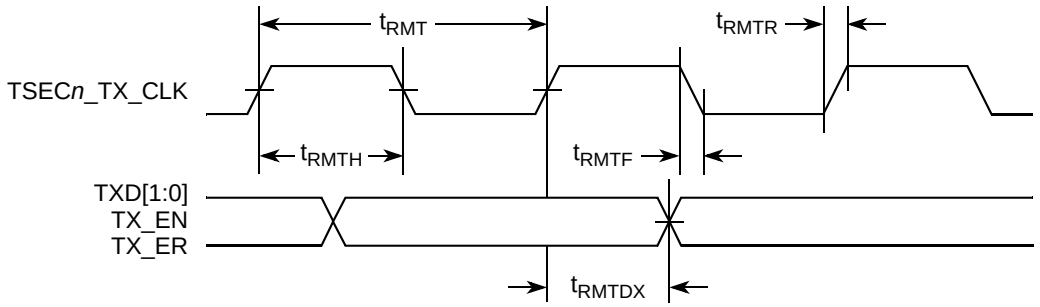



**Figure 18. RMII Transmit AC Timing Diagram**

### 8.2.7.2 RMII Receive AC Timing Specifications

**Table 35. RMII Receive AC Timing Specifications**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSEC*n*_TX_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| TSEC*n*_TX_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % |
| TSEC*n*_TX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSEC*n*_TX_CLK(20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSEC*n*_TX_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns |

**Note:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

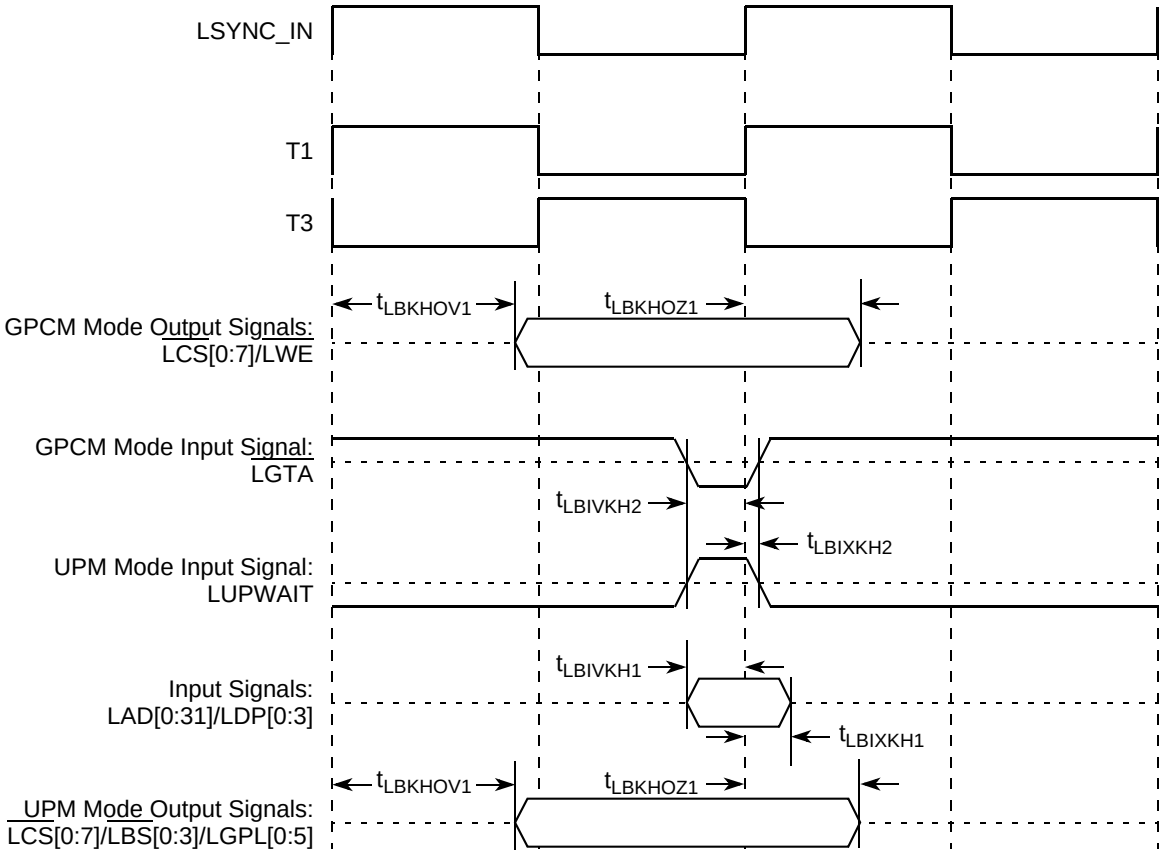



**Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)**

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out}$ = $V_{SD\_TX}$ + $V_{\overline{SD\_TX}}$ = (A + B)/2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.

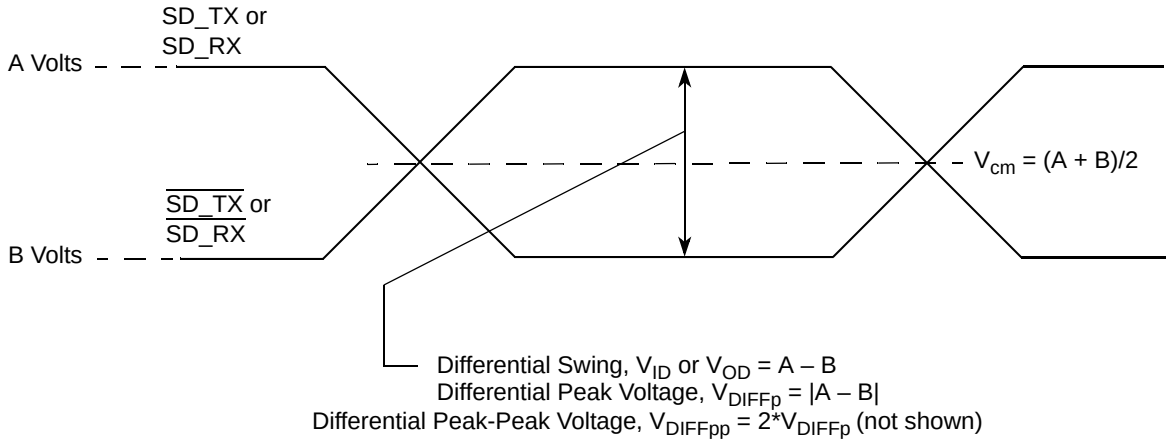



**Figure 38. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mVp-p.

## 16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

### 16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD\_SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

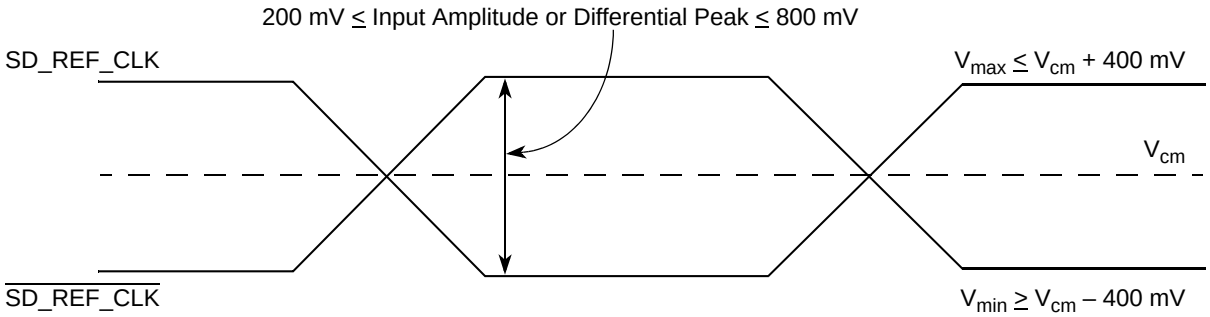



**Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

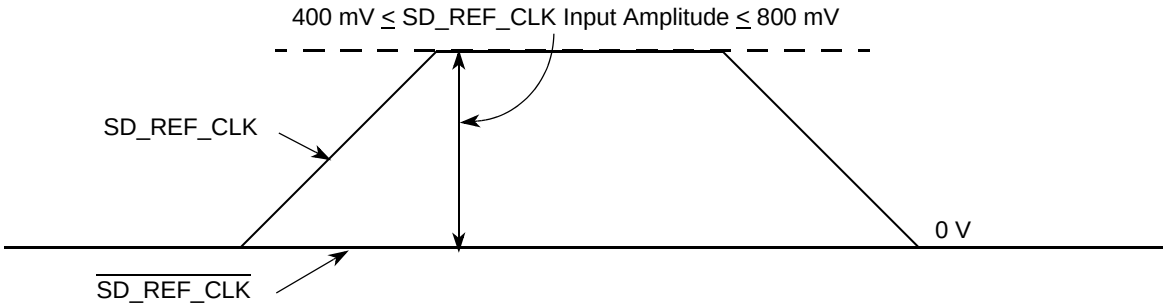



**Figure 42. Single-Ended Reference Clock Input DC Requirements**

## 16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

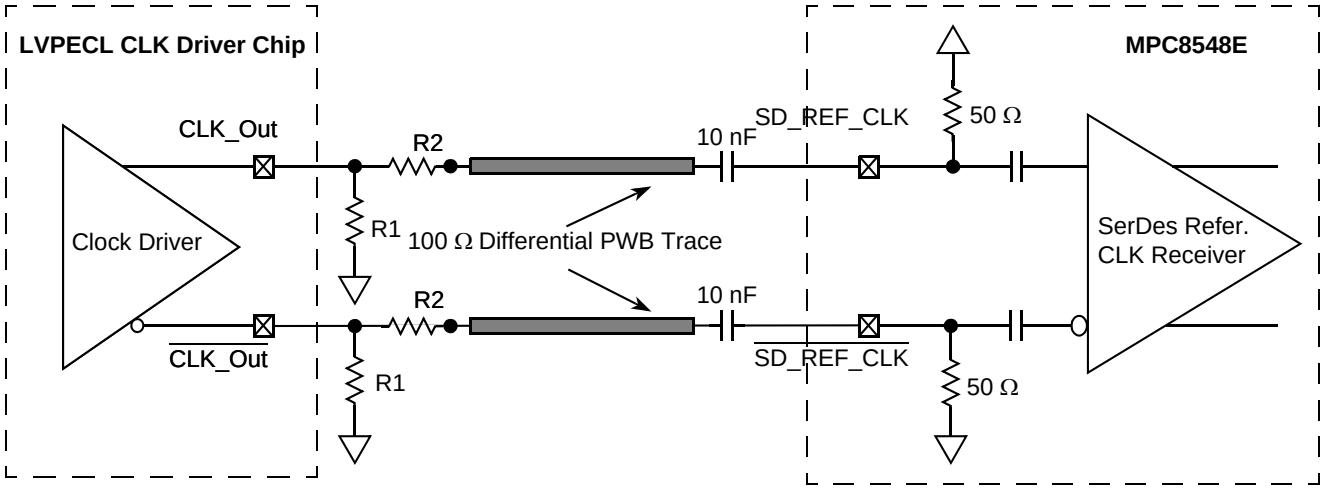



**Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.

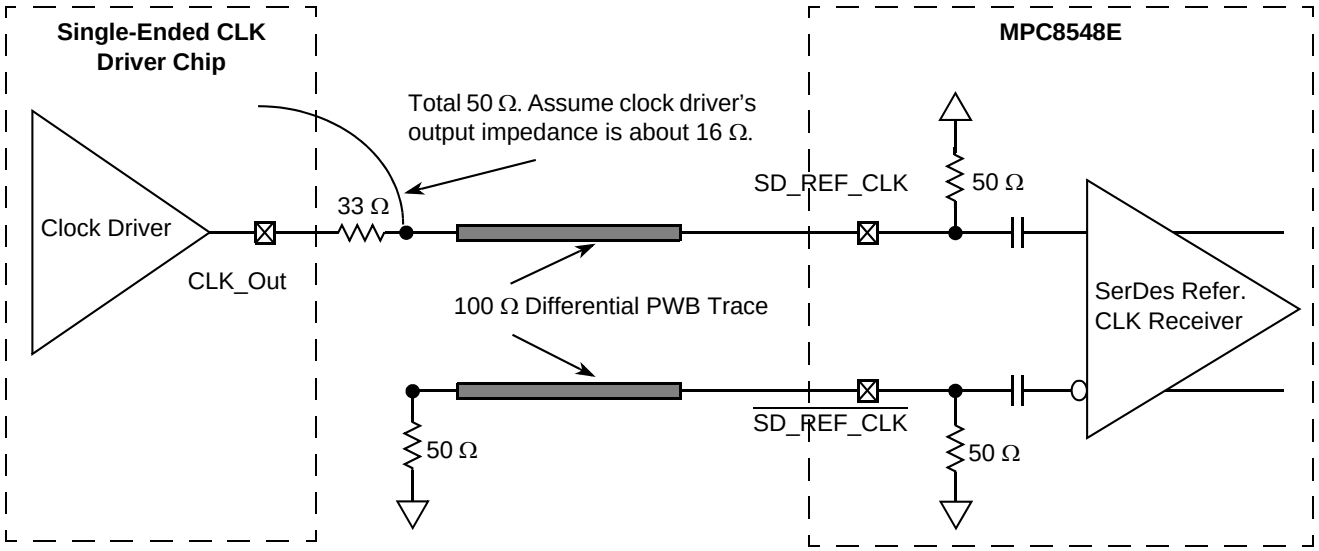



**Figure 46. Single-Ended Connection (Reference Only)**

## 18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B volts.
2. The differential output signal of the transmitter, $V_{OD}$, is defined as $V_{TD} - V_{\overline{TD}}$.
3. The differential input signal of the receiver, $V_{ID}$, is defined as $V_{RD} - V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

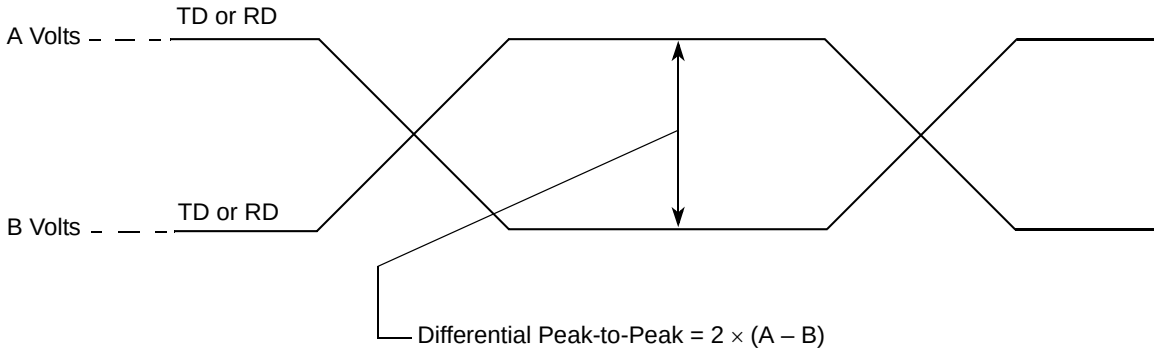



**Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mVp-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

## 18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

**Notes:**

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

## 19.3 Pinout Listings

**NOTE**

The $\overline{\text{DMA\_DACK}}$[0:1] and TEST_SEL/$\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on PCI1_AD[63:32]/PC2_AD[31:0] pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

**Table 71. MPC8548E Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 and PCI2 (One 64-Bit or Two 32-Bit)** | | | | |
| PCI1_AD[63:32]/PCI2_AD[31:0] | AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24 | I/O | $OV_{DD}$ | 17 |
| PCI1_AD[31:0] | AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{\text{BE}}$[7:4]/PCI2_C_$\overline{\text{BE}}$[3:0] | AF15, AD14, AE15, AD15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{\text{BE}}$[3:0] | AF9, AD11, Y12, Y13 | I/O | $OV_{DD}$ | 17 |
| PCI1_PAR64/PCI2_PAR | W15 | I/O | $OV_{DD}$ | |
| $\overline{\text{PCI1\_GNT}}$[4:1] | AG6, AE6, AF5, AH5 | O | $OV_{DD}$ | 5, 9, 35 |
| $\overline{\text{PCI1\_GNT0}}$ | AG5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_IRDY}}$ | AF11 | I/O | $OV_{DD}$ | 2 |
| PCI1_PAR | AD12 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI1\_PERR}}$ | AC12 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1\_SERR}}$ | V13 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI1\_STOP}}$ | W12 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI1\_TRDY}}$ | AG11 | I/O | $OV_{DD}$ | 2 |

**Table 71. MPC8548E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| PCI1_REQ[4:1] | AH2, AG4, AG3, AH4 | I | $OV_{DD}$ | — |
| | | | | — |
| | | | | — |
| | | | | — |
| | | | | — |
| PCI1_REQ0 | AH3 | I/O | $OV_{DD}$ | — |
| PCI1_CLK | AH26 | I | $OV_{DD}$ | 39 |
| PCI1_DEVSEL | AH11 | I/O | $OV_{DD}$ | 2 |
| PCI1_FRAME | AE11 | I/O | $OV_{DD}$ | 2 |
| PCI1_IDSEL | AG9 | I | $OV_{DD}$ | — |
| PCI1_REQ64/PCI2_FRAME | AF14 | I/O | $OV_{DD}$ | 2, 5, 10 |
| PCI1_ACK64/PCI2_DEVSEL | V15 | I/O | $OV_{DD}$ | 2 |
| PCI2_CLK | AE28 | I | $OV_{DD}$ | 39 |
| PCI2_IRDY | AD26 | I/O | $OV_{DD}$ | 2 |
| PCI2_PERR | AD25 | I/O | $OV_{DD}$ | 2 |
| PCI2_GNT[4:1] | AE26, AG24, AF25, AE25 | O | $OV_{DD}$ | 5, 9, 35 |
| PCI2_GNT0 | AG25 | I/O | $OV_{DD}$ | — |
| PCI2_SERR | AD24 | I/O | $OV_{DD}$ | 2, 4 |
| PCI2_STOP | AF24 | I/O | $OV_{DD}$ | 2 |
| PCI2_TRDY | AD27 | I/O | $OV_{DD}$ | 2 |
| PCI2_REQ[4:1] | AD28, AE27, W17, AF26 | I | $OV_{DD}$ | — |
| PCI2_REQ0 | AH25 | I/O | $OV_{DD}$ | — |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | H13, F13, F11, C11, J13, G13, D12, M12 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | M17, C16, K17, E16, B6, C4, H4, K1, E13 | O | $GV_{DD}$ | — |
| MDQS[0:8] | M15, A16, G17, G14, A5, D3, H1, L2, C13 | I/O | $GV_{DD}$ | — |
| MDQS[0:8] | L17, B16, J16, H14, C6, C2, H3, L4, D13 | I/O | $GV_{DD}$ | — |
| MA[0:15] | A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11 | O | $GV_{DD}$ | — |
| MBA[0:2] | F7, J7, M11 | O | $GV_{DD}$ | — |

**Table 71. MPC8548E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| SENSEVSS | M16 | — | — | 13 |
| **Analog Signals** | | | | |
| MVREF | A18 | I Reference voltage signal for DDR | MVREF | — |
| SD_IMP_CAL_RX | L28 | I | 200Ω to GND | — |
| SD_IMP_CAL_TX | AB26 | I | 100Ω to GND | — |
| SD_PLL_TPA | U26 | O | — | 24 |

**Notes:**

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to $OV_{DD}$.
3. A valid clock must be provided at POR if TSEC4_TXD[2] is set = 1.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, “CCB/SYSCLK PLL Ratio.”
8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the $V_{DD}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections must be made to these pins if they are not used.
16. These pins are not connected for any use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to $OV_{DD}$ when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI1\_C\_BE}}$[7:4]).
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx flow control.
24. Do not connect.

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{UDE}}$ | AH16 | I | $OV_{DD}$ | — |
| $\overline{\text{MCP}}$ | AG19 | I | $OV_{DD}$ | — |
| IRQ[0:7] | AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20 | I | $OV_{DD}$ | — |
| IRQ[8] | AF19 | I | $OV_{DD}$ | — |
| IRQ[9]/$\overline{\text{DMA\_DREQ3}}$ | AF21 | I | $OV_{DD}$ | 1 |
| IRQ[10]/$\overline{\text{DMA\_DACK3}}$ | AE19 | I/O | $OV_{DD}$ | 1 |
| IRQ[11]/$\overline{\text{DMA\_DDONE3}}$ | AD20 | I/O | $OV_{DD}$ | 1 |
| $\overline{\text{IRQ\_OUT}}$ | AD18 | O | $OV_{DD}$ | 2, 4 |
| **Ethernet Management Interface** | | | | |
| EC_MDC | AB9 | O | $OV_{DD}$ | 5, 9 |
| EC_MDIO | AC8 | I/O | $OV_{DD}$ | — |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | V11 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_RXD[7:0] | R5, U1, R3, U2, V3, V1, T3, T2 | I | $LV_{DD}$ | — |
| TSEC1_TXD[7:0] | T10, V7, U10, U5, U4, V6, T5, T8 | O | $LV_{DD}$ | 5, 9 |
| TSEC1_COL | R4 | I | $LV_{DD}$ | — |
| TSEC1_CRS | V5 | I/O | $LV_{DD}$ | 20 |
| TSEC1_GTX_CLK | U7 | O | $LV_{DD}$ | — |
| TSEC1_RX_CLK | U3 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | V2 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | T1 | I | $LV_{DD}$ | — |
| TSEC1_TX_CLK | T6 | I | $LV_{DD}$ | — |
| TSEC1_TX_EN | U9 | O | $LV_{DD}$ | 30 |
| TSEC1_TX_ER | T7 | O | $LV_{DD}$ | — |
| GPIN[0:7] | P2, R2, N1, N2, P3, M2, M1, N3 | I | $LV_{DD}$ | 103 |
| GPOUT[0:5] | N9, N10, P8, N7, R9, N5 | O | $LV_{DD}$ | — |
| cfg_dram_type0/GPOUT6 | R8 | O | $LV_{DD}$ | 5, 9 |
| GPOUT7 | N6 | O | $LV_{DD}$ | — |
| Reserved | P1 | — | — | 104 |
| Reserved | R6 | — | — | 104 |
| Reserved | P6 | — | — | 15 |
| Reserved | N4 | — | — | 105 |

**Table 85. Package Thermal Characteristics for FC-PBGA (continued)**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Die junction-to-board | N/A | $R_{\theta JB}$ | 5 | °C/W | 3 |
| Die junction-to-case | N/A | $R_{\theta JC}$ | 0.8 | °C/W | 4 |

**Notes:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

## 21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed-circuit board is the recommended procedure using a maximum of 10 lbs force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

# 22 System Design Information

This section provides electrical design recommendations for successful application of the device.

## 22.1 System Clocking

This device includes five PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 20.2, “CCB/SYSCLK PLL Ratio.”
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 20.3, “e500 Core PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus.
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.

## 22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_PLAT, $AV_{DD}$_CORE, $AV_{DD}$_PCI, $AV_{DD}$_LBIU, and $AV_{DD}$_SRDS, respectively). The $AV_{DD}$

## 22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

### 22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to $XV_{DD}$. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

### 22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK