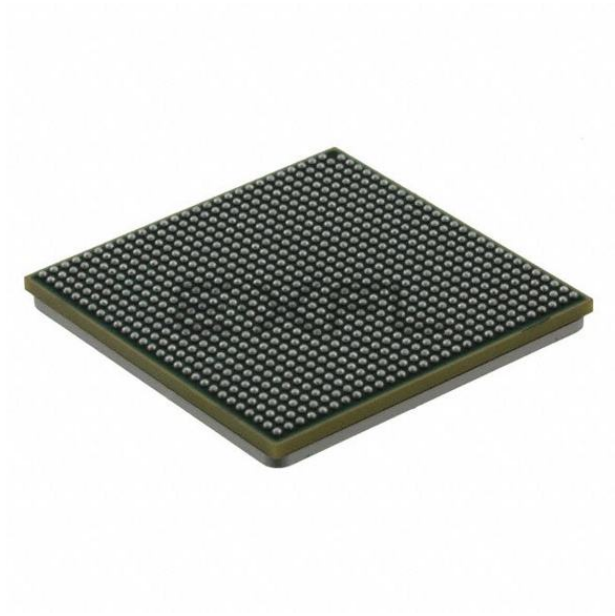

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8547evuaqg

  - Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers designed to comply with IEEE Std. 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

Table 4. Device Power Dissipation

CCB Frequency[1]	Core Frequency	SLEEP[2]	Typical-65[3]	Typical-105[4]	Maximum[5]	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on V_{DD} = 1.1 V, T_j = 65°C.
3. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65°C, running Dhrystone.
4. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105°C, running Dhrystone.
5. Maximum is based on V_{DD} = 1.1 V, T_j = 105°C, running a smoke test.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that GV_{DD}(typ) = 2.5 V for DDR SDRAM, and GV_{DD}(typ) = 1.8 V for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Figure 4 shows the DDR SDRAM output timing diagram.+

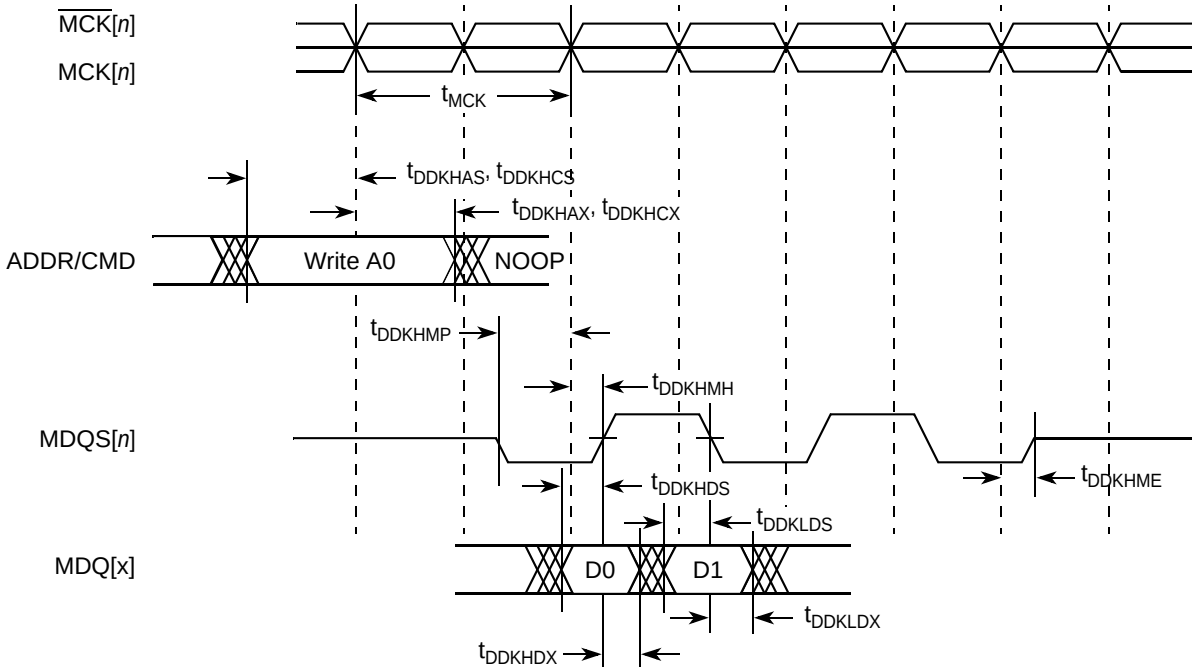

Figure 4. DDR SDRAM Output Timing Diagram

Figure 5 provides the AC test load for the DDR bus.

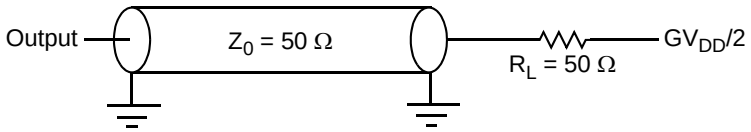

Figure 5. DDR AC Test Load

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND –0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/UPWAIT)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

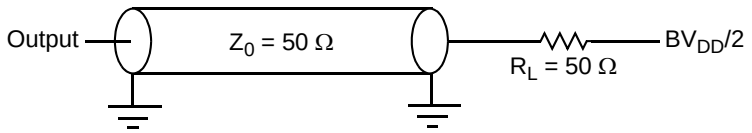

Figure 22. Local Bus AC Test Load

— The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.

— For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

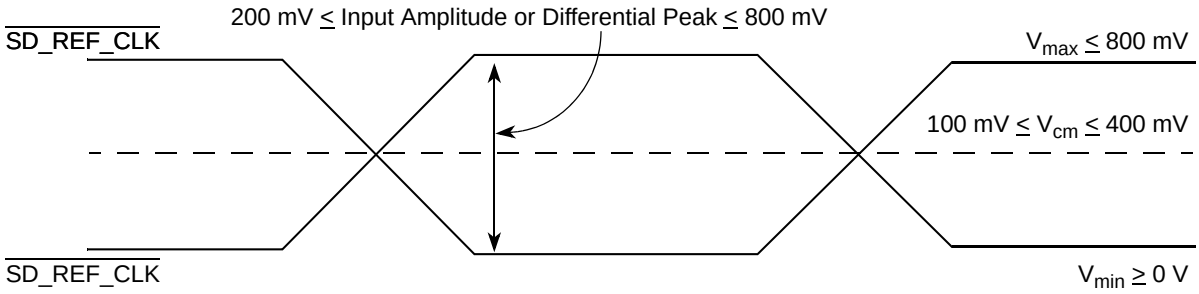

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, “AC Requirements for PCI Express SerDes Clocks”
- Section 18.2, “AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK”

16.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are designed to work with a spread spectrum clock (+0% to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane’s transmitter and receiver.

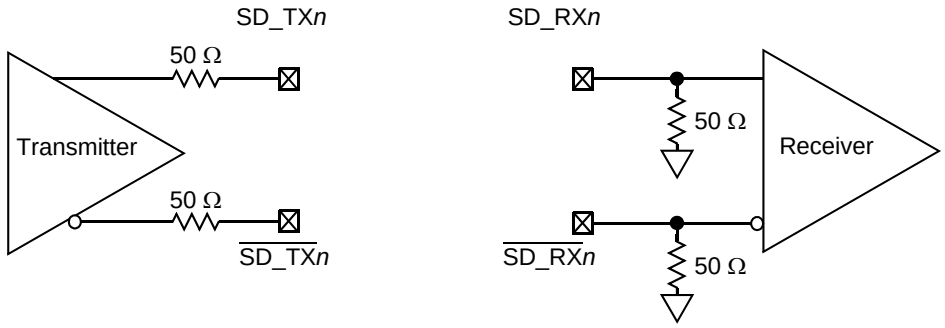

Figure 47. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, “PCI Express”
- Section 18, “Serial RapidIO”

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-}\rvert$. See Note 2.
$V_{TX-DE-RATIO}$	De- emphasized differential output voltage (ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = RMS(\lvert V_{TXD+} + V_{TXD-}\rvert/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$\lvert V_{TX-CM-DC\ (during\ L0)} + V_{TX-CM-Idle-DC\ (during\ electrical\ idle)}\rvert \le 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D–	0	—	25	mV	$\lvert V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\rvert \le 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\lvert V_{TX-D+}\rvert$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\lvert V_{TX-D-}\rvert$. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\rvert \le 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100-Ω ± 5% differential resistive load.

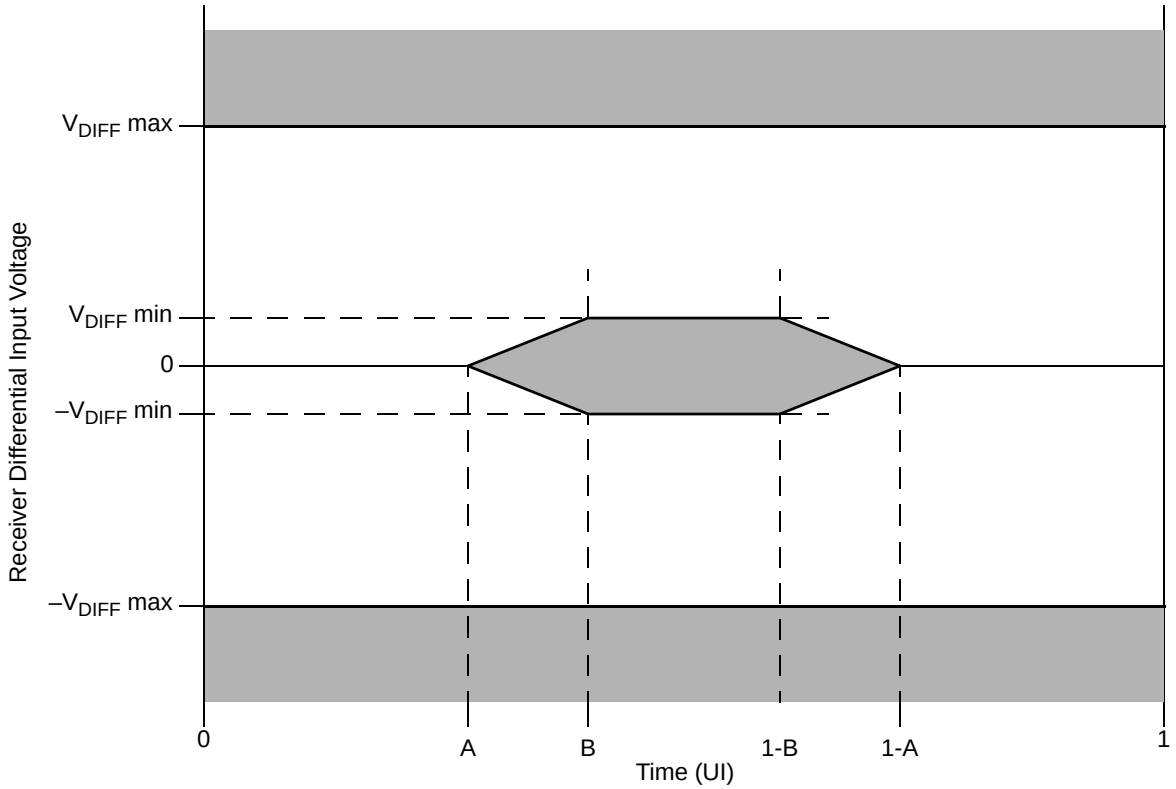

Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

19.3 Pinout Listings

NOTE

The $\overline{\text{DMA\_DACK}}$[0:1] and TEST_SEL/$\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on PCI1_AD[63:32]/PC2_AD[31:0] pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

Table 71. MPC8548E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[7:4]/PCI2_C_$\overline{\text{BE}}$[3:0]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV_{DD}	
$\overline{\text{PCI1\_GNT}}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1\_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1\_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_TRDY}}$	AG11	I/O	OV_{DD}	2

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV_{DD}	5, 9, 33
TSEC2_COL	P1	I	LV_{DD}	—
TSEC2_CRS	R6	I/O	LV_{DD}	20
TSEC2_GTX_CLK	P6	O	LV_{DD}	
TSEC2_RX_CLK	N4	I	LV_{DD}	—
TSEC2_RX_DV	P5	I	LV_{DD}	—
TSEC2_RX_ER	R1	I	LV_{DD}	—
TSEC2_TX_CLK	P10	I	LV_{DD}	—
TSEC2_TX_EN	P7	O	LV_{DD}	30
TSEC2_TX_ER	R10	O	LV_{DD}	5, 9, 33
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
Three-Speed Ethernet Controller (Gigabit Ethernet 4)				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	1
TSEC4_GTX_CLK	AA5	O	TV_{DD}	—
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV_{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV_{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV_{DD}	1, 30
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—
MDIC[0:1]	A19, B19	I/O	GV_{DD}	36

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FIFO1_RXC2	P5	I	LV_{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV_{DD}	15
cfg_dram_type1	R10	I	LV_{DD}	5
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV_{DD}	—
TSEC3_CRS	AA3	I/O	TV_{DD}	31
TSEC3_TX_ER	AB6	O	TV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:3]	M27, N25, P27, R25	I	XV_{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	O	XV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV_{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
PCI1_REQ0	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
PCI1_DEVSEL	AH11	I/O	OV_{DD}	2
PCI1_FRAME	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
cfg_pci1_width	AF14	I/O	OV_{DD}	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV_{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV_{DD}	15
cfg_dram_type1	R10	O	LV_{DD}	5, 9
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV_{DD}	—
TSEC3_CRS	AA3	I/O	TV_{DD}	31
TSEC3_TX_ER	AB6	O	TV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V,2.5 V)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	04/2008	• Removed 1:1 support on Table 82, “e500 Core to CCB Clock Ratio.” • Removed MDM from Table 18, “DDR SDRAM Input AC Timing Specifications.” MDM is an Output. • Figure 57, “PLL Power Supply Filter Circuit with PLAT Pins” (AVDD_PLAT). • Figure 58, “PLL Power Supply Filter Circuit with CORE Pins” (AVDD_CORE). • Split Figure 59, “PLL Power Supply Filter Circuit with PCI/LBIU Pins,” (formerly called just “PLL Power Supply Filter Circuit”) into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	• Adjusted maximum SYSCLK frequency down in Table 5, “SYSCLK AC Timing Specifications” per device erratum GEN-13. • Clarified notes to Table 6, “EC_GTX_CLK125 AC Timing Specifications.” • Added Section 4.4, “PCI/PCI-X Reference Clock Timing.” • Clarified descriptions and added PCI/PCI-X to Table 9, “PLL Lock Times.” • Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, “DDR and DDR2 SDRAM.” • Clarified Note 4 of Table 19, “DDR SDRAM Output AC Timing Specifications.” • Clarified the reference clock used in Section 7.2, “DUART AC Electrical Specifications.” • Corrected V_{IH}(min) in Table 22, “GMII, MII, RMII, and TBI DC Electrical Characteristics.” • Corrected V_{IL}(max) in Table 23, “GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics.” • Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. • Corrected V_{IH}(min) in Table 36, “MII Management DC Electrical Characteristics.” • Corrected t_{MDC}(min) in Table 37, “MII Management AC Timing Specifications.” • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKH2}$, $t_{LBIXKH1}$, and $t_{LBIXKH2}$ in Table 40, “Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled” and Table 40, “Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled.” • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKL2}$, $t_{LBIXKH1}$, and $t_{LBIXKL2}$ in Table 42, “Local Bus Timing Parameters—PLL Bypassed.” Note that $t_{LBIVKL2}$ and $t_{LBIXKL2}$ were previously labeled $t_{LBIVKH2}$ and $t_{LBIXKH2}$. • Added LUPWAIT signal to Figure 23, “Local Bus Signals (PLL Enabled)” and Figure 24, “Local Bus Signals (PLL Bypass Mode).” • Added $\overline{\text{LGTA}}$ signal to Figure 25, Figure 26, Figure 27 and Figure 28. • Corrected LUPWAIT assertion in Figure 26 and Figure 28. • Clarified the PCI reference clock in Section 15.2, “PCI/PCI-X AC Electrical Specifications” • Added Section 17.1, “Package Parameters.” • Added PBGA thermal information in Section 21.2, “Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid.” • Updated.” • Updated Table 87, “Part Numbering Nomenclature.”
0	07/2007	• Initial Release

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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