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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8547evuatg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

Characteristic S Junction temperature range		Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	1
	45(default) 45(default)	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	
PCI signals	25	OV _{DD} = 3.3 V	2
	45(default)		
DDR signal	18 36 (half strength mode)	GV _{DD} = 2.5 V	3
DDR2 signal	18 36 (half strength mode)	GV _{DD} = 1.8 V	3
TSEC/10/100 signals	45	L/TV _{DD} = 2.5/3.3 V	
DUART, system control, JTAG	45	OV _{DD} = 3.3 V	—
12C	150	OV _{DD} = 3.3 V	_

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.

3. The drive strength of the DDR interface in half-strength mode is at $T_i = 105^{\circ}C$ and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

- 1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
- 2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

Power Characteristics

Power Characteristics 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Table 4. Device Power Dissipation

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on V_{DD} = 1.1 V, T_i = 65°C.

3. Typical-65 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 65^{\circ}\text{C}$, running Dhrystone. 4. Typical-105 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running Dhrystone. 5. Maximum is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running a smoke test.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t _{DDKHAS}	1.48 1.95 2.40		ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t ddkhax	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCS	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCX	1.48 1.95 2.40		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	^t DDKHDS, ^t DDKLDS	538 700 900	 	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	^t ddkhdx, ^t ddkldx	538 700 900		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	6

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OH} = -1.0 \text{ mA}$)	V _{OH}	2.00	LV _{DD} /TV _{DD} + 0.3	V	
Output low voltage ($LV_{DD}/TV_{DD} = Min$, I _{OL} = 1.0 mA)	V _{OL}	GND –0.3	0.40	V	
Input high voltage	V _{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	
Input low voltage	V _{IL}	-0.3	0.90	V	
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	Ι _{ΙΗ}	_	10	μA	1, 2, 3
Input low current (V _{IN} = GND)	۱ _{IL}	-15	_	μÂ	3

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. $\mathsf{TV}_{\mathsf{DD}}$ supports eTSECs 3 and 4.

3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

Enhanced Three-Speed Ethernet (eTSEC)

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH/TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}	_	_	250	ps
Rise time RX_CLK (20%–80%)	t _{TRRR}	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXKH}	1.0	_	_	ns

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	—	0.90	V
Input high current ($OV_{DD} = Max, V_{IN}^{1} = 2.1 V$)	I _{IH}	—	40	μA
Input low current ($OV_{DD} = Max, V_{IN} = 0.5 V$)	I _{IL}	-600	—	μΑ

Table 36. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t _{MDC}	120.5		1389	ns	—
MDC clock pulse width high	t _{MDCH}	32		—	ns	—
MDC to MDIO valid	t _{MDKHDV}	$16 \times t_{CCB}$		—	ns	5
MDC to MDIO delay	t _{MDKHDX}	(16 × t _{CCB} × 8) – 3		$(16 \times t_{\rm CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t _{MDDVKH}	5		—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0		—	ns	—
MDC rise time	t _{MDCR}	_	_	10	ns	4

PCI/PCI-X

Figure 36 shows the PCI/PCI-X input AC timing conditions.



Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.





Table 53 provides the PCI-X AC timing specifications at 66 MHz.

	Table 53	. PCI-X AC	Timing	Specifications	at 66	MHz
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Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV	_	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7		ns	1, 10
SYSCLK to output high impedance	t _{PCKHOZ}	-	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t _{PCIVKH}	1.7	_	ns	3, 5
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	10
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	11
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	11
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	9, 11
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	11

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
V _{TX-DIFFp-p}	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
V _{TX-DE-RATIO}	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T _{TX-EYE}	Minimum TX eye width	0.70	—	_	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
T _{TX-EYE-MEDIAN-to-} MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median.	_	_	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
T _{TX-RISE} , T _{TX-FALL}	D+/D-TX output rise/fall time	0.125	—	_	UI	See Notes 2 and 5.
V _{TX-CM-ACp}	RMS AC peak common mode output voltage	_	_	20	mV	$\begin{split} & V_{TX\text{-}CM\text{-}ACp} = RMS(V_{TXD\text{+}} + V_{TXD\text{-}} /2 - V_{TX\text{-}CM\text{-}DC}) \\ & V_{TX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } V_{TX\text{-}D\text{+}} + V_{TX\text{-}D\text{-}} /2. \\ & See Note 2. \end{split}$
V _{TX-CM-DC-ACTIVE-} IDLE-DELTA	Absolute delta of dc common mode voltage during L0 and electrical idle	0	_	100	mV	$\begin{split} V_{TX-CM-DC} & (during \ L0) + V_{TX-CM-Idle-DC} & (during \\ electrical \ idle) &\leq 100 \ mV \\ V_{TX-CM-DC} &= DC_{(avg)} \ of \ V_{TX-D+} + V_{TX-D-} /2 \ [L0] \\ V_{TX-CM-Idle-DC} &= DC_{(avg)} \ of \ V_{TX-D+} + V_{TX-D-} /2 \\ [electrical \ idle] \\ See \ Note \ 2. \end{split}$
VTX-CM-DC-LINE-DELTA	Absolute delta of DC common mode between D+ and D–	0	_	25	mV	$\begin{split} V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} &\leq 25 \text{ mV} \\ V_{TX-CM-DC-D+} &= DC_{(avg)} \text{ of } V_{TX-D+} \\ V_{TX-CM-DC-D-} &= DC_{(avg)} \text{ of } V_{TX-D-} . \\ \text{See Note 2.} \end{split}$
V _{TX} -IDLE-DIFFp	Electrical idle differential peak output voltage	0	_	20	mV	$\begin{split} & V_{\text{TX-IDLE-DIFFp}} = V_{\text{TX-IDLE-D+}} - V_{\text{TX-IDLE-D-}} \\ & \leq 20 \text{ mV.} \\ & \text{See Note 2.} \end{split}$
V _{TX-RCV-DETECT}	The amount of voltage change allowed during receiver detection		_	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Package Description

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_		2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 Ω to GND	
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	_
SD_PLL_TPA	U26	0		24

Table 73. MPC8545E Pinout Listing (continued)

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	_	_	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	0	OV _{DD}	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV _{DD}	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
Reserved	AF15, AD14, AE15, AD15	_	—	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
Reserved	W15	_	—	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V,2.5 V)	GV _{DD}	_
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	—
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	_
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	_
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV _{DD}	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	_	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	0	V _{DD}	13

Table 74. MPC8543E Pinout Listing (continued)

21 Thermal

This section describes the thermal specifications of the device.

21.1 Thermal for Version 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

This table shows the package thermal characteristics.

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	17	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	12	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	11	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	8	°C/W	1, 2
Die junction-to-board	N/A	R_{\thetaJB}	3	°C/W	3
Die junction-to-case	N/A	$R_{ extsf{ heta}JC}$	0.8	°C/W	4

Table 84. Package Thermal Characteristics for HiCTE FC-CBGA

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.2 Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid

This section describes the thermal specifications for the FC-PBGA package for revision 2.1.1, 2.1.2, and 3.0 silicon.

This table shows the package thermal characteristics.

Table 85. Package	Thermal	Characteristics	for FC-PBGA
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Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	18	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	9	°C/W	1, 2

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a $1-\mu F$ ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA_DACK[0:1], and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

• SD_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = $0xE_0F08$) (this prevents the oscillations and holds the receiver output in a fixed state) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

22.11 Guideline for PCI Interface Termination

PCI termination if PCI 1 or PCI 2 is not used at all.

Option 1

If PCI arbiter is enabled during POR:

- All AD pins are driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

If PCI arbiter is disabled during POR:

- All AD pins are in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following is the termination recommendation:

- For LDP[0:3]—tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE—tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

24 Document Revision History

The following table provides a revision history for this hardware specification.

Rev. Date Substantive Change(s) Number • Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and 9 02/2012 Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." • Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. Removed Note from Section 5.1. "Power-On Ramp Rate". • Changed the Table 10 title to "Power Supply Ramp Rate". • Removed table 11. • Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" • Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. • Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)¹" from 4 and 25 to 2 and 10 respectively . 8 04/2011 Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." • Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. • Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information. In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO 7 09/2010 delay tMDKHDX (16 x tptb_clk x 8) - 3 - (16 x tptb_clk x 8) + 3" to "MDC to MDIO delay tMDKHDX $(16 \times tCCB \times 8) - 3 - (16 \times tCCB \times 8) + 3."$ Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes. 6 12/2009 • In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. • In Table 13 deleted ramp rate requirement for XVDD/SVDD. In Table 13 footnote 1 changed voltage range of concern from 0-400 mV to 20-500mV. In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins. 5 10/2009 • In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX CLK duty cycle. Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." • Added a reference to Revision 2.1.2. • Updated Table 55, "MII Management AC Timing Specifications." Added Section 5.1, "Power-On Ramp Rate."

Table 88. Document Revision History