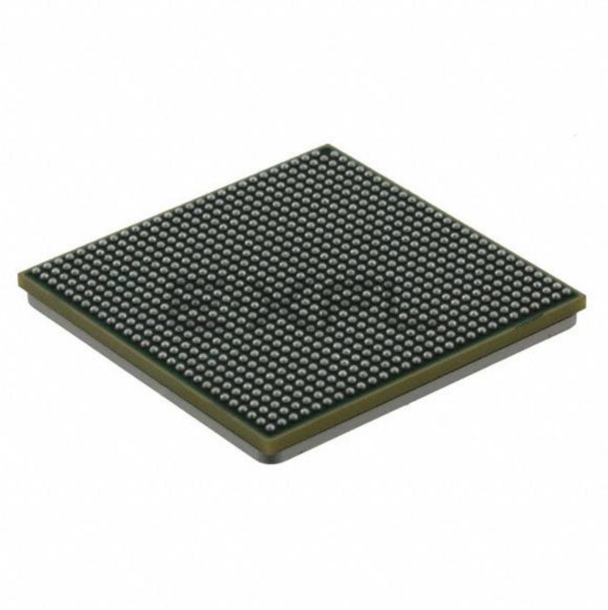
NXP USA Inc. - KMPC8547HXAQG Datasheet



Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8547hxaqg

  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency
- Serial RapidIO™ interface unit
  - Supports *RapidIO™ Interconnect Specification, Revision 1.2*
  - Both 1× and 4× LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
  - Auto detection of 1- and 4-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	1.48 1.95 2.40	— — —	ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCX}	1.48 1.95 2.40	— — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDS}, t_{DDKLDS}	538 700 900	— — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDX}, t_{DDKLDX}	538 700 900	— — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Figure 8 shows the GMII transmit AC timing diagram.

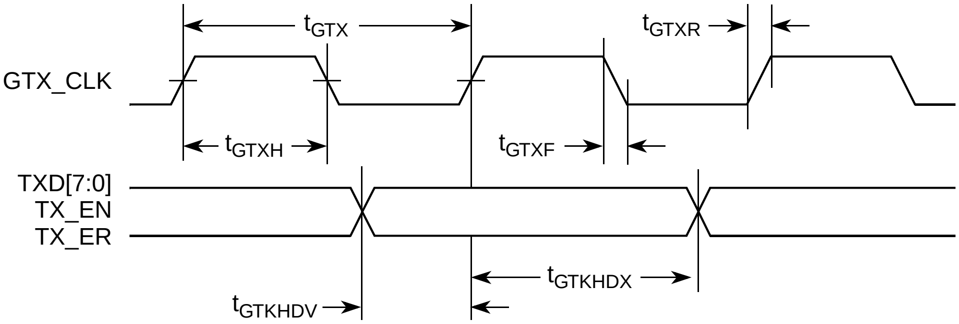


Figure 8. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}[2]	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9 provides the AC test load for eTSEC.

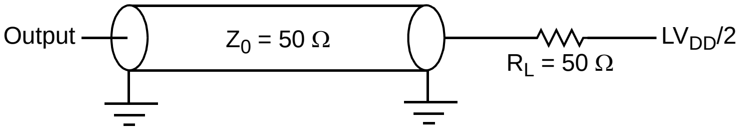


Figure 9. eTSEC AC Test Load

Figure 19 provides the AC test load for eTSEC.

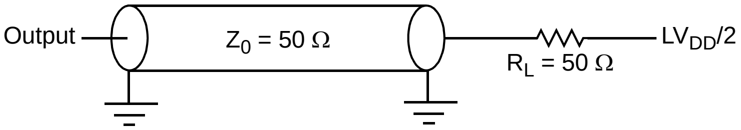


Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.

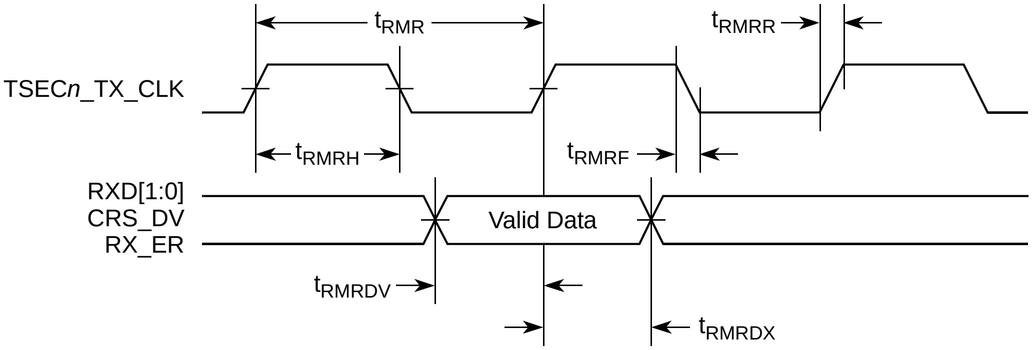


Figure 20. RMII Receive AC Timing Diagram

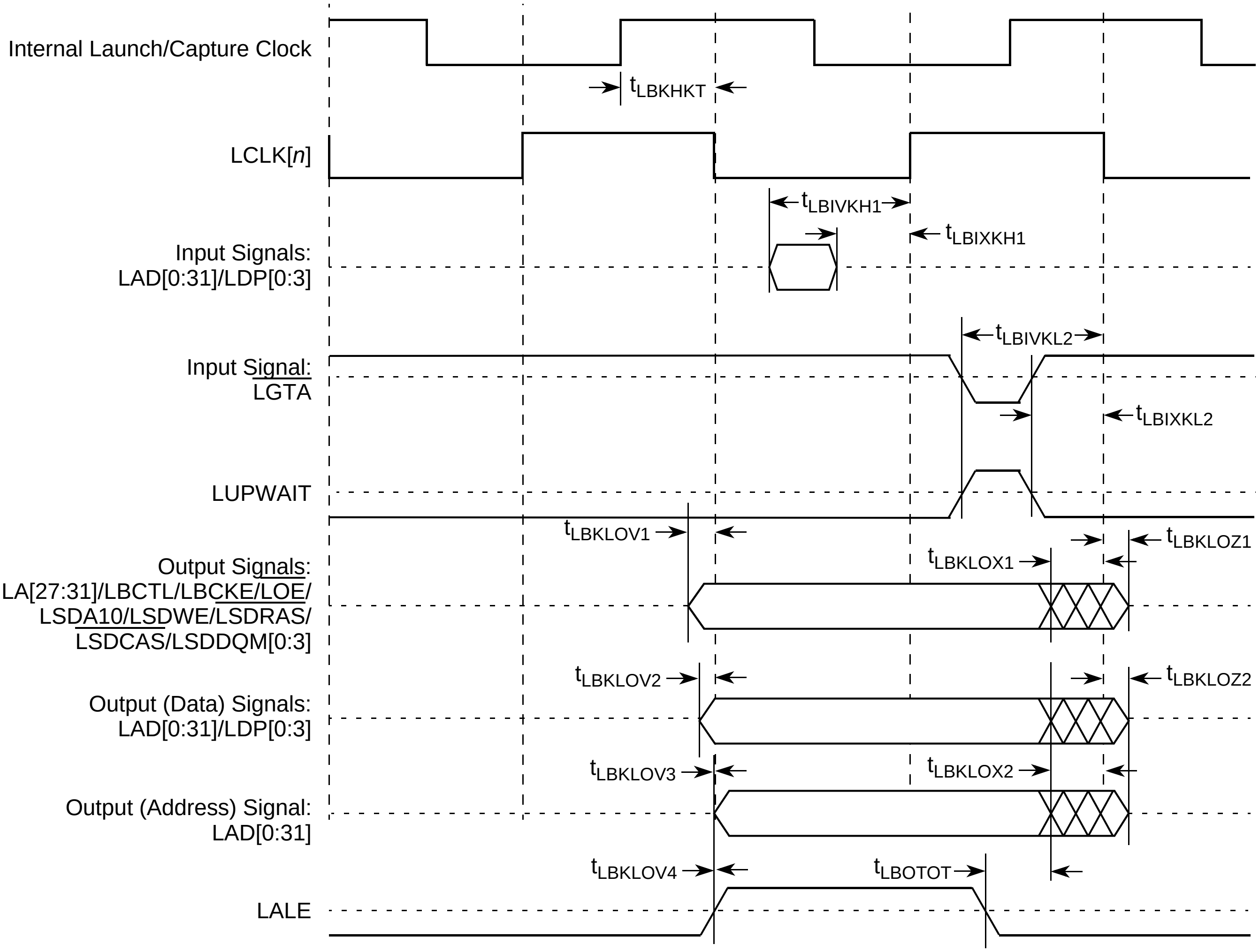


Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

14 GP_{OUT}/GP_{IN}

This section describes the DC and AC electrical specifications for the GP_{OUT}/GP_{IN} bus of the device.

14.1 GP_{OUT}/GP_{IN} Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP_{OUT} interface.

Table 47. GP_{OUT} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV_{DD}	3.13	3.47	V
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Table 48. GP_{OUT} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV_{DD}	2.37	2.63	V
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP_{IN} interface.

Table 49. GP_{IN} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the PCI AC timing specifications at 66 MHz.

Table 52. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
CLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from CLK	t_{PCKHOX}	2.0	—	ns	2, 10
CLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to CLK	t_{PCIVKH}	3.0	—	ns	2, 5, 10
Input hold from CLK	t_{PCIXKH}	0	—	ns	2, 5, 10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7, 11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8, 11

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of SYSCLK or PCI_CLK*n* to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 20, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.
10. Guaranteed by characterization.
11. Guaranteed by design.

Figure 35 provides the AC test load for PCI and PCI-X.

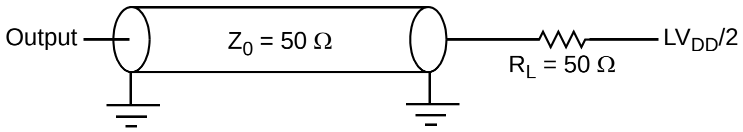


Figure 35. PCI/PCI-X AC Test Load

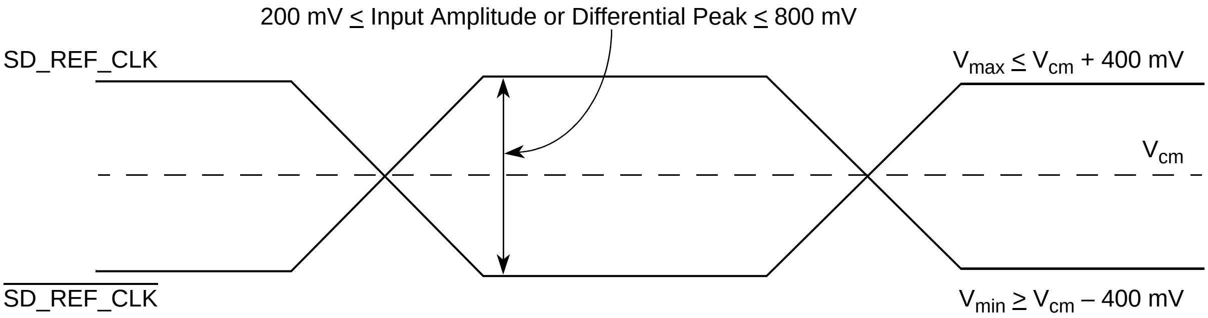


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

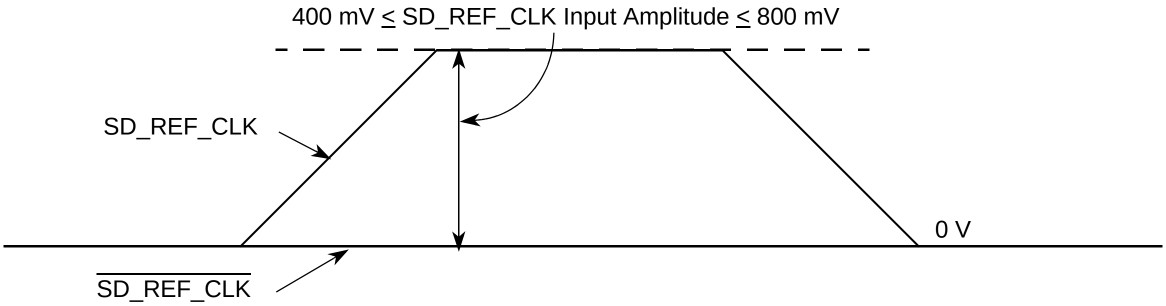


Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

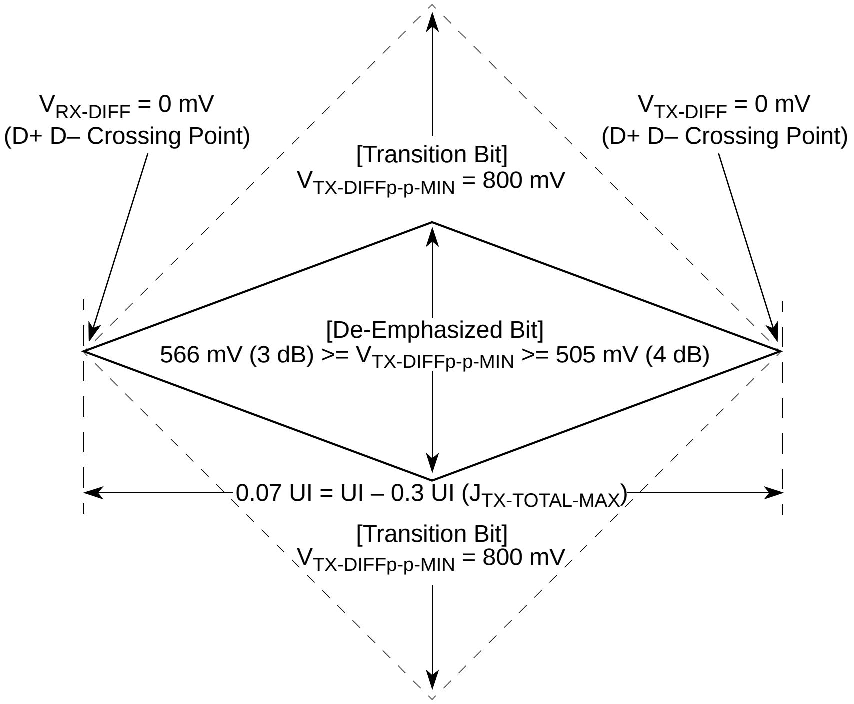


Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.

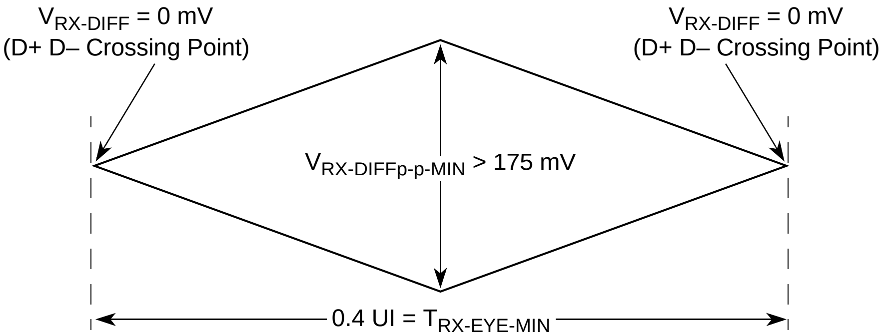


Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

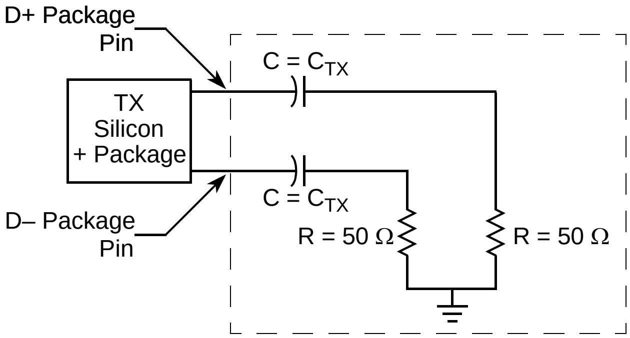


Figure 50. Compliance Test/Measurement Load

18 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8548E, for the LP-Serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

18.1 DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, “SerDes Reference Clocks.”

18.2 AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

Table 58 lists the Serial RapidIO SD_REF_CLK and SD_REF_CLK AC requirements.

Table 58. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–40	—	40	ps	—

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV$_{DD}$	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV$_{DD}$	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV$_{DD}$	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV$_{DD}$	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV$_{DD}$	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV$_{DD}$	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV$_{DD}$	—
MBA[0:2]	F7, J7, M11	O	GV$_{DD}$	—
$\overline{\text{MWE}}$	E7	O	GV$_{DD}$	—
$\overline{\text{MCAS}}$	H7	O	GV$_{DD}$	—
$\overline{\text{MRAS}}$	L8	O	GV$_{DD}$	—
MCKE[0:3]	F10, C10, J11, H11	O	GV$_{DD}$	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV$_{DD}$	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV$_{DD}$	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV$_{DD}$	—
MODT[0:3]	E6, K6, L7, M7	O	GV$_{DD}$	—
MDIC[0:1]	A19, B19	I/O	GV$_{DD}$	36

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[7:4]/PCI2_C_$\overline{\text{BE}}$[3:0]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV_{DD}	—
$\overline{\text{PCI1\_GNT}}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1\_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1\_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_TRDY}}$	AG11	I/O	OV_{DD}	2
$\overline{\text{PCI1\_REQ}}$[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ0}}$	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
$\overline{\text{PCI1\_DEVSEL}}$	AH11	I/O	OV_{DD}	2

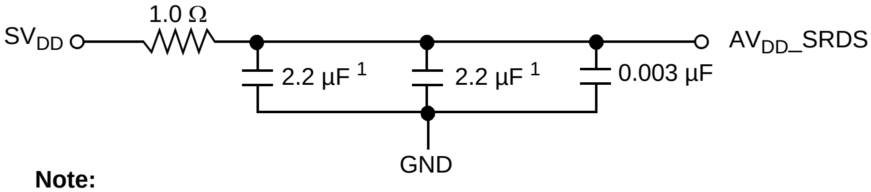
Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV_{DD}	25
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV$_{DD}$	—
LSYNC_OUT	F28	O	BV$_{DD}$	—
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV$_{DD}$	5, 9, 108
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV$_{DD}$	—
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV$_{DD}$	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV$_{DD}$	—
$\overline{\text{MCP}}$	AG19	I	OV$_{DD}$	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV$_{DD}$	—
IRQ[8]	AF19	I	OV$_{DD}$	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV$_{DD}$	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV$_{DD}$	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV$_{DD}$	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV$_{DD}$	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV$_{DD}$	5, 9
EC_MDIO	AC8	I/O	OV$_{DD}$	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV$_{DD}$	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV$_{DD}$	5, 9
TSEC1_COL	R4	I	LV$_{DD}$	—
TSEC1_CRS	V5	I/O	LV$_{DD}$	20
TSEC1_GTX_CLK	U7	O	LV$_{DD}$	—
TSEC1_RX_CLK	U3	I	LV$_{DD}$	—
TSEC1_RX_DV	V2	I	LV$_{DD}$	—
TSEC1_RX_ER	T1	I	LV$_{DD}$	—
TSEC1_TX_CLK	T6	I	LV$_{DD}$	—
TSEC1_TX_EN	U9	O	LV$_{DD}$	30
TSEC1_TX_ER	T7	O	LV$_{DD}$	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV$_{DD}$	103

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

NOTE

> It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

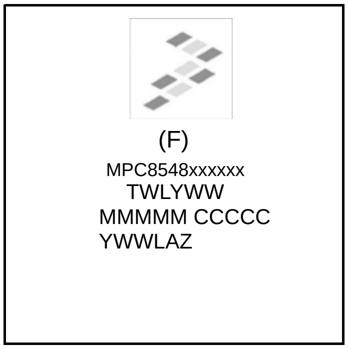
- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK

23.2 Part Marking

Parts are marked as the example shown in Figure 64.



Notes:

TWLYYWW is final test traceability code.
MMMMM is 5 digit mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	• Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. • Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." • Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. • Removed Note from Section 5.1, "Power-On Ramp Rate". • Changed the Table 10 title to "Power Supply Ramp Rate". • Removed table 11. • Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. • Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" • Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. • Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)[1]" from 4 and 25 to 2 and 10 respectively .
8	04/2011	• Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." • Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. • Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	• In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." • Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	• In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. • In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. • In Table 13 deleted ramp rate requirement for XVDD/SVDD. • In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. • In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	• In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. • Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." • Added a reference to Revision 2.1.2. • Updated Table 55, "MII Management AC Timing Specifications." • Added Section 5.1, "Power-On Ramp Rate."