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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8547hxatg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

 Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
 - Flexible configuration.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
 - Four inbound windows plus a default window on RapidIO[™]
 - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
 - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface
 - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
 - DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
 - Full ECC support
 - Page mode support
 - Up to 16 simultaneous open pages for DDR

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	1
	45(default) 45(default)	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	
PCI signals	25	OV _{DD} = 3.3 V	2
	45(default)		
DDR signal	18 36 (half strength mode)	GV _{DD} = 2.5 V	3
DDR2 signal	18 36 (half strength mode)	GV _{DD} = 1.8 V	3
TSEC/10/100 signals	45	L/TV _{DD} = 2.5/3.3 V	
DUART, system control, JTAG	45	OV _{DD} = 3.3 V	—
12C	150	OV _{DD} = 3.3 V	_

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.

3. The drive strength of the DDR interface in half-strength mode is at $T_i = 105^{\circ}C$ and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

- 1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
- 2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = min$, $I_{OH} = -4.0 mA$)	V _{OH}	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	_
Output low voltage ($LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA$)	V _{OL}	GND	0.50	V	_
Input high voltage	V _{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	_
Input low voltage	V _{IL}	-0.3	0.90	V	_
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IH}	—	40	μΑ	1, 2, 3
Input low current (V _{IN} = GND)	I	-600	_	μA	

Table 22.	GMII. MI	I. RMII. a	and TBI DC	Electrical	Characteristics
	O min, mi	.,		Licothour	onaraotoristios

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. TV_DD supports eTSECs 3 and 4.

3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

A summary of the FIFO AC specifications appears in Table 24 and Table 25.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
TX_CLK, GTX_CLK clock period	t _{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t _{FITH} /t _{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}	—	_	250	ps
Rise time TX_CLK (20%–80%)	t _{FITR}	—	_	0.75	ns
Fall time TX_CLK (80%–20%)	t _{FITF}	—	_	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t _{FITDV}	2.0	_	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	_	3.0	ns

Table 24. FIFO Mode Transmit AC Timing Specification

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t _{FIRH} /t _{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t _{FIRJ}	—		250	ps
Rise time RX_CLK (20%-80%)	t _{FIRR}	—	_	0.75	ns
Fall time RX_CLK (80%–20%)	t _{FIRF}	—	_	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{FIRDX}	0.5			ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 4.5, "Platform to FIFO Restrictions."

Timing diagrams for FIFO appear in Figure 6 and Figure 7.



Figure 6. FIFO Transmit AC Timing Diagram

Ethernet Management Interface Electrical Characteristics

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum f_{MDC} = f_{CCB} ÷ 64 and minimum f_{MDC} = f_{CCB} ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

10.2 Local Bus AC Electrical Specifications

This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.3	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}		2.5	ns	5

Table 40. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

PCI/PCI-X

Table 54. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the PCI-X 1.0a Specification.

- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the PCI-X 1.0a Specification.

- 10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
- 11. Guaranteed by characterization.

12. Guaranteed by design.

- The SD_REF_CLK and SD_REF_CLK are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or SD_REF_CLK) has a 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
- The external reference clock driver must be able to drive this termination.
- The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (see the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD_REF_CLK and $\overline{\text{SD}_{\text{REF}_{\text{CLK}}}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement:
 - This requirement is described in detail in the following sections.



Figure 39. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

• Differential mode

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
------------------------------	-------------------------

Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	_	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- -10 dB for (baud frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \le \text{Freq}(f) \le \text{baud}$ frequency

The reference impedance for the differential return loss measurements is $100-\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Characteristic	Symbol	Range		Unit	Notos
Characteristic	Symbol	Min	Max	Onic	NOIES
Output voltage	Vo	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic jitter	J _D	_	0.17	UI p-p	_
Total jitter	J _T	_	0.35	UI p-p	_
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 59. Short Run	Transmitter	AC Timina	Specifications-	-1.25 GBaud
	11 anon 11 a	.e	opoonnounomo	III OBuuu

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 2)		
TSEC2 RXDI7:01	P2, R2, N1, N2, P3, M2, M1, N3		LVpp	_
TSEC2 TXDI7:01	N9. N10. P8. N7. R9. N5. R8. N6	0	LVpp	5. 9. 33
TSEC2 COL	P1		LVpp	
TSEC2 CRS	R6	I/O	LVpp	20
TSEC2 GTX CLK	P6	0	LVDD	_
TSEC2 RX CLK	N4		LVpp	
TSEC2 RX DV	P5		LVpp	_
TSEC2 RX ER	R1		LVpp	_
TSEC2 TX CLK	P10		LVpp	
TSEC2 TX EN	P7	0	LVpp	30
TSEC2 TX ER	R10	0	LVpp	5. 9. 33
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 3)	DD	-, -,
TSEC3 TXD[3:0]	V8, W10, Y10, W7	,	TVpp	5,9,29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	
TSEC3_GTX_CLK	W8	0	TV _{DD}	
TSEC3_RX_CLK	W2	I	TV _{DD}	
TSEC3_RX_DV	W1	I	TV _{DD}	
TSEC3_RX_ER	Y2	I	TV _{DD}	
TSEC3_TX_CLK	V10		TV _{DD}	_
TSEC3_TX_EN	V9	0	TV _{DD}	30
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 4)		
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1
TSEC4_GTX_CLK	AA5	0	TV _{DD}	—
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV _{DD}	1, 30
i	DUART		•	
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	_

Table 71. MPC8548E Pinout Listing (continued)

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)		1	1
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2

Table 73. MPC8545E Pinout Listing

Package Description

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	_
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV _{DD}	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV _{DD}	2
PCI2_CLK	AE28	I	OV _{DD}	39
PCI2_IRDY	AD26	I/O	OV _{DD}	2
PCI2_PERR	AD25	I/O	OV _{DD}	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	0	OV _{DD}	5, 9, 35
PCI2_GNT0	AG25	I/O	OV _{DD}	_
PCI2_SERR	AD24	I/O	OV _{DD}	2,4
PCI2_STOP	AF24	I/O	OV _{DD}	2
PCI2_TRDY	AD27	I/O	OV _{DD}	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV _{DD}	_
PCI2_REQ0	AH25	I/O	OV _{DD}	_
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	_
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	_
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	_
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	Ο	GV _{DD}	—
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_
MWE	E7	0	GV _{DD}	_
MCAS	H7	0	GV _{DD}	_
MRAS	L8	0	GV _{DD}	_
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	_
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4		OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
cfg_pci1_width	AF14	I/O	OV _{DD}	112
Reserved	V15		—	110
Reserved	AE28	_		2
Reserved	AD26		—	110
Reserved	AD25		—	110
Reserved	AE26		—	110
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_	_	101
Reserved	AE25	_		110
Reserved	AG25		—	110
Reserved	AD24	_	—	110
Reserved	AF24	_	—	110
Reserved	AD27	_	_	110
Reserved	AD28, AE27, W17, AF26		—	110
Reserved	AH25		—	110
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	—
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 74. MPC8543E Pinout Listing (continued)

Clocking

Characteristic	Maximum Processor 800 MHz		or Core Frequency 1000 MHz		Unit	Notes
	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	MHz	1, 2

Table 77. Processor Core Clocking Specifications (MPC8543E)

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 78. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)

	Maximum Process	Unit	Notes	
Characteristic	1000, 1200			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

Table 79. Memory Bus Clocking Specifications (MPC8545E)

	Maximum Process	Unit	Notes	
Characteristic	800, 1000,			
	Min	Мах		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

 Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

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level must always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.



Figure 57. PLL Power Supply Filter Circuit with PLAT Pins



Figure 58. PLL Power Supply Filter Circuit with CORE Pins



Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD}_SRDS ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to

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The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

Rev. Number	Date	Substantive Change(s)
2	04/2008	 Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit.") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	 Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." Added Section 4.4, "PCI/PCL-X Reference Clock Timing." Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 29, "GMII, MII, RMII, and TBI DC Electrical Characteristics." Corrected V_{IL}(max) in Table 22, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. Corrected V_{IH}(min) in Table 36, "MII Management DC Electrical Characteristics." Corrected V_{IH}(min) in Table 37, "MII Management AC Timing Specifications." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKH2}, t_{LBIXKH1}, and t_{LBIXKH2} in Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled" and Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKL2}, t_{LBIXKH1}, and t_{LBIXKL2} in Table 42, "Local Bus Timing Parameters —PLL Bypassed." Note that t_{LBIVKL2} and t_{LBIXKL2} in Table 42, "Local Bus Signals (PLL Bypass Mode)." Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." Added LOPWAIT assertion in Figure 26, Figure 27 and Figure 28. Carrified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" Added LOP
0	07/2007	Initial Release

Table 88. Document Revision History (continued)

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