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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	·
Ethernet	10/100/1000Mbps (4)
SATA	·
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8548hxauj

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Characteristic		Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Table 13 provides the recommended operating conditions for the DDR SDRAM controller when $GV_{DD}(typ) = 2.5 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.15	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.15	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35 V$)	I _{OL}	16.2	—	mA	—

Table 13	DDR SDRAM	DC Electrical	Characteristics	for GV	(tvn) = 2	25 V
Table 15.	DDIX SDIXAM		Gilaracteristics		(()) – 4	1.J V

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm V}_{\rm DD}$ at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 14 provides the DDR I/O capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 14. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μ A current.







Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII 1	Transmit AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSEC <i>n</i> _TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t _{RMRR}	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMRF}	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Ethernet Management Interface Electrical Characteristics

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum f_{MDC} = f_{CCB} ÷ 64 and minimum f_{MDC} = f_{CCB} ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.



This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V with PLL disabled.

Table 42. Local Bus Timing	Parameters—PLL Bypassed
----------------------------	-------------------------

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	—	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t _{lbkhkt}	2.3	4.4	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	6.2	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.1	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	—	ns	4, 5



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	Ι _{ΙΗ}	_	10	μΑ

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$ in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	2
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.

2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCIn_CLK when it is configured for asynchronous mode.

Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 11

Notes:

- 1. See the timing measurement conditions in the PCI-X 1.0a Specification.
- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI-X 1.0a Specification.

10.Guaranteed by characterization.

11.Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV		3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	_	ns	1, 11
SYSCLK to output high impedance	t _{PCKHOZ}		7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t _{PCIVKH}	1.2	_	ns	3, 5, 9, 11
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	11
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	12
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	12
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	10, 12
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	12

Table 54. PCI-X AC Timing Specifications at 133 MHz

High-Speed Serial Interfaces (HSSI)







Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.



Figure 46. Single-Ended Connection (Reference Only)

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

components are included in this requirement. The reference impedance for return loss measurements is $100-\Omega$ resistive for differential return loss and $25-\Omega$ resistive for common mode.

Characteristic	Symbol	Range		Unit	Notes
onaraoteristic	Cymbol	Min	Мах	onit	Notes
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	_	10 ⁻¹²	—	—
Unit interval	UI	800	800	ps	±100 ppm

Table 66	. Receiver	AC	Timing	Specification	ns—1.25 GBaud
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Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notos
Gharacteristic	Symbol	Min	Max	Unit	NOICS
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10 ⁻¹²		—
Unit interval	UI	400	400	ps	±100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	I ² C interface			•
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
	SerDes			•
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—
SD_PLL_TPD	U28	0	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	3
SD_REF_CLK	T27	I	XV _{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	_	_	32
Reserved	M25, V27	—	_	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			·
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—
	System Control			
HRESET	AG17	I	OV _{DD}	_
HRESET_REQ	AG16	0	OV _{DD}	29
SRESET	AG20	I	OV _{DD}	
CKSTP_IN	AA9	I	OV _{DD}	—
CKSTP_OUT	AA8	0	OV _{DD}	2, 4
	Debug			
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29
MDVAL	AE5	0	OV _{DD}	6
CLK_OUT	AE21	0	OV _{DD}	11

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	_
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV _{DD}	
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	_
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	_
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV _{DD}	
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV _{DD}	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Powerfor CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	0	V _{DD}	13

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 Ω to GND	
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	_
SD_PLL_TPA	U26	0	_	24

Table 73. MPC8545E Pinout Listing (continued)

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
PCI1 (One 32-Bit)							
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	_	_	110			
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	0	OV _{DD}	—			
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV _{DD}	111			
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17			
Reserved	AF15, AD14, AE15, AD15	_	—	110			
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17			
Reserved	W15	_	—	110			
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35			
PCI1_GNT0	AG5	I/O	OV _{DD}	—			
PCI1_IRDY	AF11	I/O	OV _{DD}	2			
PCI1_PAR	AD12	I/O	OV _{DD}	—			
PCI1_PERR	AC12	I/O	OV _{DD}	2			
PCI1_SERR	V13	I/O	OV _{DD}	2, 4			
PCI1_STOP	W12	I/O	OV _{DD}	2			

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4		OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
cfg_pci1_width	AF14	I/O	OV _{DD}	112
Reserved	V15		—	110
Reserved	AE28	_		2
Reserved	AD26		—	110
Reserved	AD25		—	110
Reserved	AE26		—	110
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_	_	101
Reserved	AE25	_		110
Reserved	AG25		—	110
Reserved	AD24	_	—	110
Reserved	AF24	_	—	110
Reserved	AD27	_	_	110
Reserved	AD28, AE27, W17, AF26		—	110
Reserved	AH25		—	110
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	—
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 74. MPC8543E Pinout Listing (continued)

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

Table 82. e500 Core to	CCB Clock Ratio
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20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	25	33.33	41.66	66.66	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500		-	
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533		-				
20	333	500		-					

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

• SD_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = $0xE_0F08$) (this prevents the oscillations and holds the receiver output in a fixed state) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

22.11 Guideline for PCI Interface Termination

PCI termination if PCI 1 or PCI 2 is not used at all.

Option 1

If PCI arbiter is enabled during POR:

- All AD pins are driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

If PCI arbiter is disabled during POR:

- All AD pins are in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following is the termination recommendation:

- For LDP[0:3]—tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE—tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

23.2 Part Marking

Parts are marked as the example shown in Figure 64.



Notes:

TWLYYWW is final test traceability code. MMMMM is 5 digit mask number. CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States. YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device