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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8543ecpxaqgb

Table 1. Absolute Maximum Ratings ¹ (continued)

Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- The -0.3 to 2.75 V range is for DDR and -0.3 to 1.98 V range is for DDR2.
- The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
- (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes	
Core supply voltage	V _{DD}	1.1 V ± 55 mV	V	—	
PLL supply voltage	AV _{DD}	1.1 V ± 55 mV	V	1	
Core power supply for SerDes transceivers	SV _{DD}	1.1 V ± 55 mV	V	—	
Pad power supply for SerDes transceivers	XV _{DD}	1.1 V ± 55 mV	V	—	
DDR and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—	
Three-speed Ethernet I/O voltage	LV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4	
	TV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	—	4	
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage	OV _{DD}	3.3 V ± 165 mV	V	3	
Local bus I/O voltage	BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—	
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

Table 4. Device Power Dissipation

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$.
3. Typical-65 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$, running Dhrystone.
4. Typical-105 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running Dhrystone.
5. Maximum is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running a smoke test.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}[n]$ crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	1.48 1.95 2.40	— — —	ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}[n]$ output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}[n]$ output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHXC}	1.48 1.95 2.40	— — —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDS} , t_{DDKLDS}	538 700 900	— — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDX} , t_{DDKLDX}	538 700 900	— — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{\text{MCK}} - 0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	6

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND -0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	10	μA	1, 2, 3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-15	—	μA	3

Notes:

1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#) and [Table 2](#).

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC n 's TSEC n _TX_CLK, while the receive clock must be applied to pin TSEC n _RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC n _GTX_CLK pin (while transmit data appears on TSEC n _TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC n _GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see [Section 4.5, "Platform to FIFO Restrictions."](#)

Figure 8 shows the GMII transmit AC timing diagram.

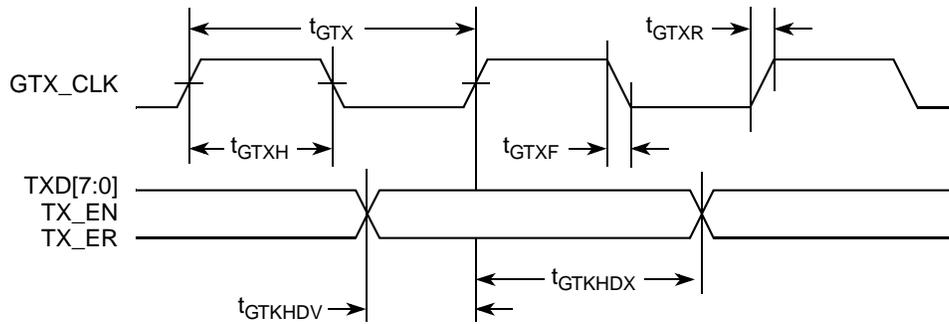


Figure 8. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}^2	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 9 provides the AC test load for eTSEC.

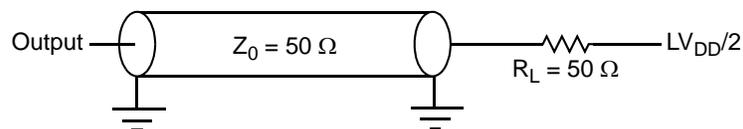


Figure 9. eTSEC AC Test Load

Figure 11 shows the MII transmit AC timing diagram.

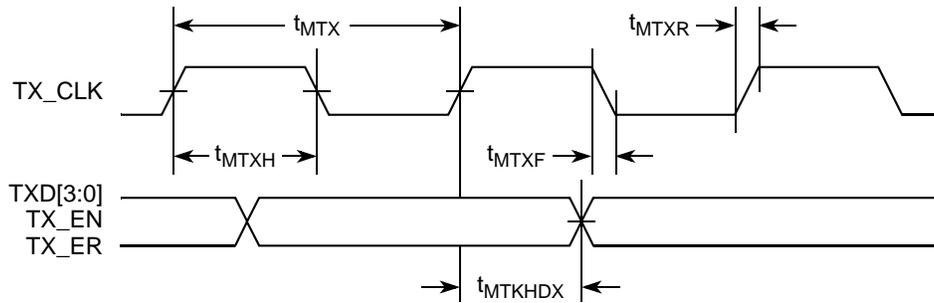


Figure 11. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}^2	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}^2	1.0	—	4.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

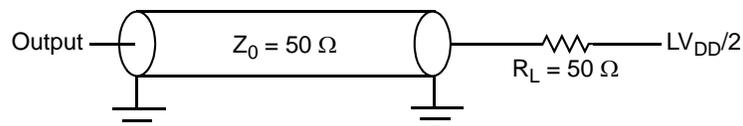


Figure 12. eTSEC AC Test Load

Figure 17 shows the RGMII and RTBI AC timing and multiplexing diagrams.

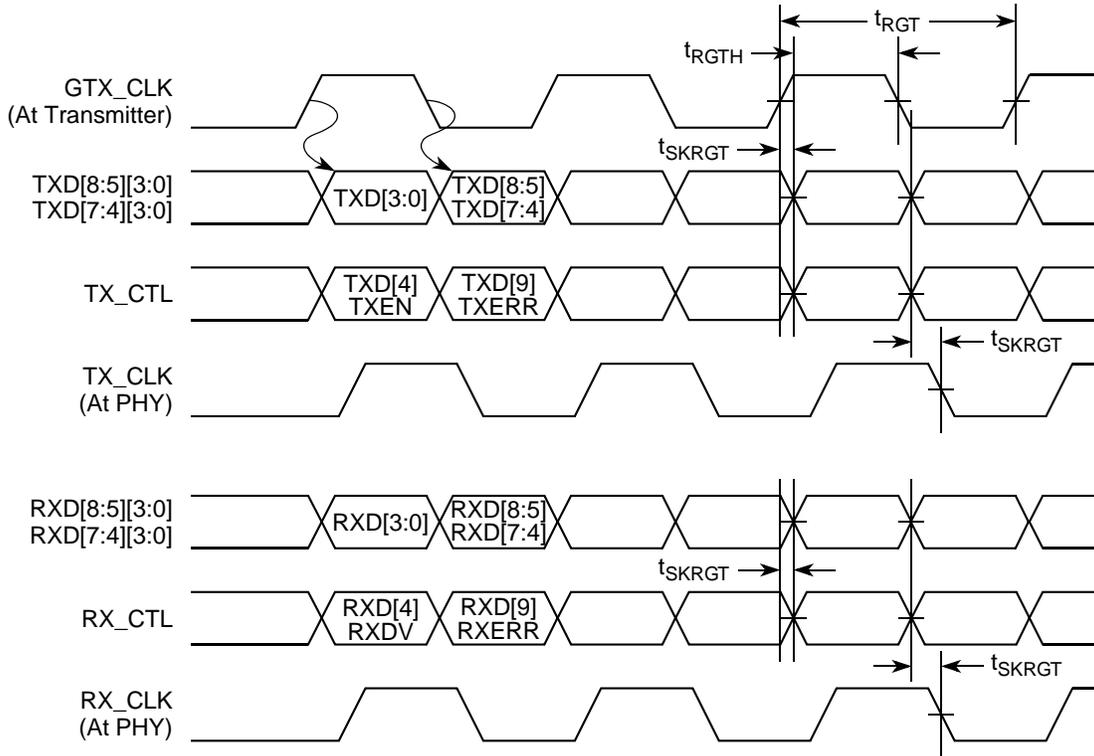


Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RGMII AC Timing Specifications

This section describes the RGMII transmit and receive AC timing specifications.

8.2.7.1 RGMII Transmit AC Timing Specifications

The RGMII transmit AC timing specifications are in this table.

Table 34. RGMII Transmit AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSEC _n _TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSEC _n _TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSEC _n _TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC _n _TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSEC _n _TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters ($BV_{DD} = 2.5$ V)—PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/UPWAIT$)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
- Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

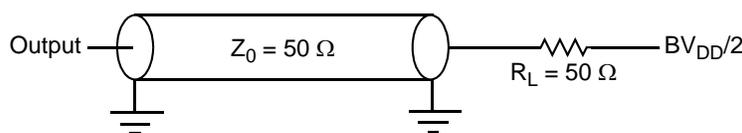


Figure 22. Local Bus AC Test Load

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
$\overline{\text{LGTA}}/\text{LUPWAIT}$ input hold from local bus clock	t_{LBIXKL2}	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t_{LBKLOV1}	—	-0.3	ns	—
Local bus clock to data valid for LAD/LDP	t_{LBKLOV2}	—	-0.1	ns	4
Local bus clock to address valid for LAD	t_{LBKLOV3}	—	0	ns	4
Local bus clock to LALE assertion	t_{LBKLOV4}	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t_{LBKLOX1}	-3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	t_{LBKLOX2}	-3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t_{LBKLOZ1}	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ2}	—	0.2	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHK1} .
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{\text{DD}}/2$.
- All signals are measured from $BV_{\text{DD}}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Guaranteed by characterization.
- Guaranteed by design.

Local Bus

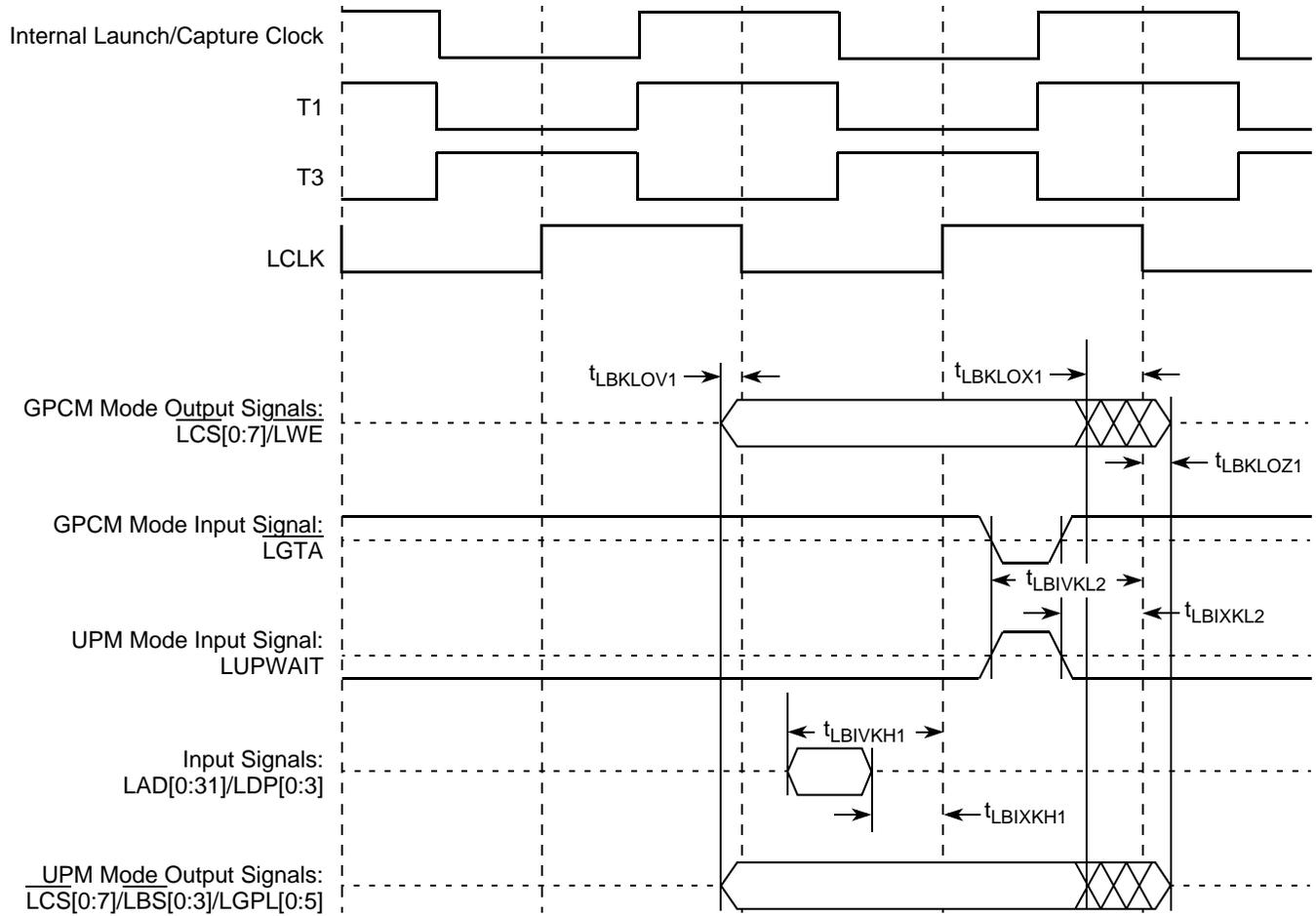


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

This table provides the PCI AC timing specifications at 66 MHz.

Table 52. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
CLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from CLK	t_{PCKHOX}	2.0	—	ns	2, 10
CLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to CLK	t_{PCIVKH}	3.0	—	ns	2, 5, 10
Input hold from CLK	t_{PCIXKH}	0	—	ns	2, 5, 10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7, 11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8, 11

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- All PCI signals are measured from $OV_{DD}/2$ of the rising edge of SYSCLK or PCI_CLK n to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see [Section 20, "Clocking."](#)
- The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs .
- Guaranteed by characterization.
- Guaranteed by design.

[Figure 35](#) provides the AC test load for PCI and PCI-X.

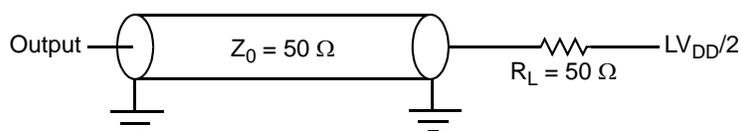


Figure 35. PCI/PCI-X AC Test Load

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see [Section 16.2, “SerDes Reference Clocks.”](#)

17.2 AC Requirements for PCI Express SerDes Clocks

[Table 55](#) lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50	—	50	ps	—

Note:

1. Typical based on *PCI Express Specification 2.0*.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification, Rev. 1.0a*.

17.4.1 Differential Transmitter (TX) Output

[Table 56](#) defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} + V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$ V_{TX-CM-DC} \text{ (during L0)} + V_{TX-CM-Idle-DC} \text{ (during electrical idle)} \leq 100$ mV $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [L0] $V_{TX-CM-Idle-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D-	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = \text{DC}_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = \text{DC}_{(avg)}$ of $ V_{TX-D-} $. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

Table 68. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	320	320	ps	± 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

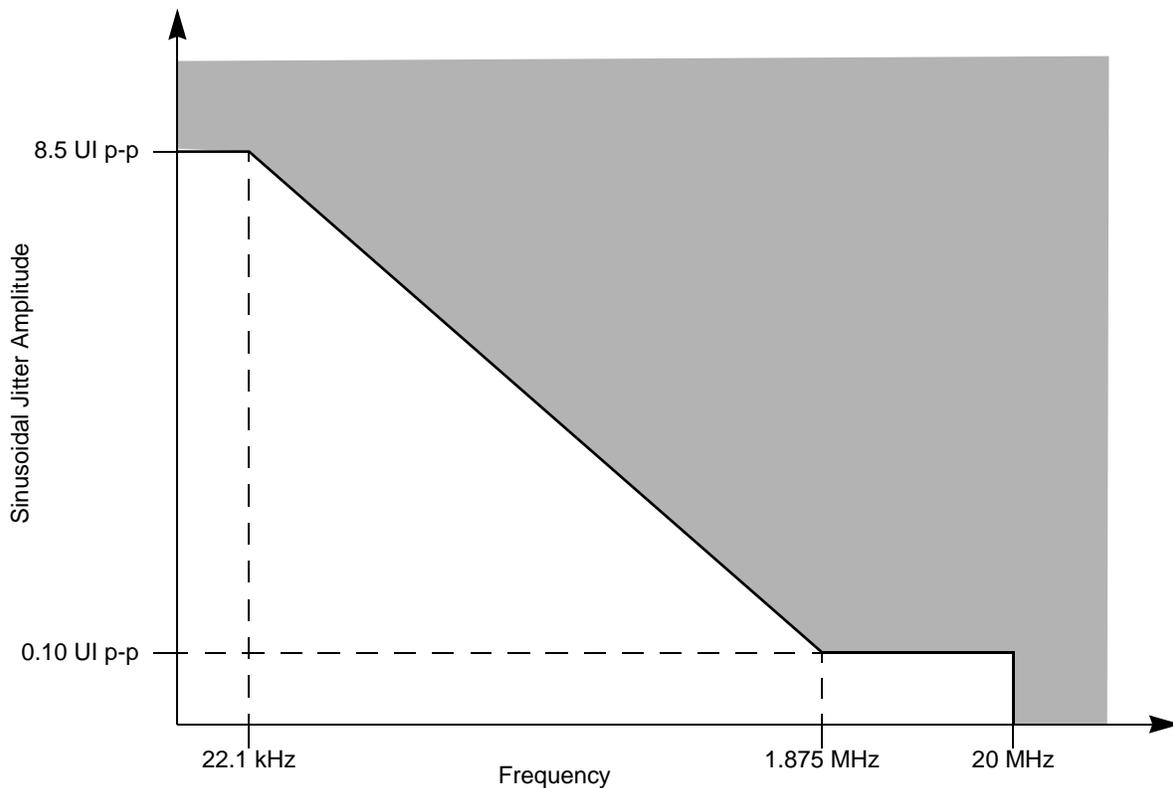


Figure 53. Single Frequency Sinusoidal Jitter Limits

Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER	R10	O	LV _{DD}	5, 9, 33
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	—
TSEC3_GTX_CLK	W8	O	TV _{DD}	—
TSEC3_RX_CLK	W2	I	TV _{DD}	—
TSEC3_RX_DV	W1	I	TV _{DD}	—
TSEC3_RX_ER	Y2	I	TV _{DD}	—
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	O	TV _{DD}	30
Three-Speed Ethernet Controller (Gigabit Ethernet 4)				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV _{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1
TSEC4_GTX_CLK	AA5	O	TV _{DD}	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV _{DD}	1, 30
DUART				
$\overline{\text{UART_CTS}}[0:1]$	AB3, AC5	I	OV _{DD}	—
$\overline{\text{UART_RTS}}[0:1]$	AC6, AD7	O	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV _{DD}	—
I²C Interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV _{DD}	—
$\overline{\text{SD_RX}}[0:3]$	M27, N25, P27, R25	I	XV _{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	O	XV _{DD}	—
$\overline{\text{SD_TX}}[0:3]$	M23, N21, P23, R21	O	XV _{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40

level must always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 57](#), one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

[Figure 57](#) through [Figure 59](#) shows the PLL power supply filter circuits.

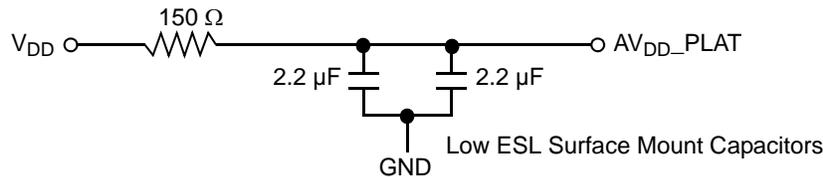


Figure 57. PLL Power Supply Filter Circuit with PLAT Pins

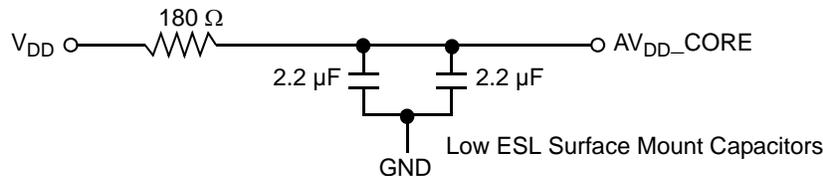


Figure 58. PLL Power Supply Filter Circuit with CORE Pins

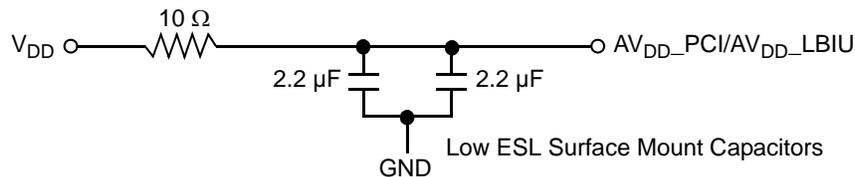


Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} ball to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDS} ball. The 0.003- μF capacitor is closest to the ball, followed by the two 2.2 μF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDS} to

- First, the board must have at least 10×10 -nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1- μ F ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: $TSEC3_TXD[3]$, $\overline{HRESET_REQ}$, $TRIG_OUT/READY/QUIESCE$, $MSRCID[2:4]$, ASLEEP. The $\overline{DMA_DACK}[0:1]$, and $TEST_SEL/TEST_SEL$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

as shown in [Figure 63](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

COP_TDO	1	2	NC
COP_TDI	3	4	$\overline{\text{COP_TRST}}$
COP_RUN/STOP	5	6	COP_VDD_SENSE
COP_TCK	7	8	$\overline{\text{COP_CHKSTP_IN}}$
COP_TMS	9	10	NC
$\overline{\text{COP_SRESET}}$	11	12	NC
$\overline{\text{COP_HRESET}}$	13	KEY No pin	
$\overline{\text{COP_CHKSTP_OUT}}$	15	16	GND

Figure 62. COP Connector Physical Pinout

- $\overline{\text{SD_REF_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (this prevents the oscillations and holds the receiver output in a fixed state) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

22.11 Guideline for PCI Interface Termination

PCI termination if PCI 1 or PCI 2 is not used at all.

Option 1

If PCI arbiter is enabled during POR:

- All AD pins are driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

If PCI arbiter is disabled during POR:

- All AD pins are in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following is the termination recommendation:

- For LDP[0:3]—tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE—tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).