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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8543ecvjaqgd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- Single inbound doorbell message structure
- Facility to accept port-write messages
- PCI Express interface
 - PCI Express 1.0a compatible
 - Supports x8,x4,x2, and x1 link widths
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - 8 PCI Express
 - 4 PCI Express and 4 serial RapidIO
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1TM

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that $GV_{DD}(typ) = 2.5 \text{ V}$ for DDR SDRAM, and $GV_{DD}(typ) = 1.8 \text{ V}$ for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 \times GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	—	mA	—
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH/TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}	_	_	250	ps
Rise time RX_CLK (20%–80%)	t _{TRRR}	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXKH}	1.0	_	_	ns

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t _{RMRR}	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMRF}	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

JTAG

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.







Figure 32. Boundary-Scan Timing Diagram

3.	The maximum t _{I2DXKL}	has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal	al.

For the detail of I²C frequency calculation, see Determining the I²C Frequency Divider Ratio for SCL (AN2919). Note that the

200 MHz

390 kHz

0x26

512

133 MHz

346 kHz

0x00

384

4. Guaranteed by design.

FDR bit setting

I²C source clock frequency

Actual FDR divider selected

Actual I²C SCL frequency generated

Figure 33 provides the AC test load for the I^2C .



Figure 33. I²C AC Test Load

57

Table 46. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	—	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I²C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

266 MHz

378 kHz

0x05

704

333 MHz

0x2A

371 kHz

896

I²C source clock frequency is half of the CCB clock frequency for the device.

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.



Figure 46. Single-Ended Connection (Reference Only)

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
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Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	—	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 56. Differential Transmitter	· (TX) Output	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{TX-DC-CM}	The TX DC common mode voltage	0	_	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX short circuit current limit	_	_	90	mA	The total current the transmitter can provide when shorted to its ground
T _{TX-IDLE-MIN}	Minimum time spent in electrical idle	50	_		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
RL _{TX-DIFF}	Differential return loss	12	_	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL _{TX-CM}	Common mode return loss	6		—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z _{TX-DIFF-DC}	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z _{TX-DC}	Transmitter DC impedance	40	_	_	Ω	Required TX D+ as well as D– DC impedance during all states
L _{TX-SKEW}	Lane-to-lane output skew	_	_	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C _{TX}	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

Serial RapidIO

Characteristic	Symbol	Rai	nge	Unit	Netas
Characteristic	Symbol	Min	Max	Onit	NOICES
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	800	1600	mVp-p	_
Deterministic jitter	J _D	—	0.17	UI p-p	_
Total jitter	J _T	—	0.35	UI p-p	_
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 63. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Table 64. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notos
Min Max		Onic	NOIES		
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	800	1600	mVp-p	_
Deterministic jitter	J _D	—	0.17	UI p-p	_
Total jitter	J _T	—	0.35	UI p-p	_
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 52 with the parameters specified in Table 65 when measured at the output pins of the device and the device is driving a $100-\Omega \pm 5\%$ differential resistive load. The output eye pattern of an LP-serial

18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100-\Omega \pm 5\%$ differential resistive load.



Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

Package Description

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Package Description

Signal	Signal Package Pin Number				
MDIC[0:1]	I/O	GV _{DD}	36		
	Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}		
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	_	
LA[27]	H21	0	BV _{DD}	5, 9	
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9	
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	—	
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1	
LCS6/DMA_DACK2	G20	0	BV _{DD}	1	
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1	
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9	
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9	
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9	
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9	
LALE	H24	0	BV _{DD}	5, 8, 9	
LBCTL	G27	0	BV _{DD}	5, 8, 9	
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9	
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9	
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9	
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9	
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—	
LGPL5	E26	0	BV _{DD}	5, 9	
LCKE	E24	0	BV _{DD}	—	
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—	
LSYNC_IN	F27	I	BV _{DD}	—	
LSYNC_OUT	F28	0	BV _{DD}	—	
	DMA		I		
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 106	
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	-	
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	-	
Programmable Interrupt Controller					

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}	
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	_
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	_
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	_
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV _{DD}	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)		26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	0	V _{DD}	13
SENSEVSS	M16	—		13
	Analog Signals			
MVREF	A18	I Reference voltage signal for DDR	MVREF	

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	Ι	200 Ω to GND	
SD_IMP_CAL_TX	AB26	l	100 Ω to GND	_
SD_PLL_TPA	U26	0	_	24

Table 73. MPC8545E Pinout Listing (continued)

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 (One 32-Bit)			
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	_	_	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	0	OV _{DD}	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV _{DD}	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
Reserved	AF15, AD14, AE15, AD15	_	_	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
Reserved	W15	_	_	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV

These capacitors must have a value of 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

Rev. Number	Date	Substantive Change(s)
2	04/2008	 Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit.") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	 Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." Added Section 4.4, "PCI/PCL-X Reference Clock Timing." Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 29, "GMII, MII, RMII, and TBI DC Electrical Characteristics." Corrected V_{IL}(max) in Table 22, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. Corrected V_{IH}(min) in Table 36, "MII Management DC Electrical Characteristics." Corrected V_{IH}(min) in Table 37, "MII Management AC Timing Specifications." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKH2}, t_{LBIXKH1}, and t_{LBIXKH2} in Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled" and Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKL2}, t_{LBIXKH1}, and t_{LBIXKL2} in Table 42, "Local Bus Timing Parameters —PLL Bypassed." Note that t_{LBIVKL2} and t_{LBIXKL2} in Table 42, "Local Bus Signals (PLL Bypass Mode)." Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." Added LOPWAIT assertion in Figure 26, Figure 27 and Figure 28. Carrified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" Added LOP
0	07/2007	Initial Release

Table 88. Document Revision History (continued)

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