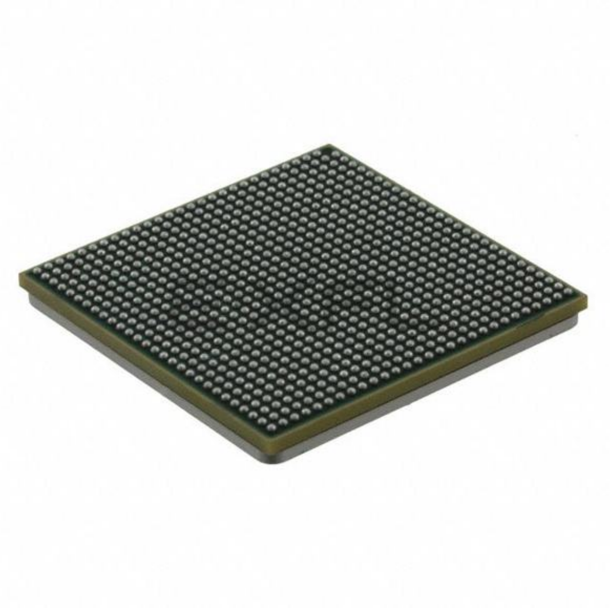


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8543ehxang

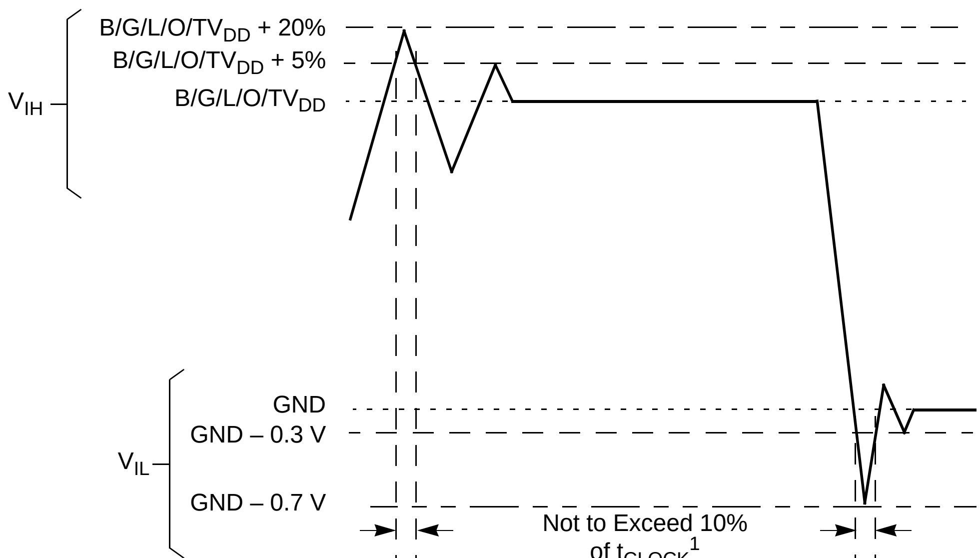
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



Notes:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I²C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI*n*_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	µs
Local bus PLL lock time	—	50	µs
PCI/PCI-X bus PLL lock time	—	50	µs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.
2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, “PLL Power Supply Filtering,” the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:
1. Guaranteed by design.
2. f_{CCB} refers to the internal platform clock.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—		10	ns	4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB} \div 64$ and minimum $f_{MDC} = f_{CCB} \div 448$. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the *MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual* for more detail.
3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
4. Guaranteed by design.
5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.

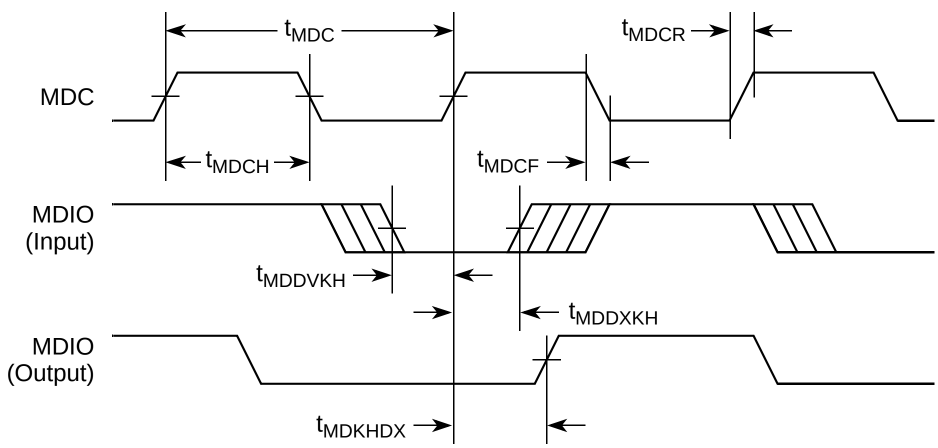


Figure 21. MII Management Interface Timing Diagram

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}$/UPWAIT)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{LGTA}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{LGTA}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

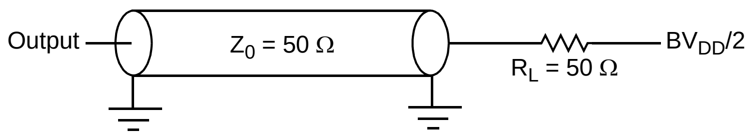


Figure 22. Local Bus AC Test Load

Figure 36 shows the PCI/PCI-X input AC timing conditions.

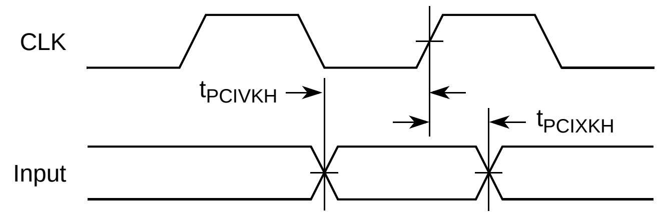


Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.

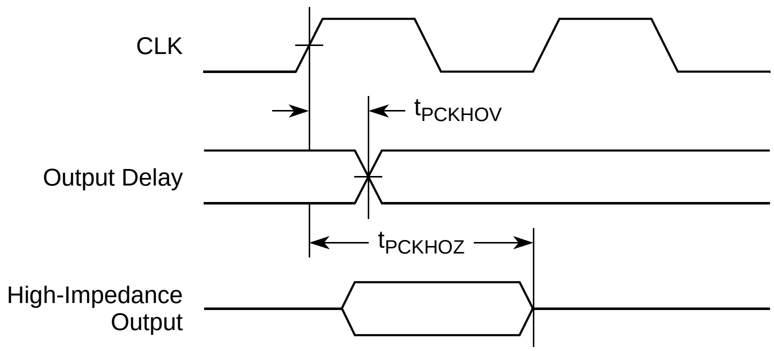


Figure 37. PCI/PCI-X Output AC Timing Measurement Condition

Table 53 provides the PCI-X AC timing specifications at 66 MHz.

Table 53. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11

16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- Single-ended swing
  The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.
- Differential output voltage, V_{OD} (or differential output swing):
  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.
- Differential input voltage, V_{ID} (or differential input swing):
  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.
- Differential peak voltage, V_{DIFFp}
  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A – B|$ volts.
- Differential peak-to-peak, $V_{DIFFp\text{-}p}$
  Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp\text{-}p} = 2 \times V_{DIFFp} = 2 \times |(A – B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
- Common mode voltage, V_{cm}
  The common mode voltage is equal to one half of the sum of the voltages between each conductor

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}DC\text{-}CM}$	The TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50	—		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
$RL_{TX\text{-}DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC impedance during all states
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{crosslink}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in Figure 48.)
3. A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 50 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D-}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications Rev 1.0a.*
7. See Section 4.2.6.3 of the *PCI Express Base Specifications Rev 1.0a.*
8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 48 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

Table 68. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	320	320	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

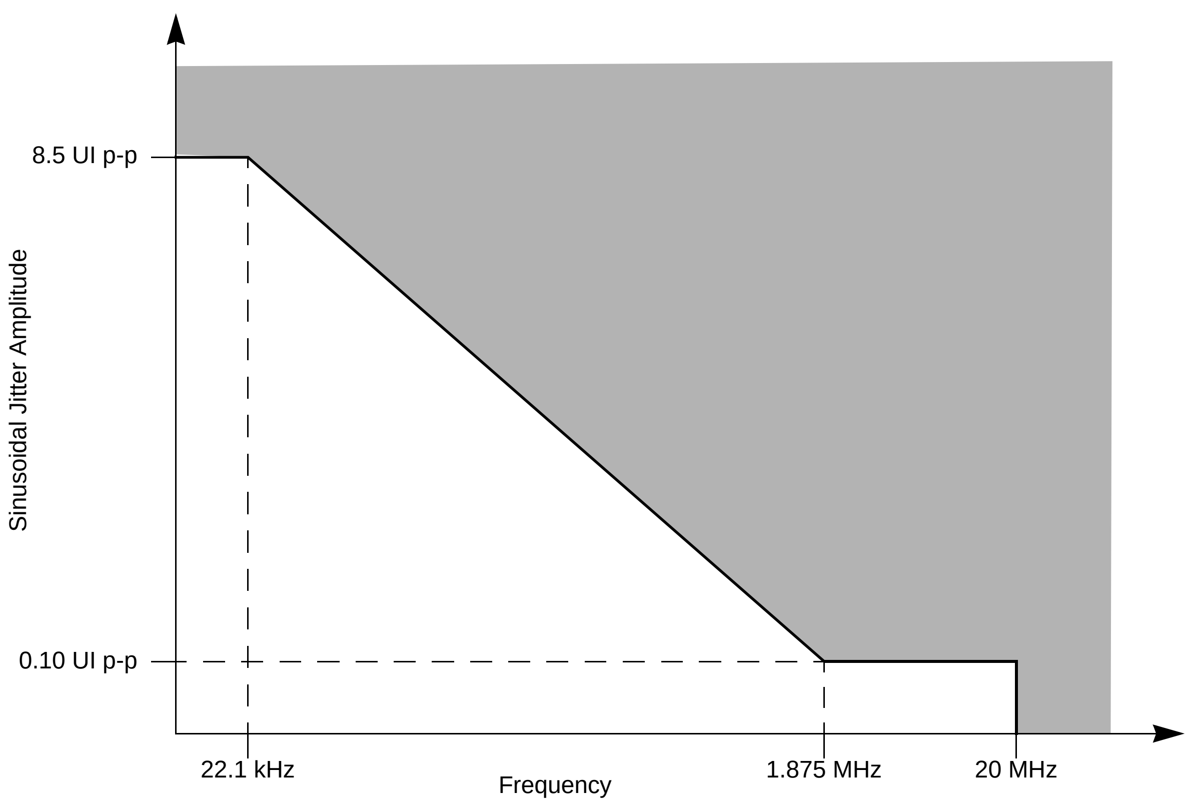


Figure 53. Single Frequency Sinusoidal Jitter Limits

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

25.These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.

26.Independent supplies derived from board V_{DD}.

27.Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OV_{DD}.

29. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], TSEC4_TXD3/TSEC3_TXD7, HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.

30.This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

31.This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.

32.These pins must be connected to XV_{DD}.

33.TSEC2_TXD1, TSEC2_TX_ER are multiplexed as cfg_dram_type[0:1]. They must be valid at power-up, even before $\overline{\text{HRESET}}$ assertion.

34.These pins must be pulled to ground through a 300-Ω (±10%) resistor.

35.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as 'no connect' or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block drives the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.

36.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

38.These pins must be left floating.

39. If PCI1 or PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK or PCI2_CLK. Otherwise the processor will not boot up.

40.These pins must be connected to GND.

101.This pin requires an external 4.7-kΩ resistor to GND.

102.For Rev. 2.x silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b11 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

103.If these pins are not used as GPIN*n* (general-purpose input), they must be pulled low (to GND) or high (to LV_{DD}) through 2–10 kΩ resistors.

104.These must be pulled low to GND through 2–10 kΩ resistors if they are not used.

105.These must be pulled low or high to LV_{DD} through 2–10 kΩ resistors if they are not used.

106.For rev. 2.x silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b10 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

107.For rev. 2.x silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b01 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

108.For rev. 2.x silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b11 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

109.This is a test signal for factory use only and must be pulled down (100 Ω – 1 kΩ) to GND for normal machine operation.

110.These pins must be pulled high to OV_{DD} through 2–10 kΩ resistors.

111.If these pins are not used as GPIN*n* (general-purpose input), they must be pulled low (to GND) or high (to OV_{DD}) through 2–10 kΩ resistors.

112.This pin must not be pulled down during POR configuration.

113.These should be pulled low or high to OV_{DD} through 2–10 kΩ resistors.

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV_{DD}	5, 9, 33
TSEC2_COL	P1	I	LV_{DD}	—
TSEC2_CRS	R6	I/O	LV_{DD}	20
TSEC2_GTX_CLK	P6	O	LV_{DD}	—
TSEC2_RX_CLK	N4	I	LV_{DD}	—
TSEC2_RX_DV	P5	I	LV_{DD}	—
TSEC2_RX_ER	R1	I	LV_{DD}	—
TSEC2_TX_CLK	P10	I	LV_{DD}	—
TSEC2_TX_EN	P7	O	LV_{DD}	30

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER	R10	O	LV_{DD}	5, 9, 33
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
Three-Speed Ethernet Controller (Gigabit Ethernet 4)				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	1
TSEC4_GTX_CLK	AA5	O	TV_{DD}	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV_{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV_{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV_{DD}	1, 30
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—
I^{2}C Interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:3]	M27, N25, P27, R25	I	XV_{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[0:3]	M23, N21, P23, R21	O	XV_{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD\_TX}}$[0:3]	M23, N21, P23, R21	O	XV_{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11
Clock				
RTC	AF16	I	OV_{DD}	—
SYSCLK	AH17	I	OV_{DD}	—
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV_{DD}	—
LSYNC_OUT	F28	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV_{DD}	5, 9, 108
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Table 82. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	**25**	**33.33**	**41.66**	**66.66**	**83**	**100**	**111**	**133.33**
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500			
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533						
20	333	500							

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

21 Thermal

This section describes the thermal specifications of the device.

21.1 Thermal for Version 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

This table shows the package thermal characteristics.

Table 84. Package Thermal Characteristics for HiCTE FC-CBGA

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{\theta JA}$	17	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{\theta JA}$	11	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\theta JA}$	8	°C/W	1, 2
Die junction-to-board	N/A	$R_{\theta JB}$	3	°C/W	3
Die junction-to-case	N/A	$R_{\theta JC}$	0.8	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.2 Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid

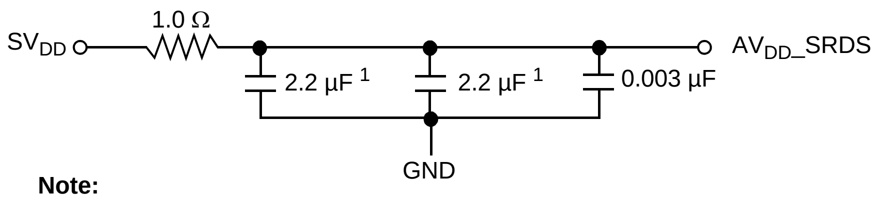
This section describes the thermal specifications for the FC-PBGA package for revision 2.1.1, 2.1.2, and 3.0 silicon.

This table shows the package thermal characteristics.

Table 85. Package Thermal Characteristics for FC-PBGA

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{\theta JA}$	18	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{\theta JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{\theta JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1, 2

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

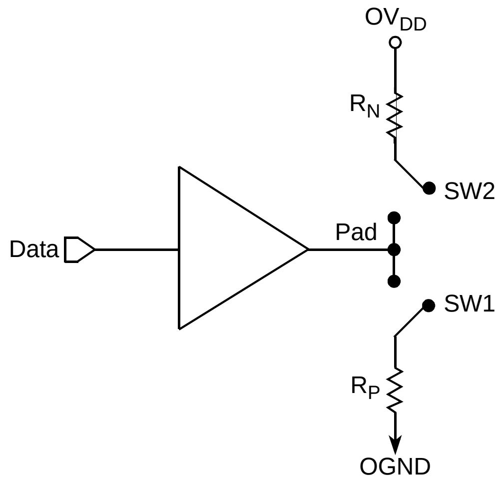


Figure 61. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 86. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

22.8 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value must permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor minimizes the disruption of signal quality or speed for output pins thus configured.