Freescale Semiconductor - MPC8543EVTANGD Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8543evtangd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the device. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	2
Three-speed Ethernet I/O voltage		LV_{DD} (for eTSEC1 and eTSEC2) TV_{DD} (for eTSEC3 and eTSEC4)	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 3.63 –0.3 to 2.75	V	3
PCI/PCI-X, DUART, system control and power management, I^2C, Ethernet MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	4
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet I/O signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	4
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	DUART, SYSCLK, system control and power management, I^2C, Ethernet MII management, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4

Figure 4 shows the DDR SDRAM output timing diagram.+

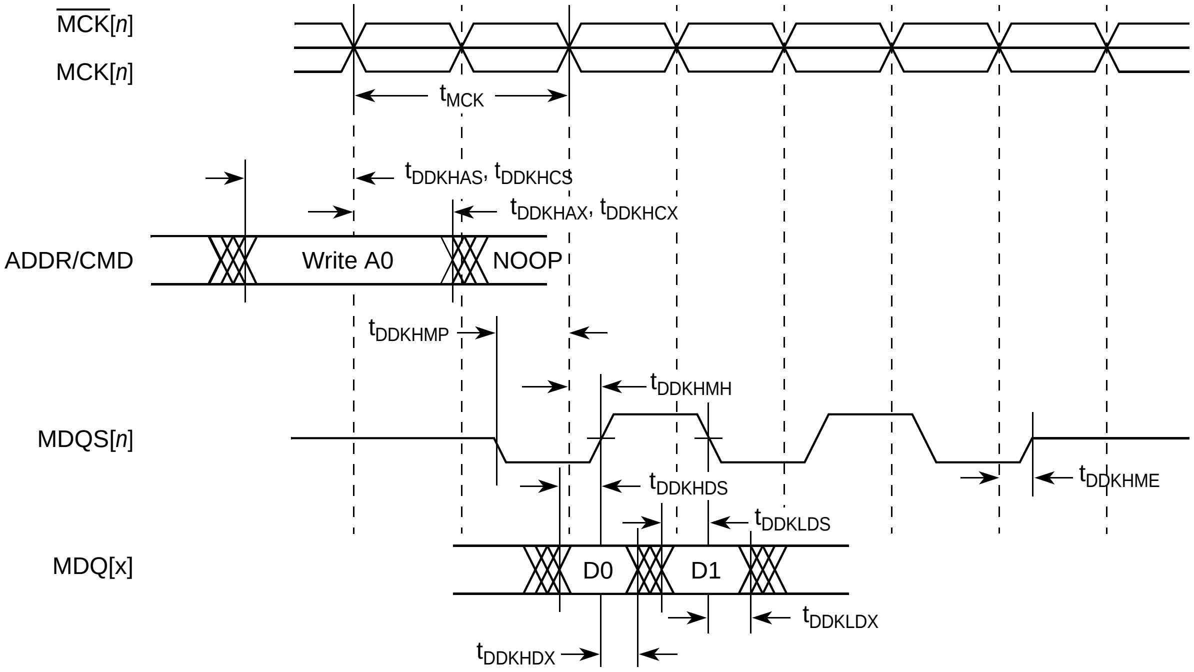

Figure 4. DDR SDRAM Output Timing Diagram

Figure 5 provides the AC test load for the DDR bus.

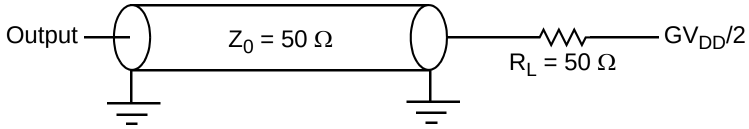

Figure 5. DDR AC Test Load

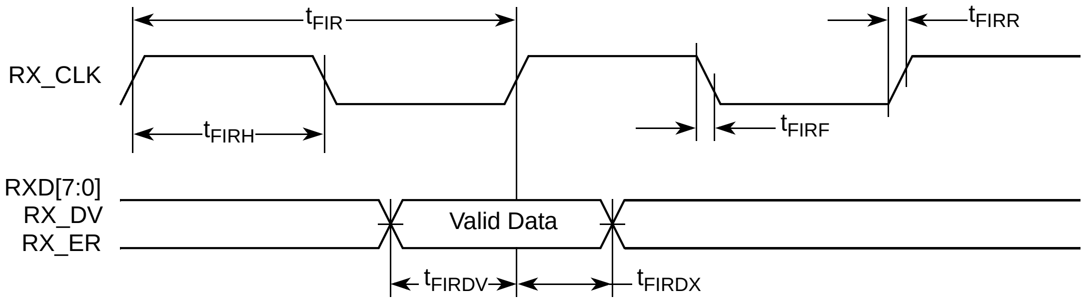

Figure 7. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%–80%)	t_{GTXR}[2]	—	—	1.0	ns
GTX_CLK data clock fall time (80%–20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 36. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, $V_{IN}{}^{1}$ = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t_{MDC}	120.5	—	1389	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16 \times t_{CCB}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{CCB} \times 8) - 3$	—	$(16 \times t_{CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.

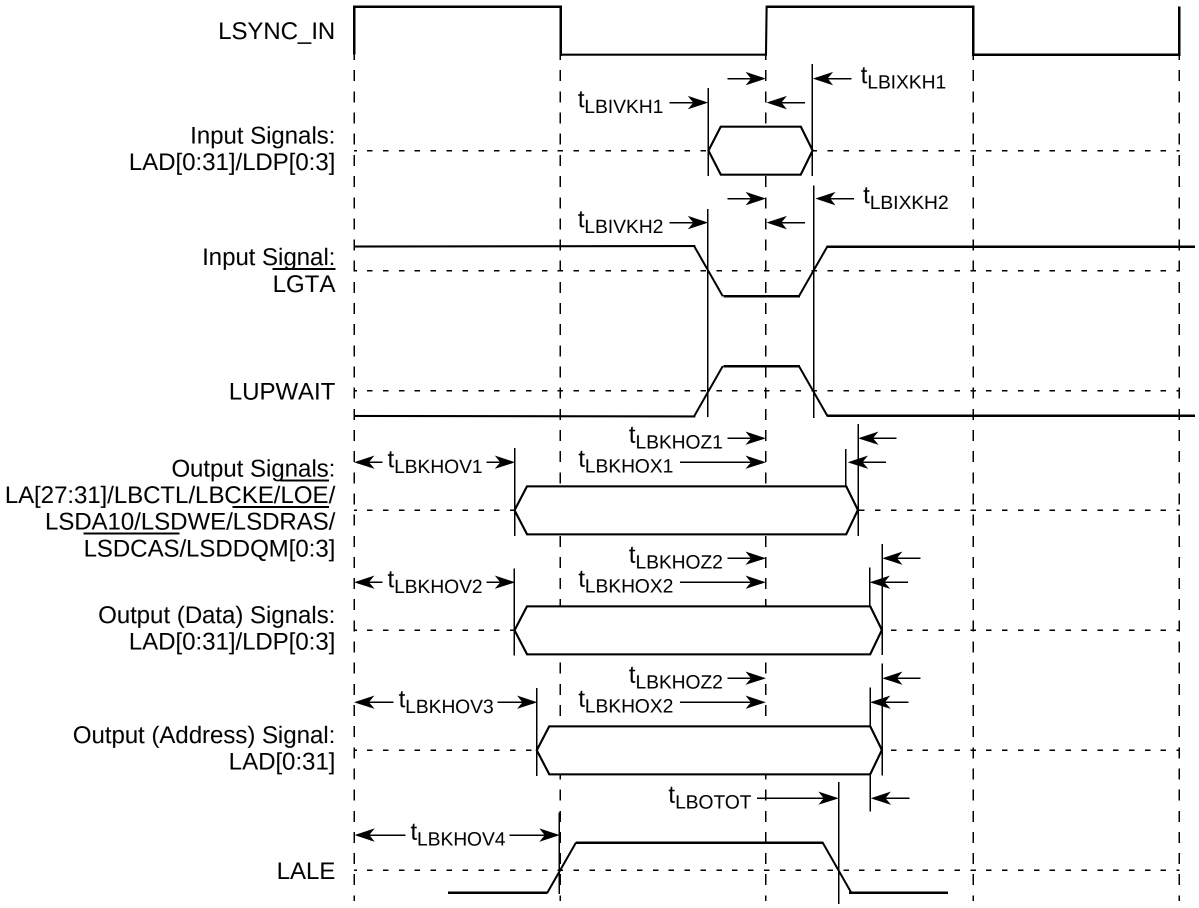

Figure 23. Local Bus Signals (PLL Enabled)

This table describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V with PLL disabled.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5

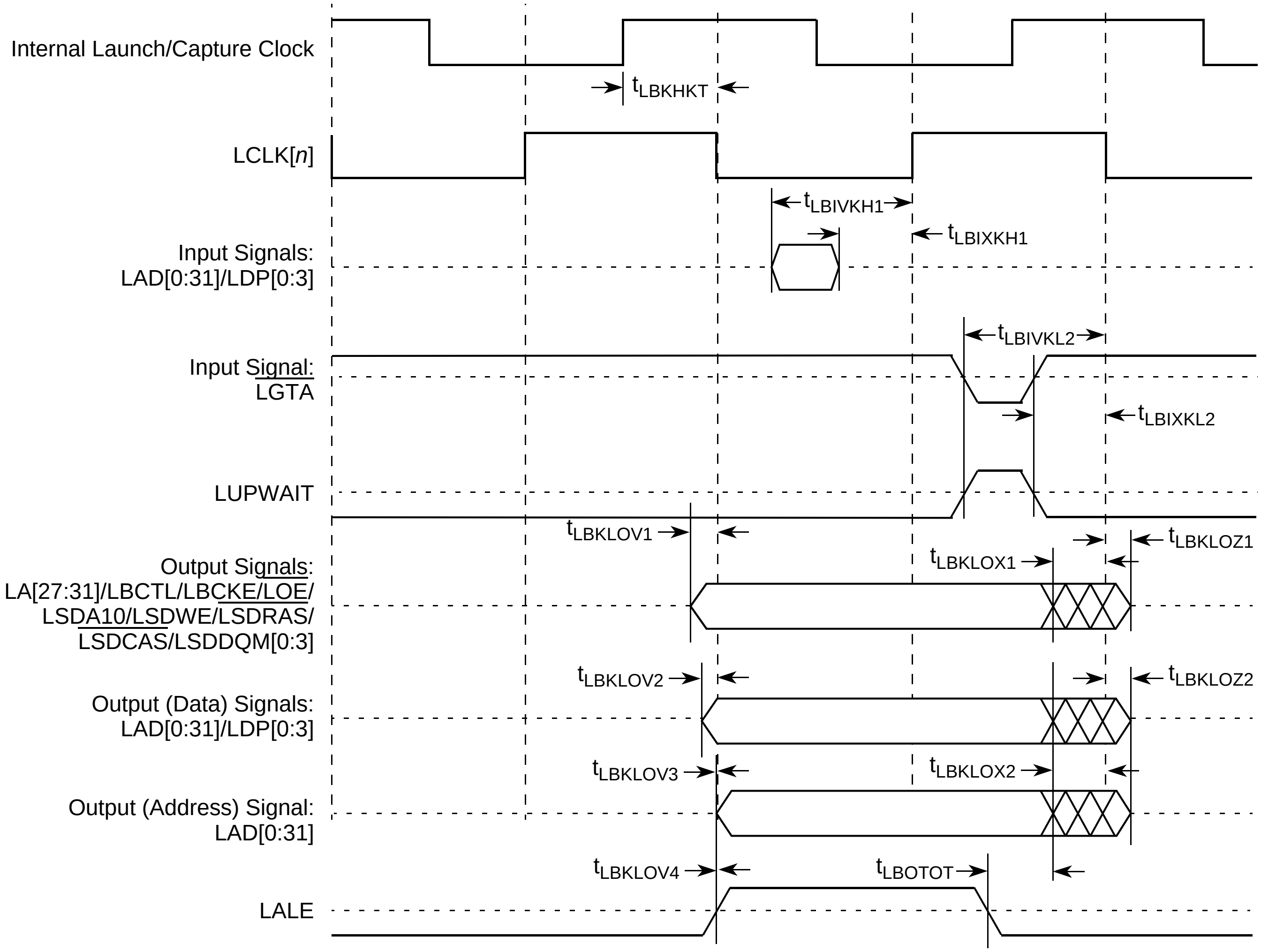

Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, “AC Requirements for PCI Express SerDes Clocks”
- Section 18.2, “AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK”

16.2.4.1 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK are designed to work with a spread spectrum clock (+0% to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane’s transmitter and receiver.

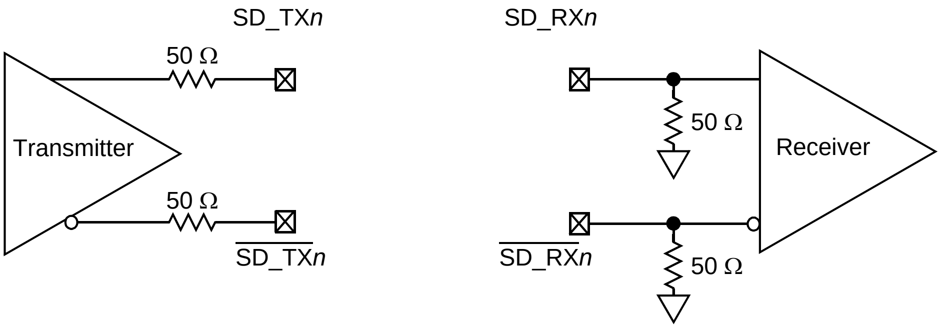

Figure 47. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, “PCI Express”
- Section 18, “Serial RapidIO”

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

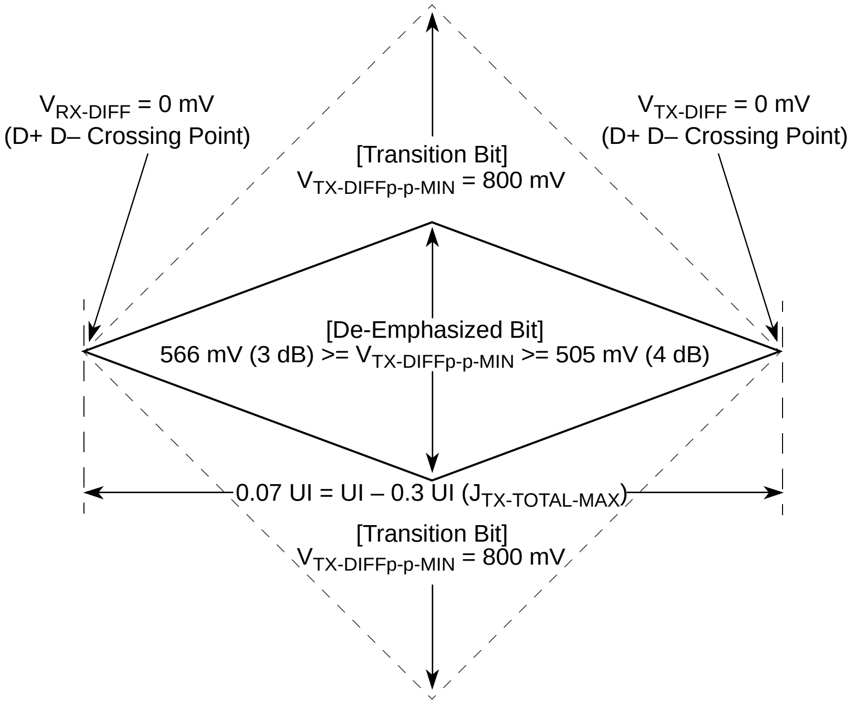

Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$. See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$L_{TX\text{-}SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in Figure 49). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –{300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 50) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 49) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

Table 60. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 61. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

Table 62. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	800	1600	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	800	800	ps	±100 ppm

Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV$_{DD}$	—
LSYNC_OUT	F28	O	BV$_{DD}$	—
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV$_{DD}$	5, 9, 102
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV$_{DD}$	—
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV$_{DD}$	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV$_{DD}$	—
$\overline{\text{MCP}}$	AG19	I	OV$_{DD}$	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV$_{DD}$	—
IRQ[8]	AF19	I	OV$_{DD}$	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV$_{DD}$	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV$_{DD}$	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV$_{DD}$	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV$_{DD}$	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV$_{DD}$	5, 9
EC_MDIO	AC8	I/O	OV$_{DD}$	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV$_{DD}$	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV$_{DD}$	5, 9
TSEC1_COL	R4	I	LV$_{DD}$	—
TSEC1_CRS	V5	I/O	LV$_{DD}$	20
TSEC1_GTX_CLK	U7	O	LV$_{DD}$	—
TSEC1_RX_CLK	U3	I	LV$_{DD}$	—
TSEC1_RX_DV	V2	I	LV$_{DD}$	—
TSEC1_RX_ER	T1	I	LV$_{DD}$	—
TSEC1_TX_CLK	T6	I	LV$_{DD}$	—
TSEC1_TX_EN	U9	O	LV$_{DD}$	30
TSEC1_TX_ER	T7	O	LV$_{DD}$	—

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—
MDIC[0:1]	A19, B19	I/O	GV_{DD}	36

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV_{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11
Clock				
RTC	AF16	I	OV_{DD}	—
SYSCLK	AH17	I	OV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V,2.5 V)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 80. Memory Bus Clocking Specifications (MPC8543E)

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000 MHz			
	Min	Max		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

20.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 81:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, see the *PCI 2.2 Specification*.

Table 81. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	20:1
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Table 82. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	**25**	**33.33**	**41.66**	**66.66**	**83**	**100**	**111**	**133.33**
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500			
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533						
20	333	500							

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

Table 87. Part Numbering Nomenclature (continued)

MPC	*nnnnn*	*t*	*pp*	*ff*	*c*	*r*
Product Code	**Part Identifier**	**Temperature**	**Package[1, 2, 3]**	**Processor Frequency[4]**	**Core Frequency**	**Silicon Version**
MPC	8545E	Blank = 0 to 105°C C = –40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Notes:

1. See Section 19, “Package Description,” for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	• Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. • Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." • Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. • Removed Note from Section 5.1, "Power-On Ramp Rate". • Changed the Table 10 title to "Power Supply Ramp Rate". • Removed table 11. • Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. • Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" • Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. • Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)[1]" from 4 and 25 to 2 and 10 respectively .
8	04/2011	• Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." • Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. • Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	• In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." • Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	• In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. • In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. • In Table 13 deleted ramp rate requirement for XVDD/SVDD. • In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. • In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	• In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. • Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." • Added a reference to Revision 2.1.2. • Updated Table 55, "MII Management AC Timing Specifications." • Added Section 5.1, "Power-On Ramp Rate."