

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8543evuang

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

 Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
 - Flexible configuration.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
 - Four inbound windows plus a default window on RapidIO[™]
 - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
 - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface
 - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
 - DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
 - Full ECC support
 - Page mode support
 - Up to 16 simultaneous open pages for DDR

Overview

- AESU-Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

- VRRP and HSRP support for seamless router fail-over
- Up to 16 exact-match MAC addresses supported
- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
 - PCI 2.2 and PCI-X 1.0 compatible
 - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
 - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
 - Host and agent mode support
 - 64-bit dual address cycle (DAC) support
 - PCI-X supports multiple split transactions
 - Supports PCI-to-memory and memory-to-PCI streaming

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t _{SYSCLK}	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	_	—	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, I _{OH} = -1.0 mA)	V _{OH}	2.00	LV _{DD} /TV _{DD} + 0.3	V	
Output low voltage ($LV_{DD}/TV_{DD} = Min$, I _{OL} = 1.0 mA)	V _{OL}	GND –0.3	0.40	V	
Input high voltage	V _{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	
Input low voltage	V _{IL}	-0.3	0.90	V	
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	Ι _{ΙΗ}	_	10	μA	1, 2, 3
Input low current (V _{IN} = GND)	۱ _{IL}	-15	_	μÂ	3

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. $\mathsf{TV}_{\mathsf{DD}}$ supports eTSECs 3 and 4.

3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	AC Timing	Specifications
-------------	-----------	------------------	----------------

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t _{TRX}	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t _{SKTRX}	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t _{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t _{TRDXKH}	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t _{TRXR} ²	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t _{TRXF} ²	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}

2. Guaranteed by design.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	_	150	ps	7, 8
Input setup to local bus clock (except LGTA/UPWAIT)	t _{LBIVKH1}	1.9	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	_	2.1	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}		2.3	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}		2.4	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}		2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}		2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}		2.6	ns	5

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub></sub>

- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.



Figure 22. Local Bus AC Test Load

Local Bus



Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).





Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

Local Bus



Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Parameter	Symbol ¹	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.4	V

 Table 43. JTAG DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} in this case, represents the OV_{IN}

12.2 JTAG AC Electrical Specifications

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 32.

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	6
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25		ns	4

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹

PCI/PCI-X

Table 54. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the PCI-X 1.0a Specification.

- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the PCI-X 1.0a Specification.

- 10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
- 11. Guaranteed by characterization.

12. Guaranteed by design.

Serial RapidIO

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.



Figure 52. Transmitter Output Compliance Mask

Transmitter Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 65. Transmitter Differential Output Eye Diagram Parameters

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times$ (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling

18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100-\Omega \pm 5\%$ differential resistive load.



Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

Package Description

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	_
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	0	—	24

Table 71. MPC8548E Pinout Listing (continued)

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.

- 2. Recommend a weak pull-up resistor (2-10 kΩ) be placed on this pin to OV_{DD}.
- 3. A valid clock must be provided at POR if TSEC4_TXD[2] is set = 1.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- 10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 14.Internal thermally sensitive resistor.
- 15.No connections must be made to these pins if they are not used.
- 16. These pins are not connected for any use.
- 17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI1_C_BE[7:4]).
- 19.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 20. This pin is only an output in FIFO mode when used as Rx flow control.

24.Do not connect.

Package Description

Table 72	. MPC8547E	Pinout Listing	(continued)
----------	------------	-----------------------	-------------

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_	_	2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13		GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11		GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1		_	104
Reserved	R6	—	—	104
Reserved	P6		_	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV _{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	_	105
FIFO1_TXC2	P7	0	LV _{DD}	15
cfg_dram_type1	R10	0	LV _{DD}	5, 9
Thr	ee-Speed Ethernet Controller (Gigabit I	Ethernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_
TSEC3_GTX_CLK	W8	0	TV _{DD}	_
TSEC3_RX_CLK	W2	I	TV _{DD}	_
TSEC3_RX_DV	W1	I	TV _{DD}	_
TSEC3_RX_ER	Y2	I	TV _{DD}	_
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	0	TV _{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	_
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV _{DD}	—
TSEC3_CRS	AA3	I/O	TV _{DD}	31
TSEC3_TX_ER	AB6	0	TV _{DD}	—
	DUART	1		
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	_
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	_
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	—
	I ² C interface	1 1		
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27

Table 74. MPC8543E Pinout Listing (continued)

Ordering Information

MPC	nnnnn	t	рр	ff	C	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8545E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Table 87. Part Numbering Nomenclature (continued)

Notes:

1. See Section 19, "Package Description," for more information on available package types.

2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.

- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.