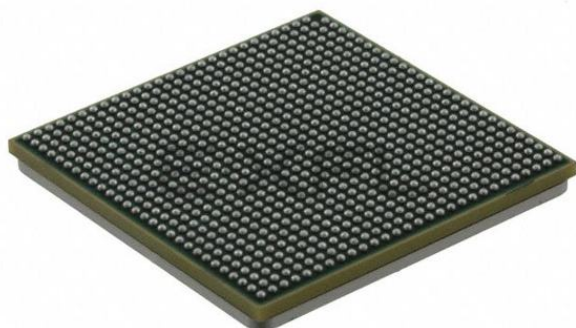




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8543hxaqg

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four controllers designed to comply with IEEE Std. 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations. See [Section 8.1, “Enhanced Three-Speed Ethernet Controller \(eTSEC\) \(10/100/1Gb Mbps\)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics,”](#) for more information.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

Table 4. Device Power Dissipation

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$.
3. Typical-65 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$, running Dhrystone.
4. Typical-105 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running Dhrystone.
5. Maximum is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running a smoke test.

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see [Table 2](#)) with $OV_{DD} = 3.3\text{ V} \pm 165\text{ mV}$.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	16	—	133	MHz	1 , 6 , 7 , 8
SYSCLK cycle time	t_{SYSCLK}	7.5	—	60	ns	6 , 7 , 8
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4 , 5

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2](#), “CCB/SYSCLK PLL Ratio,” and [Section 20.3](#), “e500 Core PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth must be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
7. For spread spectrum clocking. Guidelines are + 0% to –1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{\text{CCB}}$, and minimum clock low time is $2 \times t_{\text{CCB}}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8548E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 19](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

[Figure 3](#) shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

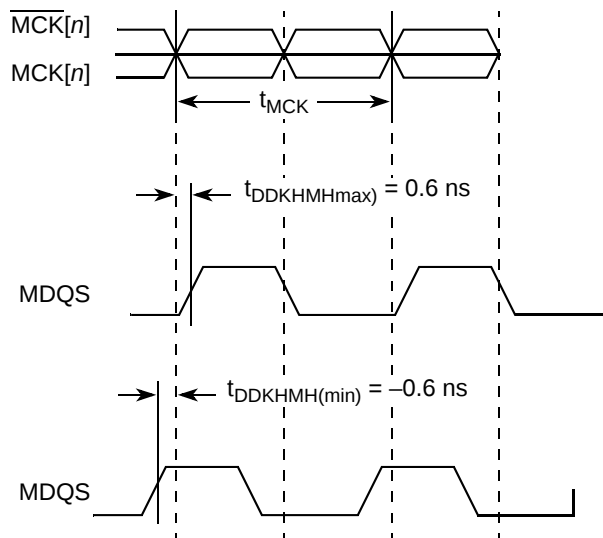
**Figure 3. Timing Diagram for t_{DDKHMH}**

Figure 14 shows the TBI transmit AC timing diagram.

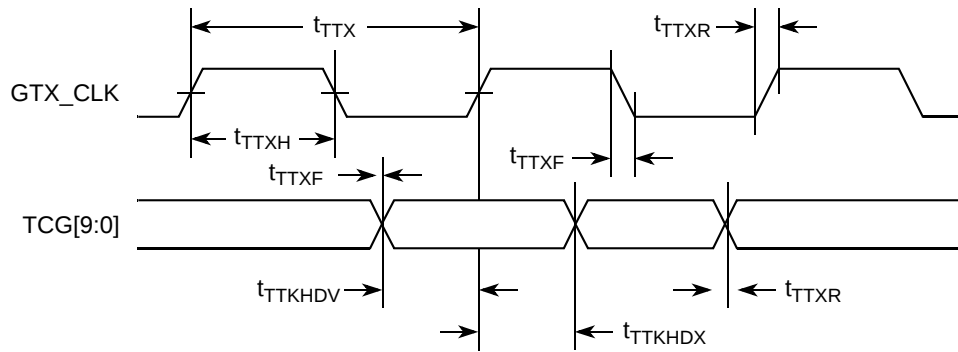


Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 31. TBI Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSECn_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns
TSECn_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSECn_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSECn_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
TSECn_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}^2	0.7	—	2.4	ns
TSECn_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}^2	0.7	—	2.4	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in “[Section 8, “Enhanced Three-Speed Ethernet \(eTSEC\).”](#)”

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 36. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.10	$OV_{DD} + 0.3$	V
Output low voltage ($OV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current ($OV_{DD} = \text{Max}$, $V_{IN}^1 = 2.1 \text{ V}$)	I_{IH}	—	40	μA
Input low current ($OV_{DD} = \text{Max}$, $V_{IN} = 0.5 \text{ V}$)	I_{IL}	-600	—	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V $\pm$ 5%.

Parameter	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t_{MDC}	120.5	—	1389	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16 \times t_{CCB}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{CCB} \times 8) - 3$	—	$(16 \times t_{CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.

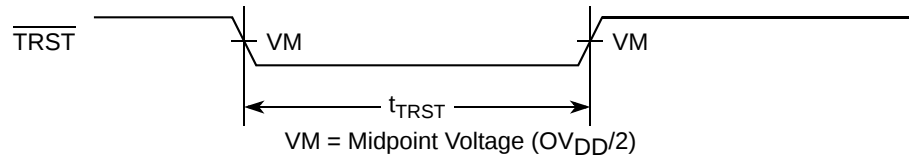


Figure 31. $\overline{\text{TRST}}$ Timing Diagram

Figure 32 provides the boundary-scan timing diagram.

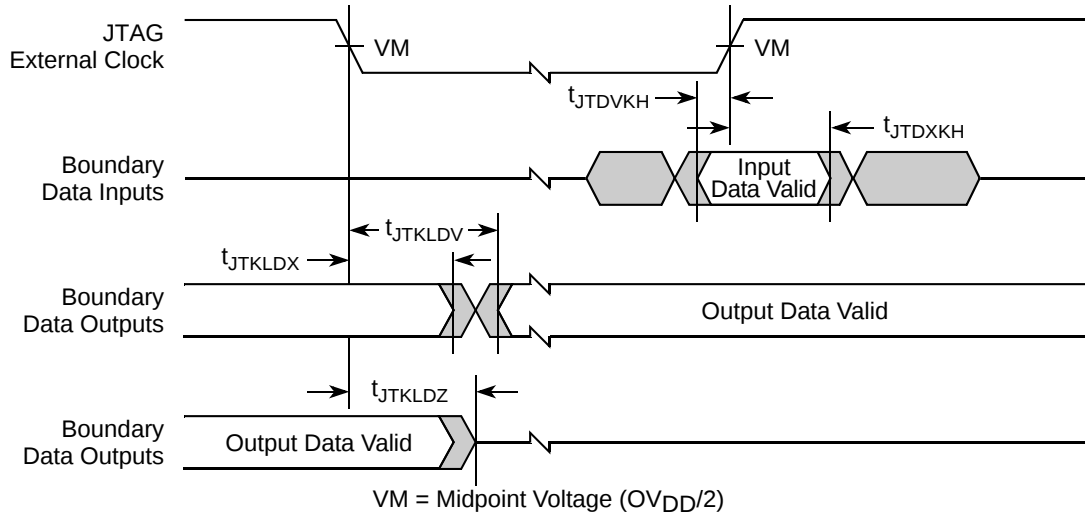


Figure 32. Boundary-Scan Timing Diagram

Table 46. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

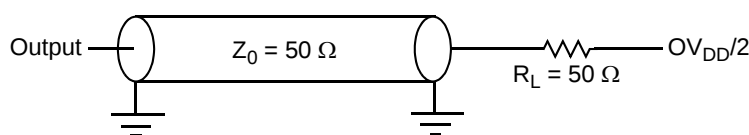
Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the $V_{IH}(\text{min})$ of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I²C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I ² C source clock frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR bit setting	0x2A	0x05	0x26	0x00
Actual FDR divider selected	896	704	512	384
Actual I ² C SCL frequency generated	371 kHz	378 kHz	390 kHz	346 kHz

For the detail of I²C frequency calculation, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919). Note that the I²C source clock frequency is half of the CCB clock frequency for the device.
- The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- Guaranteed by design.

Figure 33 provides the AC test load for the I²C.

Figure 33. I²C AC Test Load

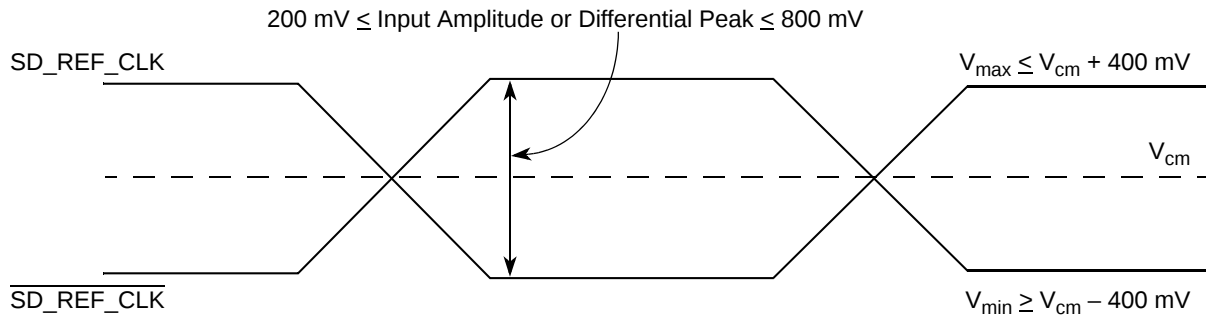


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

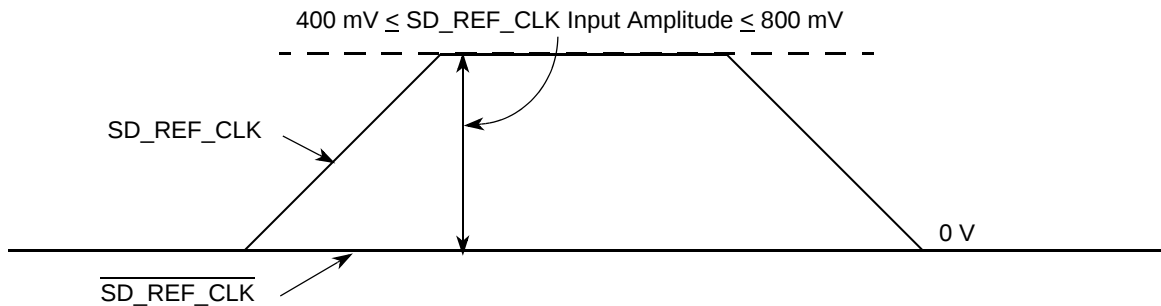


Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D– TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} + V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$ V_{TX-CM-DC}(\text{during L0}) + V_{TX-CM-Idle-DC}(\text{during electrical idle}) \leq 100$ mV $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [L0] $V_{TX-CM-Idle-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D–	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = \text{DC}_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = \text{DC}_{(avg)}$ of $ V_{TX-D-} $. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S_{11} , of the transmitter in each case shall be better than:

- -10 dB for $(\text{baud frequency})/10 < \text{Freq}(f) < 625$ MHz, and
- -10 dB + $10\log(f/625 \text{ MHz})$ dB for $625 \text{ MHz} \leq \text{Freq}(f) \leq \text{baud frequency}$

The reference impedance for the differential return loss measurements is $100\text{-}\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 59. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	−0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\text{-}\Omega \pm 5\%$ differential resistive load.

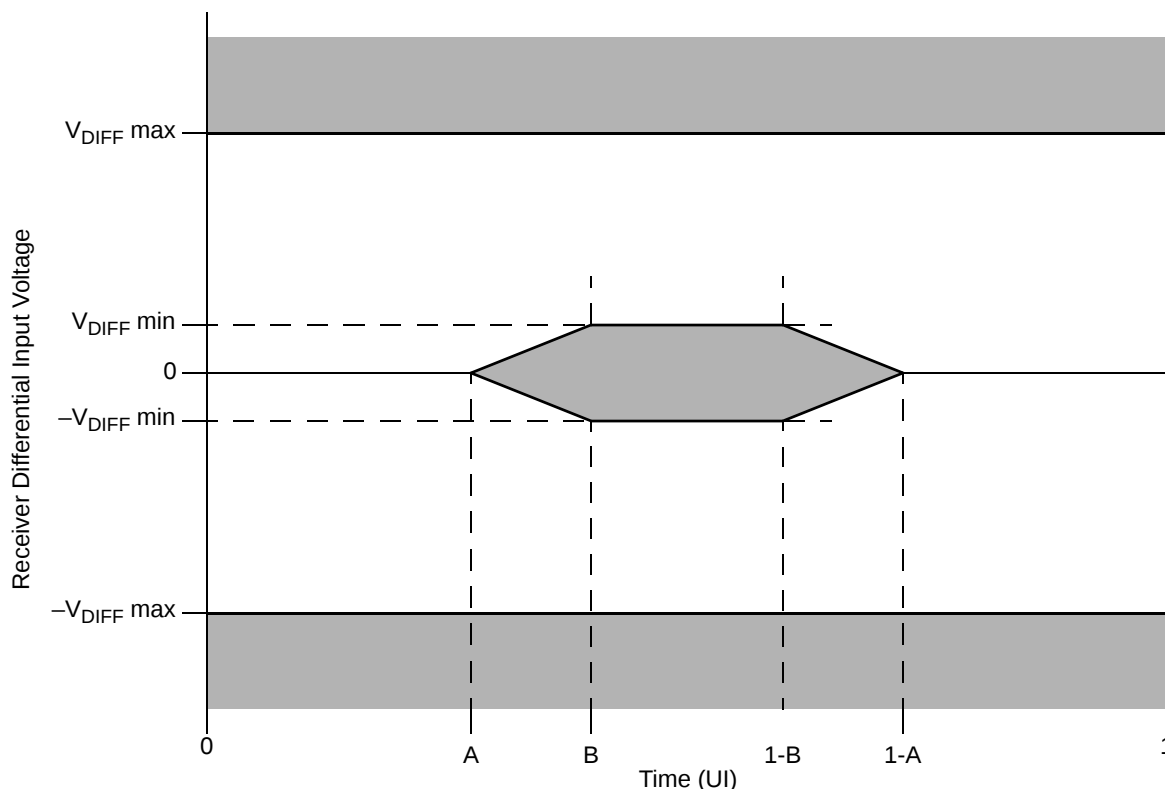


Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

19.3 Pinout Listings

NOTE

The $\overline{\text{DMA_DACK}}[0:1]$ and $\overline{\text{TEST_SEL}}/\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on $\text{PCI1_AD}[63:32]/\text{PC2_AD}[31:0]$ pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

Table 71. MPC8548E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
$\text{PCI1_AD}[63:32]/\text{PCI2_AD}[31:0]$	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
$\text{PCI1_AD}[31:0]$	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[7:4]/\text{PCI2_C_}\overline{\text{BE}}[3:0]$	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[3:0]$	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
$\text{PCI1_PAR64}/\text{PCI2_PAR}$	W15	I/O	OV_{DD}	
$\overline{\text{PCI1_GNT}}[4:1]$	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1_TRDY}}$	AG11	I/O	OV_{DD}	2

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	O	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	O	LV _{DD}	30
TSEC1_TX_ER	T7	O	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV _{DD}	5, 9, 33
TSEC2_COL	P1	I	LV _{DD}	—
TSEC2_CRS	R6	I/O	LV _{DD}	20
TSEC2_GTX_CLK	P6	O	LV _{DD}	—
TSEC2_RX_CLK	N4	I	LV _{DD}	—
TSEC2_RX_DV	P5	I	LV _{DD}	—
TSEC2_RX_ER	R1	I	LV _{DD}	—
TSEC2_TX_CLK	P10	I	LV _{DD}	—
TSEC2_TX_EN	P7	O	LV _{DD}	30

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	—
$\overline{\text{SD_REF_CLK}}$	T27	I	XV _{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV _{DD}	—
$\overline{\text{HRESET_REQ}}$	AG16	O	OV _{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV _{DD}	—
$\overline{\text{CKSTP_IN}}$	AA9	I	OV _{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11
Clock				
RTC	AF16	I	OV _{DD}	—
SYSCLK	AH17	I	OV _{DD}	—
JTAG				
TCK	AG28	I	OV _{DD}	—
TDI	AH28	I	OV _{DD}	12
TDO	AF28	O	OV _{DD}	—
TMS	AH27	I	OV _{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV _{DD}	12

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_TX[0:3]	M23, N21, P23, R21	O	XV _{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	—
SD_REF_CLK	T27	I	XV _{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
HRESET	AG17	I	OV _{DD}	—
HRESET_REQ	AG16	O	OV _{DD}	29
SRESET	AG20	I	OV _{DD}	—
CKSTP_IN	AA9	I	OV _{DD}	—
CKSTP_OUT	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11
Clock				
RTC	AF16	I	OV _{DD}	—
SYSCLK	AH17	I	OV _{DD}	—
JTAG				
TCK	AG28	I	OV _{DD}	—
TDI	AH28	I	OV _{DD}	12

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PCI1_TRDY}}$	AG11	I/O	OV _{DD}	2
$\overline{\text{PCI1_REQ}}[4:1]$	AH2, AG4, AG3, AH4	I	OV _{DD}	—
$\overline{\text{PCI1_REQ0}}$	AH3	I/O	OV _{DD}	—
$\overline{\text{PCI1_CLK}}$	AH26	I	OV _{DD}	39
$\overline{\text{PCI1_DEVSEL}}$	AH11	I/O	OV _{DD}	2
$\overline{\text{PCI1_FRAME}}$	AE11	I/O	OV _{DD}	2
$\overline{\text{PCI1_IDSEL}}$	AG9	I	OV _{DD}	—
cfg_pci1_width	AF14	I/O	OV _{DD}	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
$\overline{\text{MDQS}}[0:8]$	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV _{DD}	—
MBA[0:2]	F7, J7, M11	O	GV _{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MWE}}$	E7	O	GV _{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV _{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV _{DD}	11
$\overline{\text{MCS}}[0:3]$	K8, J8, G8, F8	O	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV _{DD}	—
$\overline{\text{MCK}}[0:5]$	J9, A15, G1, L9, B14, F2	O	GV _{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	O	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV _{DD}	5, 7, 9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV _{DD}	—
$\overline{\text{LCS5/DMA_DREQ2}}$	D23	I/O	BV _{DD}	1
$\overline{\text{LCS6/DMA_DACK2}}$	G20	O	BV _{DD}	1
$\overline{\text{LCS7/DMA_DDONE2}}$	E21	O	BV _{DD}	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV _{DD}	5, 9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV _{DD}	5, 9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV _{DD}	5, 9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV _{DD}	5, 9
LALE	H24	O	BV _{DD}	5, 8, 9
LBCTL	G27	O	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV _{DD}	5, 9
LGPL1/LSDWE	G22	O	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	O	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	O	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—
LGPL5	E26	O	BV _{DD}	5, 9
LCKE	E24	O	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV _{DD}	—

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD_TX}}$ [7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}$ [7:0]
- SD_REF_CLK
- $\overline{\text{SD_REF_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin `cfg_srds_en` on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD_TX}}$ [7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}$ [7:0]
- SD_REF_CLK

Table 87. Part Numbering Nomenclature (continued)

MPC	nnnnn	t	pp	ff	c	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8545E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Notes:

1. See [Section 19, "Package Description,"](#) for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.