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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8543vjangd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Power Characteristics

Power Characteristics 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Table 4. Device Power Dissipation

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on V_{DD} = 1.1 V, T_i = 65°C.

3. Typical-65 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 65^{\circ}\text{C}$, running Dhrystone. 4. Typical-105 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running Dhrystone. 5. Maximum is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running a smoke test.

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t _{SYSCLK}	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	_	—	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = min$, $I_{OH} = -4.0 mA$)	V _{OH}	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	_
Output low voltage ($LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA$)	V _{OL}	GND	0.50	V	_
Input high voltage	V _{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	_
Input low voltage	V _{IL}	-0.3	0.90	V	_
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IH}	—	40	μΑ	1, 2, 3
Input low current (V _{IN} = GND)	IIL	-600	_	μA	

Table 22.	GMII. MI	I. RMII. a	and TBI DC	Electrical	Characteristics
	O min, mi	.,		Licothour	onaraotoristios

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. TV_DD supports eTSECs 3 and 4.

3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Local Bus



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Parameter	Symbol ¹	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.4	V

 Table 43. JTAG DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} in this case, represents the OV_{IN}

12.2 JTAG AC Electrical Specifications

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 32.

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	6
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0		ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25		ns	4

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹

Parar	Symbol ²	Min	Мах	Unit	Notes	
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	4 2	20 10	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	30 30		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO		t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

 Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.



Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.



Figure 30. JTAG Clock Input Timing Diagram

3.	The maximum t _{I2DXKL}	has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal	al.

For the detail of I²C frequency calculation, see Determining the I²C Frequency Divider Ratio for SCL (AN2919). Note that the

200 MHz

390 kHz

0x26

512

133 MHz

346 kHz

0x00

384

4. Guaranteed by design.

FDR bit setting

I²C source clock frequency

Actual FDR divider selected

Actual I²C SCL frequency generated

Figure 33 provides the AC test load for the I^2C .



Figure 33. I²C AC Test Load

57

Table 46. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	—	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I²C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

266 MHz

378 kHz

0x05

704

333 MHz

0x2A

371 kHz

896

I²C source clock frequency is half of the CCB clock frequency for the device.

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.



Figure 46. Single-Ended Connection (Reference Only)

Table 56. Differential Transmitter	· (TX) Output	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{TX-DC-CM}	The TX DC common mode voltage	0	_	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX short circuit current limit	_	_	90	mA	The total current the transmitter can provide when shorted to its ground
T _{TX-IDLE-MIN}	Minimum time spent in electrical idle	50	_		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
RL _{TX-DIFF}	Differential return loss	12	_	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL _{TX-CM}	Common mode return loss	6		—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z _{TX-DIFF-DC}	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z _{TX-DC}	Transmitter DC impedance	40	_	_	Ω	Required TX D+ as well as D– DC impedance during all states
L _{TX-SKEW}	Lane-to-lane output skew	_	_	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C _{TX}	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
L _{TX-SKEW}	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in Figure 49). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to $-{300 \text{ mV}}$ and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 50) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 49) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

Serial RapidIO

Table 60. Short Run Transmitter	AC Timing Specifications-	–2.5 GBaud
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Characteristic	Symbol	Range		Unit	Nataa	
Characteristic	Symbol	Min	Max	Unit	Notes	
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair	
Differential output voltage	V _{DIFFPP}	500	1000	mV p-p	_	
Deterministic jitter	J _D	—	0.17	UI p-p	_	
Total jitter	J _T	—	0.35	UI p-p	_	
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit interval	UI	400	400	ps	±100 ppm	

Table 61. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notos	
Characteristic	Symbol	Min	Max	Onic	NOIES	
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair	
Differential output voltage	V _{DIFFPP}	500	1000	mVp-p	_	
Deterministic jitter	J _D	_	0.17	UI p-p	_	
Total jitter	J _T	_	0.35	UI p-p	_	
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of multilane link	
Unit interval	UI	320	320	ps	±100 ppm	

Table 62. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notos	
	Symbol	Min	Max	Onic	Notes	
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair	
Differential output voltage	V _{DIFFPP}	800	1600	mVp-p	-	
Deterministic jitter	J _D	—	0.17	UI p-p	_	
Total jitter	J _T	—	0.35	UI p-p	_	
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes o multilane link	
Unit interval	UI	800	800	ps	±100 ppm	

Serial RapidIO

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.



Figure 52. Transmitter Output Compliance Mask

Transmitter Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 65. Transmitter Differential Output Eye Diagram Parameters

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times$ (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling

This section details package parameters, pin assignments, and dimensions.

19.1 Package Parameters

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are provided in Table 70.

Parameter	CBGA ¹	PBGA ²
Package outline	29 mm × 29 mm	29 mm × 29 mm
Interconnects	783	783
Ball pitch	1 mm	1 mm
Ball diameter (typical)	0.6 mm	0.6 mm
Solder ball	63% Sn	63% Sn
	37% Pb	37% Pb
	0% Ag	0% Ag
Solder ball (lead-free)	95% Sn	96.5% Sn
	4.5% Ag	3.5% Ag
	0.5% Cu	

Table 70. Package Parameters

Notes:

1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

2. The FC-PBGA package is available on only versions 2.1.1 and 2.1.2, and 3.0 of the device.

Signal	Package Pin Number	Pin Type	Power Supply	Notes					
	I ² C interface			•					
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27					
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27					
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27					
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27					
	SerDes			•					
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}						
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—					
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—					
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—					
SD_PLL_TPD	U28	0	XV _{DD}	24					
SD_REF_CLK	T28	I	XV _{DD}	3					
SD_REF_CLK	T27	I	XV _{DD}	3					
Reserved	AC1, AC3	—	—	2					
Reserved	M26, V28	_	_	32					
Reserved	M25, V27	—	_	34					
Reserved	M20, M21, T22, T23	—	—	38					
General-Purpose Output									
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	I XV _{DD}						
	System Control								
HRESET	AG17	I	OV _{DD}	_					
HRESET_REQ	AG16	0	OV _{DD}	29					
SRESET	AG20	I	OV _{DD}						
CKSTP_IN	AA9	I	OV _{DD}	—					
CKSTP_OUT	AA8	0	OV _{DD}	2, 4					
	Debug								
TRIG_IN	AB2	I	OV _{DD}	—					
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29					
MSRCID[0:1]	AE4, AG2 O OV		OV _{DD}	5, 6, 9					
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29					
MDVAL	AE5	0	OV _{DD}	6					
CLK_OUT	AE21	0	OV _{DD}	11					

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
Reserved	U20, V22, W20, Y22	_	—	15				
Reserved	U21, V23, W21, Y23	—	—	15				
SD_PLL_TPD	U28	0	XV _{DD}	24				
SD_REF_CLK	T28	I	XV _{DD}	—				
SD_REF_CLK	T27	I	XV _{DD}	—				
Reserved	AC1, AC3	—	—	2				
Reserved	M26, V28	—	—	32				
Reserved	M25, V27	—	—	34				
Reserved	M20, M21, T22, T23	—	—	38				
	General-Purpose Output							
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	_				
	System Control							
HRESET	AG17	I	OV _{DD}	_				
HRESET_REQ	AG16	0	OV _{DD}	29				
SRESET	AG20	I	OV _{DD}	_				
CKSTP_IN	AA9	I	OV _{DD}	_				
CKSTP_OUT	AA8	0	OV _{DD}	2, 4				
	Debug							
TRIG_IN	AB2	I	OV _{DD}	—				
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29				
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9				
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29				
MDVAL	AE5	0	OV _{DD}	6				
CLK_OUT	AE21	0	OV _{DD}	11				
	Clock							
RTC	AF16	I	OV _{DD}	—				
SYSCLK	AH17	I	OV _{DD}	—				
	JTAG							
ТСК	AG28	I	OV _{DD}	—				
TDI	AH28	Ι	OV _{DD}	12				
TDO	AF28	0	OV _{DD}	_				
TMS	AH27	I	OV _{DD}	12				
TRST	AH23	Ι	OV _{DD}	12				

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)		1		
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17	
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17	
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17	
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17	
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35	
PCI1_GNT0	AG5	I/O	OV _{DD}	—	
PCI1_IRDY	AF11	I/O	OV _{DD}	2	
PCI1_PAR	AD12	I/O	OV _{DD}	—	
PCI1_PERR	AC12	I/O	OV _{DD}	2	
PCI1_SERR	V13	I/O	OV _{DD}	2, 4	
PCI1_STOP	W12	I/O	OV _{DD}	2	
PCI1_TRDY	AG11	I/O	OV _{DD}	2	
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	Ι	OV _{DD}	—	
PCI1_REQ0	AH3	I/O	OV _{DD}	—	
PCI1_CLK	AH26	I	OV _{DD}	39	
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2	

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)	•	
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	T7	0	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4			105

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4		OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
cfg_pci1_width	AF14	I/O	OV _{DD}	112
Reserved	V15		—	110
Reserved	AE28	_		2
Reserved	AD26		—	110
Reserved	AD25		—	110
Reserved	AE26		—	110
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_	_	101
Reserved	AE25	_		110
Reserved	AG25		—	110
Reserved	AD24	_	—	110
Reserved	AF24	_	—	110
Reserved	AD27	_	_	110
Reserved	AD28, AE27, W17, AF26		—	110
Reserved	AH25		—	110
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	—
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 74. MPC8543E Pinout Listing (continued)

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout