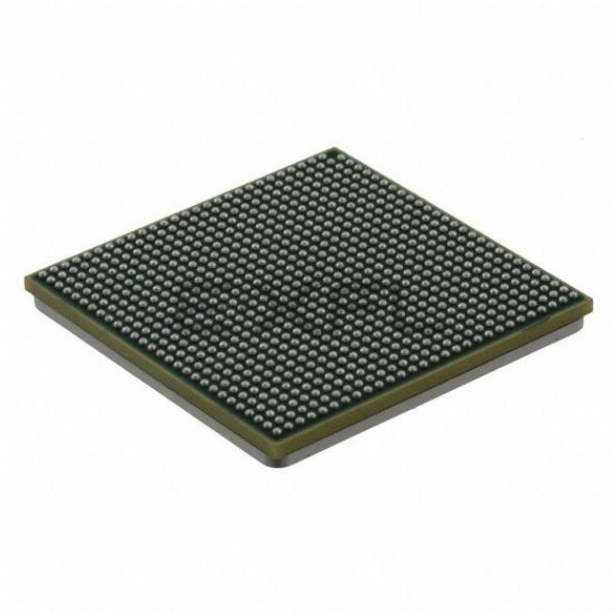

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8543vtangb

  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  - PCI 2.2 and PCI-X 1.0 compatible
  - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
3. The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
4. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage		AV_{DD}	1.1 V ± 55 mV	V	1
Core power supply for SerDes transceivers		SV_{DD}	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.1 V ± 55 mV	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	—	4
PCI/PCI-X, DUART, system control and power management, I^2C, Ethernet MII management, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, Ethernet MII management, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3

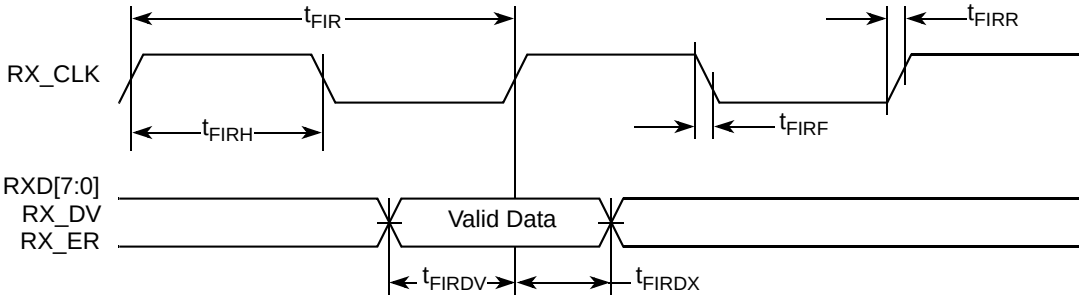


Figure 7. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%–80%)	t_{GTXR}[2]	—	—	1.0	ns
GTX_CLK data clock fall time (80%–20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 shows the GMII receive AC timing diagram.

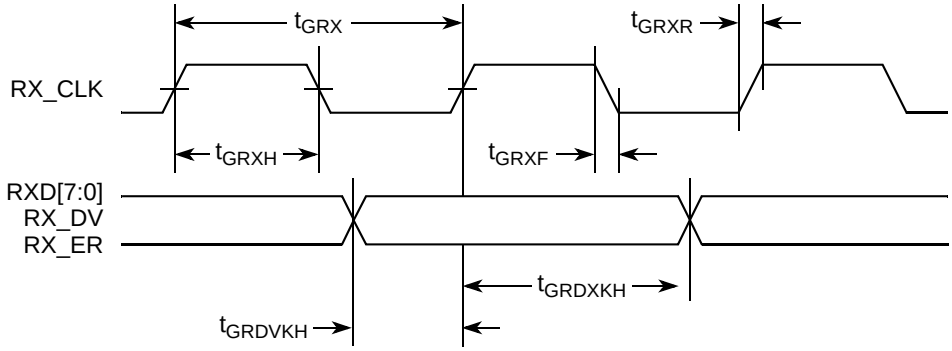


Figure 10. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 28. MII Transmit AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 17 shows the RGMII and RTBI AC timing and multiplexing diagrams.

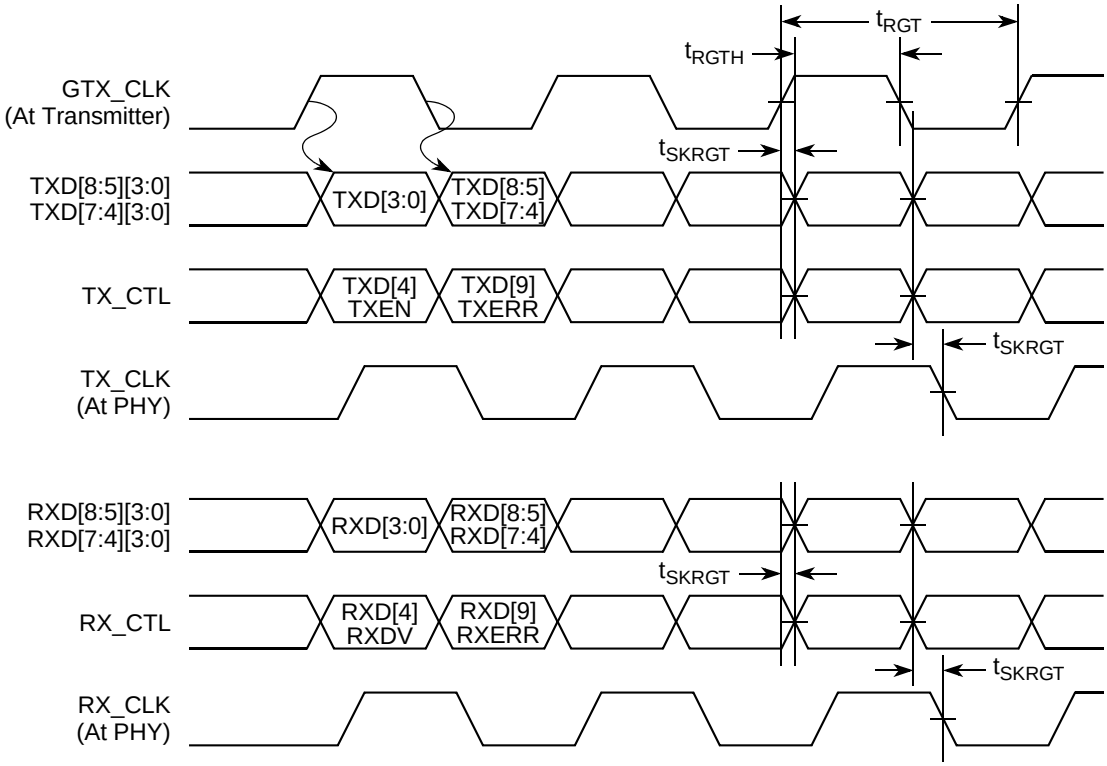


Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII Transmit AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 36. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN}[1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t_{MDC}	120.5	—	1389	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16 \times t_{CCB}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{CCB} \times 8) - 3$	—	$(16 \times t_{CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/UPWAIT)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

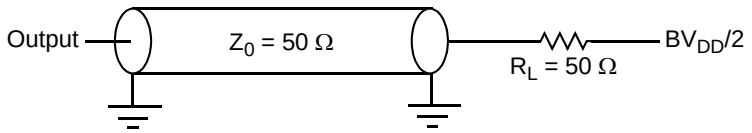


Figure 22. Local Bus AC Test Load

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCI*n*_CLK when it is configured for asynchronous mode.

— The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.

— For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

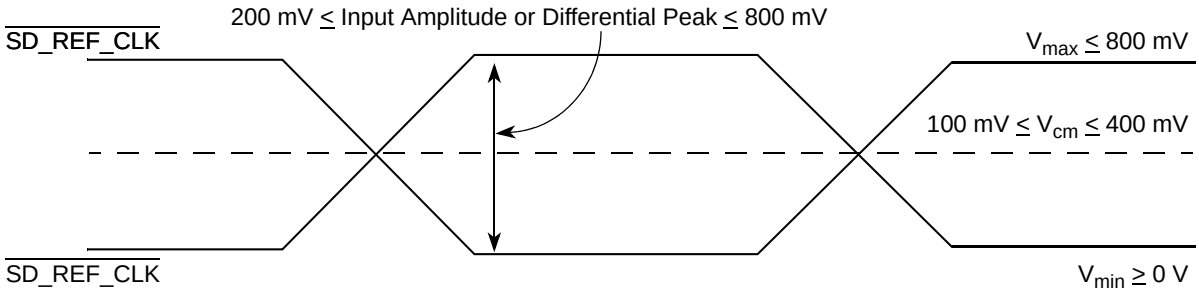


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

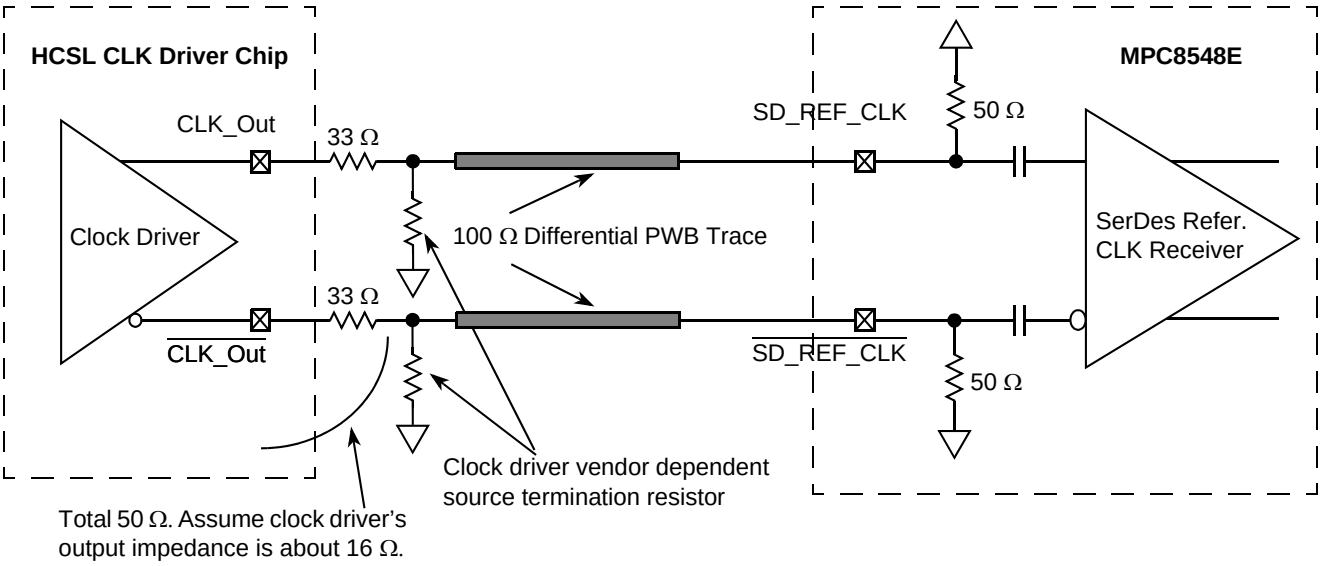


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

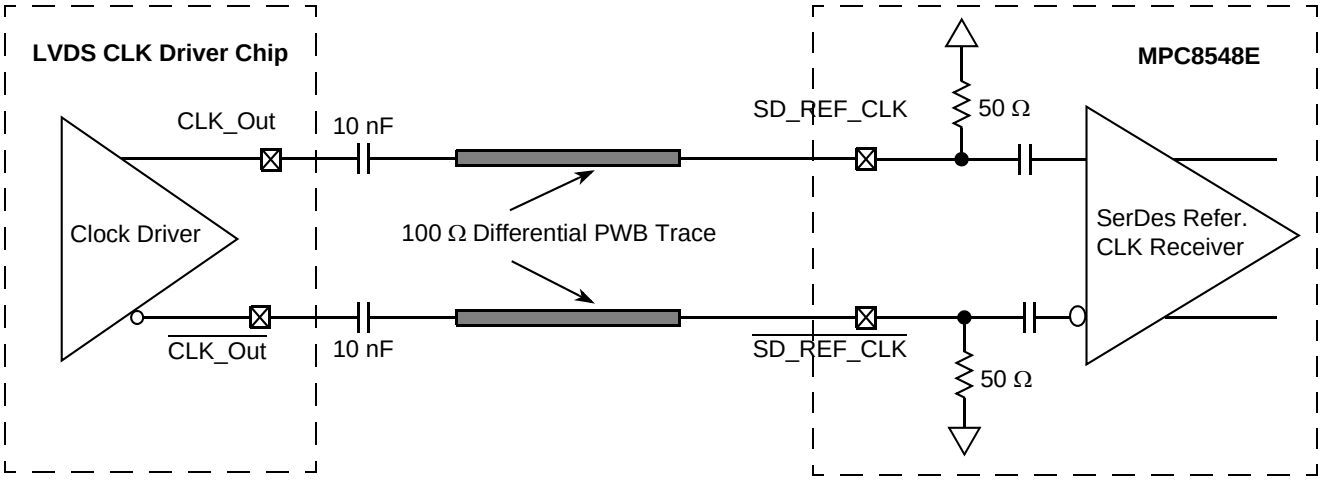


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

Note:
1. Typical based on *PCI Express Specification 2.0*.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a*.

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

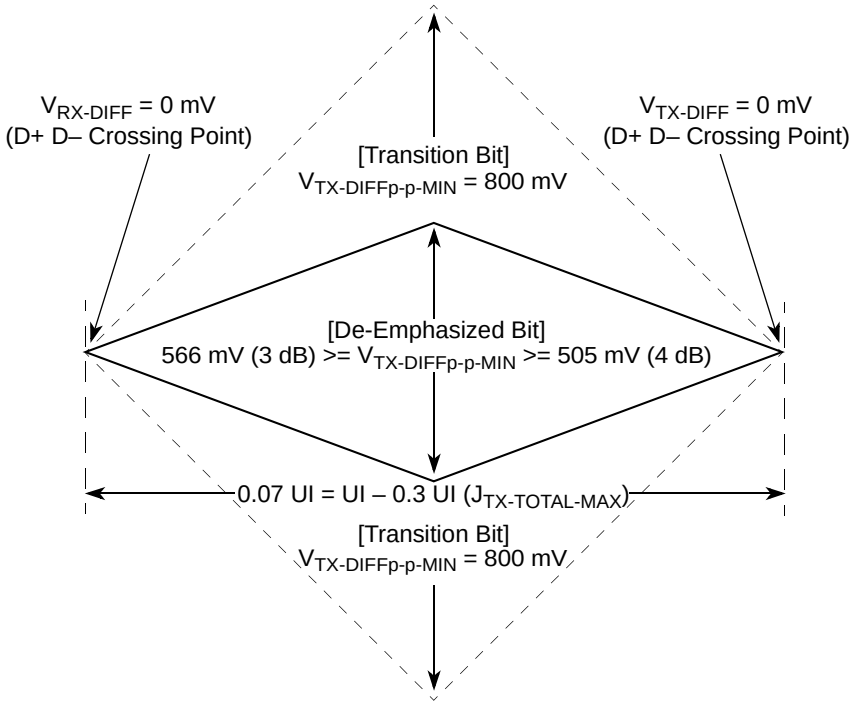


Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$. See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

Table 63. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	800	1600	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 64. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	800	1600	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 52 with the parameters specified in Table 65 when measured at the output pins of the device and the device is driving a 100-Ω ± 5% differential resistive load. The output eye pattern of an LP-serial

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—
MDIC[0:1]	A19, B19	I/O	GV_{DD}	36

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV_{DD}	25
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV_{DD}	—

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	O	AVDD_SRDS	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1000 MHz		1200 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 76. Processor Core Clocking Specifications (MPC8545E)

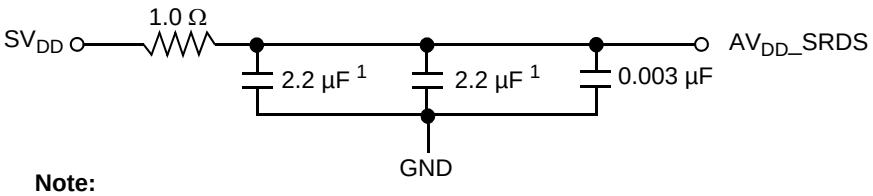
Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system