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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8545ehxang

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- VRRP and HSRP support for seamless router fail-over
- Up to 16 exact-match MAC addresses supported
- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  - PCI 2.2 and PCI-X 1.0 compatible
  - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming

**Power Characteristics** 

#### **Power Characteristics** 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency <sup>1</sup>	Core Frequency	SLEEP <sup>2</sup>	Typical-65 <sup>3</sup>	Typical-105 <sup>4</sup>	Maximum <sup>5</sup>	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

## **Table 4. Device Power Dissipation**

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on  $V_{DD}$  = 1.1 V,  $T_i$  = 65°C.

3. Typical-65 is based on  $V_{DD} = 1.1 \text{ V}$ ,  $T_j = 65^{\circ}\text{C}$ , running Dhrystone. 4. Typical-105 is based on  $V_{DD} = 1.1 \text{ V}$ ,  $T_j = 105^{\circ}\text{C}$ , running Dhrystone. 5. Maximum is based on  $V_{DD} = 1.1 \text{ V}$ ,  $T_j = 105^{\circ}\text{C}$ , running a smoke test.

# 4 Input Clocks

This section discusses the timing for the input clocks.

# 4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

## Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$ .

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f <sub>SYSCLK</sub>	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t <sub>SYSCLK</sub>	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t <sub>KHK</sub> /t <sub>SYSCLK</sub>	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{CCB}$ , and minimum clock low time is  $2 \times t_{CCB}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.

# 8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

## 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV <sub>DD</sub> TV <sub>DD</sub>	3.13	3.47	V	1, 2
Output high voltage ( $LV_{DD}/TV_{DD} = min$ , $I_{OH} = -4.0 mA$ )	V <sub>OH</sub>	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	_
Output low voltage ( $LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA$ )	V <sub>OL</sub>	GND	0.50	V	_
Input high voltage	V <sub>IH</sub>	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	_
Input low voltage	V <sub>IL</sub>	-0.3	0.90	V	_
Input high current ( $V_{IN} = LV_{DD}$ , $V_{IN} = TV_{DD}$ )	I <sub>IH</sub>	—	40	μΑ	1, 2, 3
Input low current (V <sub>IN</sub> = GND)	IIL	-600	_	μA	

Table 22.	GMII. MI	I. RMII. a	and TBI DC	Electrical	Characteristics
	<b>O</b> min, mi	.,		Licothour	onaraotoristios

Notes:

1.  $LV_{DD}$  supports eTSECs 1 and 2.

2.  $\mathsf{TV}_\mathsf{DD}$  supports eTSECs 3 and 4.

3. The symbol V<sub>IN</sub>, in this case, represents the LV<sub>IN</sub> and TV<sub>IN</sub> symbols referenced in Table 1 and Table 2.

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t <sub>RMTDX</sub>	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>MTKHDX</sub> symbolizes MII transmit timing (MT) for the time t<sub>MTX</sub> clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t<sub>MTX</sub> represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

## Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

## 8.2.7.2 RMII Receive AC Timing Specifications

## Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t <sub>RMR</sub>	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t <sub>RMRH</sub>	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t <sub>RMRJ</sub>	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t <sub>RMRR</sub>	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t <sub>RMRF</sub>	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t <sub>RMRDV</sub>	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t <sub>RMRDX</sub>	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>MRDVKH</sub> symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>MRDXKL</sub> symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>MRX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>MRX</sub> represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub></sub>

# **10.2 Local Bus AC Electrical Specifications**

This table describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	12	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.3	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.5	ns	5

## Table 40. Local Bus Timing Parameters (BV<sub>DD</sub> = 3.3 V)—PLL Enabled

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

#### Local Bus



Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

#### Local Bus



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

3.	The maximum t <sub>I2DXKL</sub>	has only to be met if the device does not stretch the LOW period $(t_{\text{I2CL}})$ of the SCL signal	al.

For the detail of I<sup>2</sup>C frequency calculation, see Determining the I<sup>2</sup>C Frequency Divider Ratio for SCL (AN2919). Note that the

200 MHz

390 kHz

0x26

512

133 MHz

346 kHz

0x00

384

#### 4. Guaranteed by design.

FDR bit setting

I<sup>2</sup>C source clock frequency

Actual FDR divider selected

Actual I<sup>2</sup>C SCL frequency generated

Figure 33 provides the AC test load for the  $I^2C$ .



Figure 33. I<sup>2</sup>C AC Test Load

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## Table 46. I<sup>2</sup>C AC Electrical Specifications (continued)

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	$0.2 \times OV_{DD}$	—	V	_

#### Notes:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>12DVKH</sub> symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>12SXKL</sub> symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t<sub>12C</sub> clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V<sub>IH</sub>(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I<sup>2</sup>C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I<sup>2</sup>C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I<sup>2</sup>C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

266 MHz

378 kHz

0x05

704

333 MHz

0x2A

371 kHz

896

I<sup>2</sup>C source clock frequency is half of the CCB clock frequency for the device.

#### PCI/PCI-X

Figure 36 shows the PCI/PCI-X input AC timing conditions.



Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.





Table 53 provides the PCI-X AC timing specifications at 66 MHz.

	Table 53	. PCI-X AC	Timing	<b>Specifications</b>	at 66	MHz
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Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	<sup>t</sup> PCKHOV	_	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t <sub>PCKHOX</sub>	0.7		ns	1, 10
SYSCLK to output high impedance	t <sub>PCKHOZ</sub>	-	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t <sub>PCIVKH</sub>	1.7	_	ns	3, 5
Input hold time from SYSCLK	t <sub>PCIXKH</sub>	0.5	_	ns	10
REQ64 to HRESET setup time	t <sub>PCRVRH</sub>	10	_	clocks	11
HRESET to REQ64 hold time	t <sub>PCRHRX</sub>	0	50	ns	11
HRESET high to first FRAME assertion	t <sub>PCRHFV</sub>	10	_	clocks	9, 11
PCI-X initialization pattern to HRESET setup time	<sup>t</sup> PCIVRH	10	_	clocks	11

#### High-Speed Serial Interfaces (HSSI)

- The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND\_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND\_SRDSn). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
  - The reference clock can also be single-ended. The SD\_REF\_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from  $V_{min}$  to  $V_{max}$ ) with SD\_REF\_CLK either left unconnected or tied to ground.
  - The SD\_REF\_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DCor AC-coupled into the unused phase (SD\_REF\_CLK) through the same source impedance as the clock input (SD\_REF\_CLK) in use.



Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

#### High-Speed Serial Interfaces (HSSI)

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.





Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50- $\Omega$  termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50  $\Omega$ . R1 is used to DC-bias the LVPECL outputs prior

#### PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

## NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- $\Omega$  probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

## 17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

## NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 50. Compliance Test/Measurement Load

# 18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and  $\overline{TD}$ ) or a receiver input (RD and  $\overline{RD}$ ). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD,  $\overline{\text{TD}}$ , RD, and  $\overline{\text{RD}}$  each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter,  $V_{OD}$ , is defined as  $V_{TD} V_{\overline{TD}}$ .
- 3. The differential input signal of the receiver,  $V_{ID}$ , is defined as  $V_{RD} V_{\overline{RD}}$ .
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is  $2 \times (A B)$  volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

# 18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Table 71	. MPC8548E	<b>Pinout Listing</b>	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Clock				
RTC	AF16	I	OV <sub>DD</sub>	—
SYSCLK	AH17	I	OV <sub>DD</sub>	—
	JTAG			
ТСК	AG28	I	OV <sub>DD</sub>	—
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	0	OV <sub>DD</sub>	—
TMS	AH27	ļ	OV <sub>DD</sub>	12
TRST	AH23	I	OV <sub>DD</sub>	12
	DFT			
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
LSSD_MODE	AH20	I	OV <sub>DD</sub>	25
TEST_SEL	AH14	I	OV <sub>DD</sub>	25
	Thermal Management			
THERM0	AG1	—	—	14
THERM1	AH1	—	_	14
	Power Management			
ASLEEP	AH18	0	OV <sub>DD</sub>	9, 19, 29
	Power and Ground Signals			
GND	<ul> <li>A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17,</li> <li>F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27,</li> <li>L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13,</li> <li>U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27,</li> <li>K28, L24, L26, N24, N27, P25, R28, T24, T26,</li> <li>U24, V25, W28, Y24, Y26, AA24, AA27, AB25,</li> <li>AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27</li> </ul>	_	_	_
OV <sub>DD</sub>	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV <sub>DD</sub>	—

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	_
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	0	—	24

#### Table 71. MPC8548E Pinout Listing (continued)

#### Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA\_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA\_REQ2.

- 2. Recommend a weak pull-up resistor (2-10 kΩ) be placed on this pin to OV<sub>DD</sub>.
- 3. A valid clock must be provided at POR if TSEC4\_TXD[2] is set = 1.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- 10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V<sub>DD</sub>/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 14.Internal thermally sensitive resistor.
- 15.No connections must be made to these pins if they are not used.
- 16. These pins are not connected for any use.
- 17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV<sub>DD</sub> when using 64-bit buffer mode (pins PCI\_AD[63:32] and PCI1\_C\_BE[7:4]).
- 19.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 20. This pin is only an output in FIFO mode when used as Rx flow control.

24.Do not connect.

#### Package Description

## Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
25.These are test signals for factory u	ise only and must be pulled up (100 $\Omega$ –1 k $\Omega$ ) to (	DV <sub>DD</sub> for normal	machine opera	ation.	
26.Independent supplies derived from board V <sub>DD</sub> .					
27.Recommend a pull-up resistor (~1	$k\Omega$ ) be placed on this pin to OV <sub>DD</sub> .				
29. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], TSEC4_TXD3/TSEC3_TXD7, HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP.					
30. This pin requires an external 4.7-k driven.	2 pull-down resistor to prevent PHY from seeing a	valid transmit en	able before it is	actively	
31. This pin is only an output in eTSE	C3 FIFO mode when used as Rx flow control.				
32. These pins must be connected to 2	XV <sub>DD</sub> .				
33.TSEC2_TXD1, TSEC2_TX_ER an HRESET assertion.	e multiplexed as cfg_dram_type[0:1]. They must	be valid at powe	r-up, even befo	ore	
34. These pins must be pulled to group	nd through a 300- $\Omega$ (±10%) resistor.				
35.When a PCI block is disabled, eith down to select external arbiter if the connect' or terminated through 2–1 connected to any other PCI device. POR config pins—irrespective of w any other PCI device connected or	er the POR config pin that selects between interrere is any other PCI device connected on the PCI 0 k $\Omega$ pull-up resistors with the default of internal. The PCI block drives the PCI <i>n_</i> AD pins if it is context. The block drives the DEVDISR register or the bus.	hal and external a bus, or leave th arbiter if the PCI nfigured to be th not. It may caus	arbiter must be e PCI <i>n_</i> AD pin <i>n_</i> AD pins are e PCI arbiter— e contention if	e pulled is as 'no not through there is	
36.MDIC0 is grounded through an 18. 1% resistor. These pins are used for	2- $\Omega$ precision 1% resistor and MDIC1 is connected or automatic calibration of the DDR IOs.	ed to GV <sub>DD</sub> throu	gh an 18.2-Ω p	recision	
38. These pins must be left floating.					
39. If PCI1 or PCI2 is configured as P Otherwise the processor will not be	CI asynchronous mode, a valid clock must be pro oot up.	ovided on pin PC	I1_CLK or PCI	2_CLK.	
40.These pins must be connected to	GND.				
101.This pin requires an external 4.7-	kΩ resistor to GND.				
102.For Rev. 2.x silicon, DMA_DACK POR configuration are don't care.	[0:1] must be 0b11 during POR configuration; for	rev. 1.x silicon, t	he pin values o	during	
103.If these pins are not used as GPI $2-10 \text{ k}\Omega$ resistors.	Nn (general-purpose input), they must be pulled	low (to GND) or	high (to LV <sub>DD</sub> )	through	
104.These must be pulled low to GNE	D through 2–10 k $\Omega$ resistors if they are not used.				
105.These must be pulled low or high	to $\text{LV}_{\text{DD}}$ through 2–10 k $\Omega$ resistors if they are no	t used.			
106.For rev. 2.x silicon, DMA_DACK[0 configuration are don't care.	):1] must be 0b10 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR	
107.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	):1] must be 0b01 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR	
108.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	):1] must be 0b11 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR	
109. This is a test signal for factory us	e only and must be pulled down (100 $\Omega$ – 1 k $\Omega$ ) t	o GND for norma	al machine ope	eration.	
111. If these pins are not used as GPI	Nn (general-purpose input), they must be pulled I	ow (to GND) or h	nigh (to OV <sub>DD</sub> )	through	
2-10 K22 HESISIUIS.	during DOP configuration				
112. This pin must not be pulled down	$\alpha$ $\alpha$ $\beta$				
	$\int \int \nabla \nabla D = \int \nabla \nabla \nabla \nabla D = \int \nabla \nabla \nabla \nabla \nabla \nabla D = \int \nabla \nabla$				

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER	R10	0	LV <sub>DD</sub>	5, 9, 33
Three	e-Speed Ethernet Controller (Gigabit Eth	ernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	_
TSEC3_GTX_CLK	W8	0	TV <sub>DD</sub>	_
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	_
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	_
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	_
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	_
TSEC3_TX_EN	V9	0	TV <sub>DD</sub>	30
Three	e-Speed Ethernet Controller (Gigabit Eth	ernet 4)		
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV <sub>DD</sub>	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	1
TSEC4_GTX_CLK	AA5	0	TV <sub>DD</sub>	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV <sub>DD</sub>	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV <sub>DD</sub>	1, 30
· · ·	DUART			•
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	—
UART_RTS[0:1]	AC6, AD7	0	OV <sub>DD</sub>	—
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	—
UART_SOUT[0:1]	AB7, AD8	0	OV <sub>DD</sub>	_
· · ·	I <sup>2</sup> C Interface			•
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4, 27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4, 27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4, 27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4, 27
· · ·	SerDes			
SD_RX[0:3]	M28, N26, P28, R26	I	XV <sub>DD</sub>	—
SD_RX[0:3]	M27, N25, P27, R25	I	XV <sub>DD</sub>	—
SD_TX[0:3]	M22, N20, P22, R20	0	XV <sub>DD</sub>	—
SD_TX[0:3]	M23, N21, P23, R21	0	XV <sub>DD</sub>	<b>—</b>
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	_	40

## Table 72. MPC8547E Pinout Listing (continued)

Table 72.	MPC8547E	<b>Pinout Listing</b>	(continued)
		i mout Listing	(continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
DFT					
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25	
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25	
LSSD_MODE	AH20	I	OV <sub>DD</sub>	25	
TEST_SEL	AH14	I	OV <sub>DD</sub>	25	
	Thermal Management				
THERMO	AG1			14	
THERM1	AH1			14	
	Power Management				
ASLEEP	AH18	0	$OV_{DD}$	9, 19, 29	
	Power and Ground Signals				
GND	<ul> <li>A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17,</li> <li>F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27,</li> <li>L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13,</li> <li>U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27,</li> <li>K28, L24, L26, N24, N27, P25, R28, T24, T26,</li> <li>U24, V25, W28, Y24, Y26, AA24, AA27, AB25,</li> <li>AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27</li> </ul>	_	_	_	
OV <sub>DD</sub>	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV <sub>DD</sub>		
LV <sub>DD</sub>	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV <sub>DD</sub>		
TV <sub>DD</sub>	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV <sub>DD</sub>	_	
GV <sub>DD</sub>	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV <sub>DD</sub>		

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV <sub>DD</sub>	—
LSYNC_OUT	F28	0	BV <sub>DD</sub>	—
	DMA		I	
DMA_DACK[0:1]	AD3, AE1	0	OV <sub>DD</sub>	5, 9, 108
DMA_DREQ[0:1]	AD4, AE2	I	OV <sub>DD</sub>	—
DMA_DDONE[0:1]	AD2, AD1	0	OV <sub>DD</sub>	—
	Programmable Interrupt Controller		I	
UDE	AH16	I	OV <sub>DD</sub>	_
MCP	AG19	I	OV <sub>DD</sub>	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	Ι	OV <sub>DD</sub>	—
IRQ[8]	AF19	I	OV <sub>DD</sub>	—
IRQ[9]/DMA_DREQ3	AF21	I	OV <sub>DD</sub>	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV <sub>DD</sub>	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV <sub>DD</sub>	1
IRQ_OUT	AD18	0	OV <sub>DD</sub>	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV <sub>DD</sub>	5, 9
EC_MDIO	AC8	I/O	OV <sub>DD</sub>	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV <sub>DD</sub>	—
	Three-Speed Ethernet Controller (Gigabit Ether	rnet 1)		
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV <sub>DD</sub>	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV <sub>DD</sub>	5, 9
TSEC1_COL	R4	I	LV <sub>DD</sub>	—
TSEC1_CRS	V5	I/O	LV <sub>DD</sub>	20
TSEC1_GTX_CLK	U7	0	LV <sub>DD</sub>	—
TSEC1_RX_CLK	U3	I	LV <sub>DD</sub>	—
TSEC1_RX_DV	V2	I	LV <sub>DD</sub>	—
TSEC1_RX_ER	T1	I	LV <sub>DD</sub>	—
TSEC1_TX_CLK	Т6	I	LV <sub>DD</sub>	—
TSEC1_TX_EN	U9	0	LV <sub>DD</sub>	30
TSEC1_TX_ER	Τ7	0	LV <sub>DD</sub>	
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV <sub>DD</sub>	103