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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8545epxangd

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO™ interface unit
 - Supports *RapidIO™ Interconnect Specification, Revision 1.2*
 - Both 1× and 4× LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

- Single inbound doorbell message structure
- Facility to accept port-write messages
- PCI Express interface
 - PCI Express 1.0a compatible
 - Supports x8, x4, x2, and x1 link widths
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - 8 PCI Express
 - 4 PCI Express and 4 serial RapidIO
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1™

4.5 Platform to FIFO Restrictions

Note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency}/4.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 127 MHz.

For FIFO encoded mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency}/4.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 167 MHz.

4.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527 \text{ MHz} \times (\text{PCI-Express link width})}{8}$$

See *MPC8548ERM, Rev. 2, PowerQUICC III Integrated Processor Family Reference Manual*, Section 18.1.3.2, “Link Width,” for PCI Express interface width details.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

See *MPC8548ERM, Rev. 2, PowerQUICC III Integrated Processor Family Reference Manual*, Section 17.4, “1x/4x LP-Serial Signal Descriptions,” for serial RapidIO interface width and frequency details.

4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform see the specific section of this document.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that $GV_{DD}(\text{typ}) = 2.5 \text{ V}$ for DDR SDRAM, and $GV_{DD}(\text{typ}) = 1.8 \text{ V}$ for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 11. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280 \text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail must track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR2 I/O capacitance when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 12. DDR2 SDRAM Capacitance for $GV_{DD}(\text{typ})=1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, \overline{DQS}	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 22](#) and [Table 23](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 22. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	V_{DD} V_{DD}	3.13	3.47	V	1, 2
Output high voltage ($V_{DD}/V_{DD} = \min$, $I_{OH} = -4.0$ mA)	V_{OH}	2.40	$V_{DD}/V_{DD} + 0.3$	V	—
Output low voltage ($V_{DD}/V_{DD} = \min$, $I_{OL} = 4.0$ mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	$V_{DD}/V_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.90	V	—
Input high current ($V_{IN} = V_{DD}$, $V_{IN} = V_{DD}$)	I_{IH}	—	40	μ A	1, 2, 3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-600	—	μ A	—

Notes:

1. V_{DD} supports eTSECs 1 and 2.
2. V_{DD} supports eTSECs 3 and 4.
3. The symbol V_{IN} , in this case, represents the V_{IH} and V_{IL} symbols referenced in [Table 1](#) and [Table 2](#).

A summary of the FIFO AC specifications appears in [Table 24](#) and [Table 25](#).

Table 24. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDV}	0.5	—	—	ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See [Section 4.5, “Platform to FIFO Restrictions.”](#)

Timing diagrams for FIFO appear in [Figure 6](#) and [Figure 7](#).

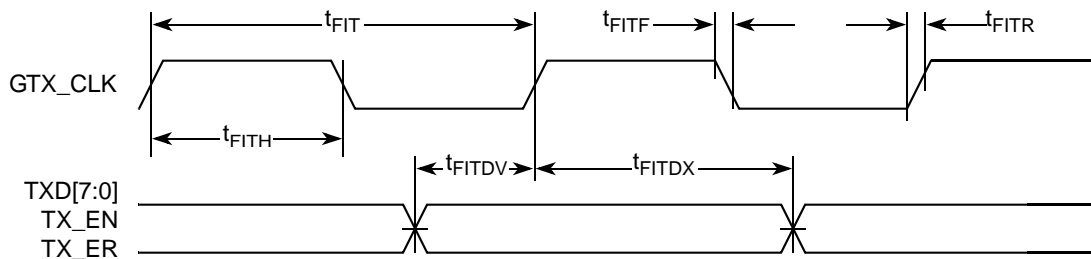


Figure 6. FIFO Transmit AC Timing Diagram

Figure 14 shows the TBI transmit AC timing diagram.

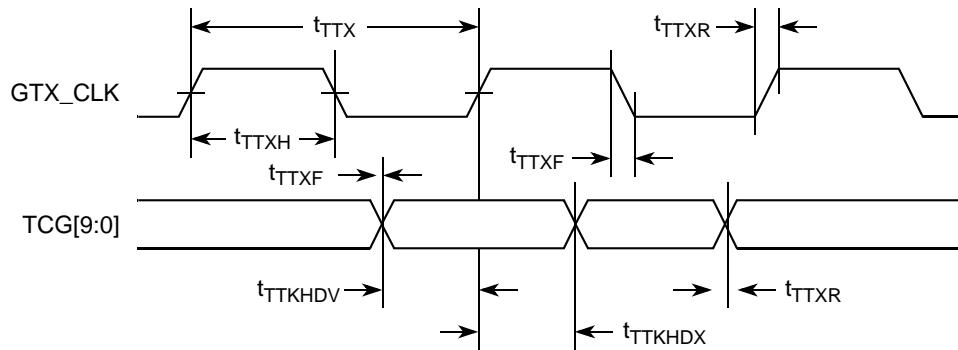


Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 31. TBI Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSEC _n _RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns
TSEC _n _RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
TSEC _n _RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSEC _n _RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC _n _RX_CLK	t_{TRDXKH}	1.5	—	—	ns
TSEC _n _RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}^2	0.7	—	2.4	ns
TSEC _n _RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}^2	0.7	—	2.4	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters ($BV_{DD} = 2.5$ V)—PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/UPWAIT$)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

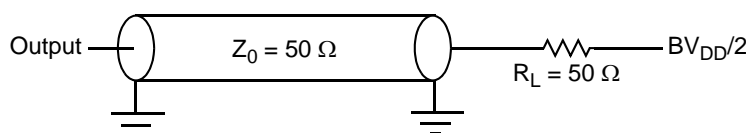


Figure 22. Local Bus AC Test Load

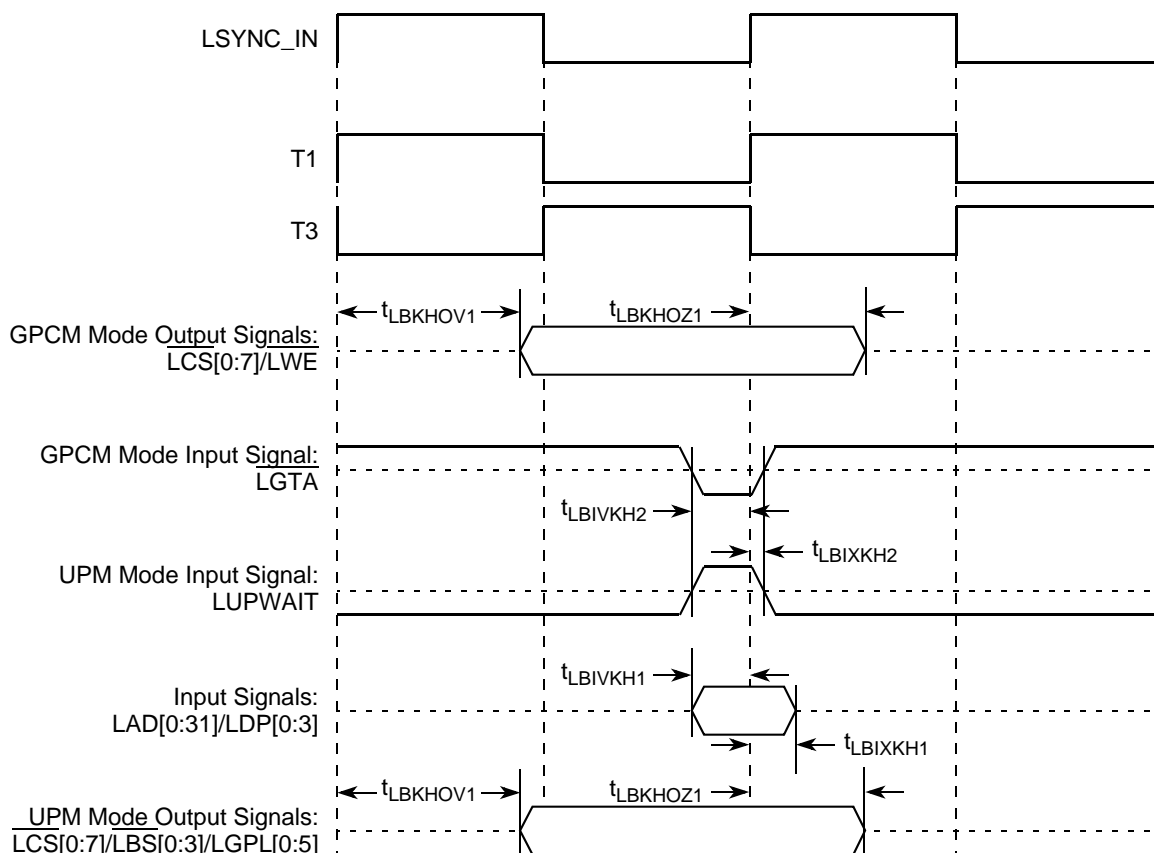


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

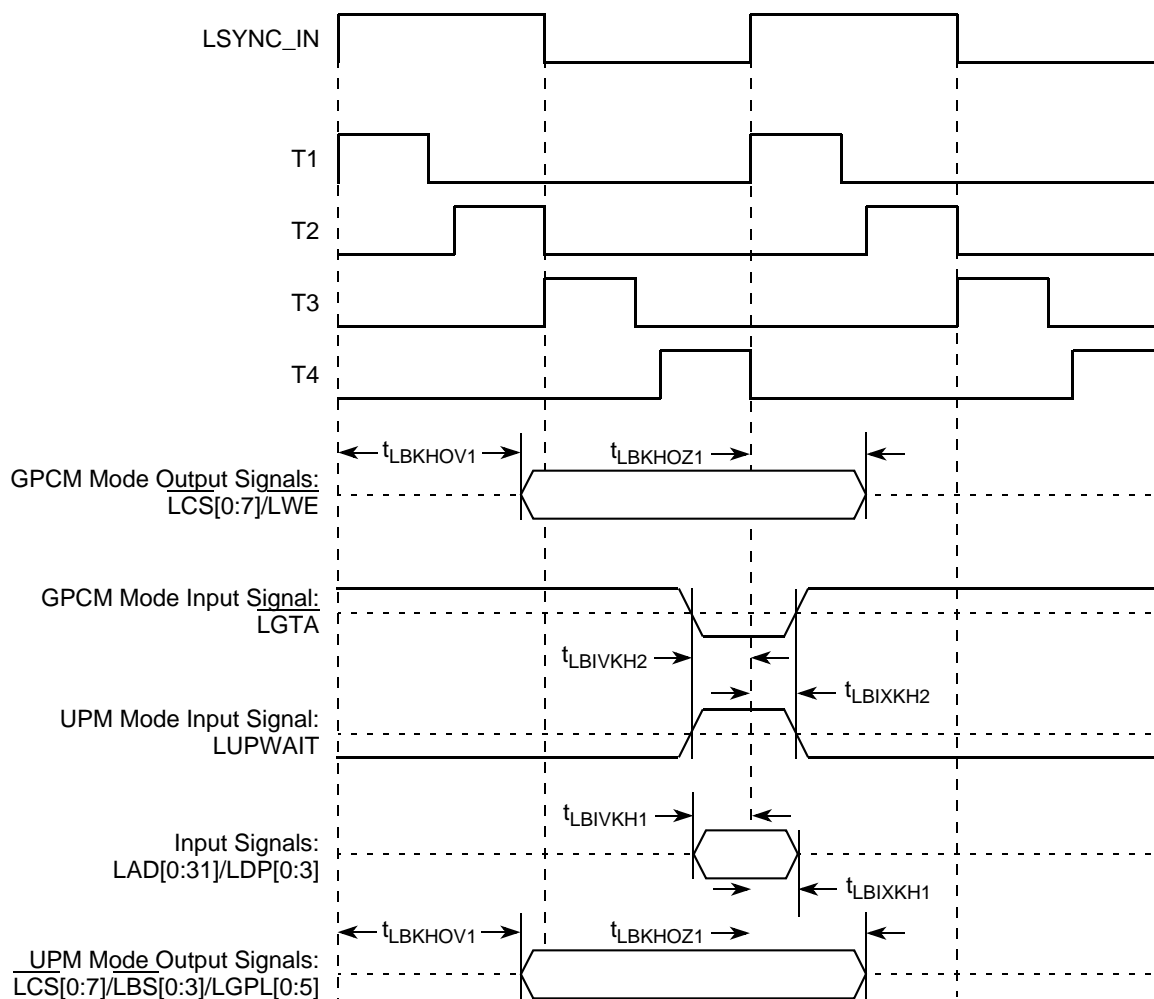


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

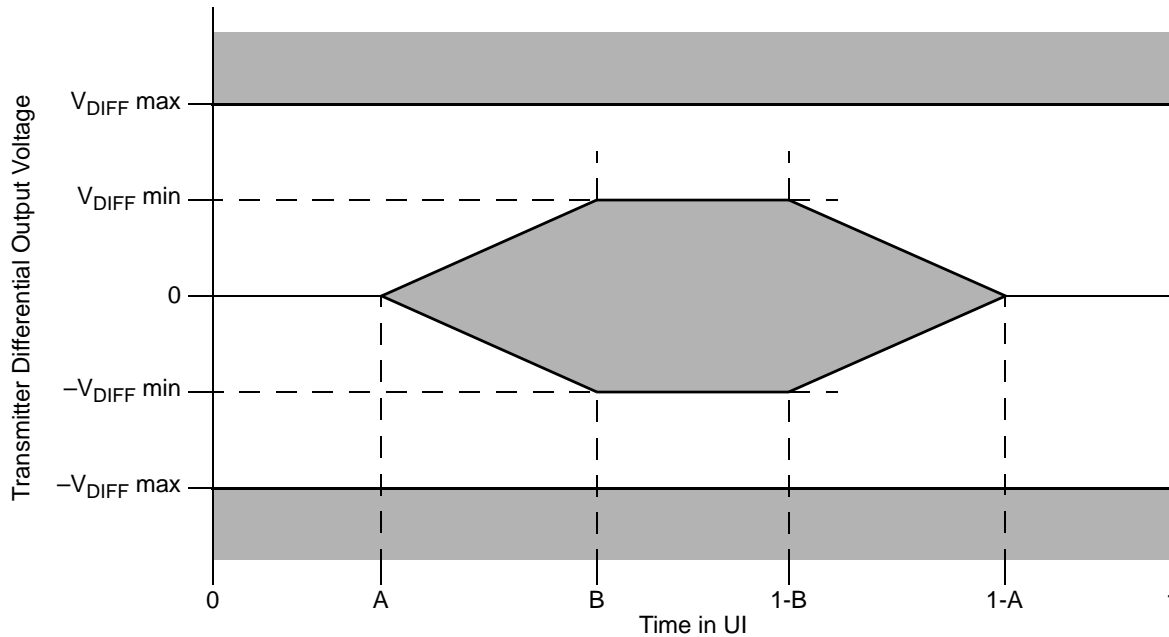


Figure 52. Transmitter Output Compliance Mask

Table 65. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times$ (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling

802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100- Ω resistive $\pm 5\%$ differential to 2.5 GHz.

18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive $\pm 5\%$ differential to 2.5 GHz.

18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in [Section 18.7, “Receiver Specifications,”](#) and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in [Figure 54](#) and [Table 69](#). Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in [Section 18.7, “Receiver Specifications,”](#) is then added to the signal and the test load is replaced by the receiver being tested.

19.3 Pinout Listings

NOTE

The $\overline{\text{DMA_DACK}}[0:1]$ and $\overline{\text{TEST_SEL}}/\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on $\text{PCI1_AD}[63:32]/\text{PC2_AD}[31:0]$ pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

Table 71. MPC8548E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
$\text{PCI1_AD}[63:32]/\text{PCI2_AD}[31:0]$	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
$\text{PCI1_AD}[31:0]$	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[7:4]/\text{PCI2_C_}\overline{\text{BE}}[3:0]$	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[3:0]$	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
$\text{PCI1_PAR64}/\text{PCI2_PAR}$	W15	I/O	OV_{DD}	
$\overline{\text{PCI1_GNT}}[4:1]$	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1_TRDY}}$	AG11	I/O	OV_{DD}	2

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
I²C interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	—
$\overline{\text{SD_RX}}[0:7]$	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV _{DD}	—
$\overline{\text{SD_TX}}[0:7]$	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV _{DD}	—
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	3
$\overline{\text{SD_REF_CLK}}$	T27	I	XV _{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV _{DD}	—
$\overline{\text{HRESET_REQ}}$	AG16	O	OV _{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV _{DD}	—
$\overline{\text{CKSTP_IN}}$	AA9	I	OV _{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD} .
3. A valid clock must be provided at POR if $\text{TSEC4_TXD}[2]$ is set = 1.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of $\text{LA}[28:31]$ during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See [Section 20.2, “CCB/SYSCLK PLL Ratio.”](#)
8. The value of LALE , LGPL2 , and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the [Section 20.3, “e500 Core PLL Ratio.”](#)
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the $\text{V}_{\text{DD}}/\text{GND}$ planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections must be made to these pins if they are not used.
16. These pins are not connected for any use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins $\text{PCI_AD}[63:32]$ and $\text{PCI1_C_BE}[7:4]$).
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx flow control.
24. Do not connect.

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
DMA_DACK[0:1]	AD3, AE1	O	OV _{DD}	5, 9, 108
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	O	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	O	LV _{DD}	30
TSEC1_TX_ER	T7	O	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV _{DD}	5, 9
GPOUT7	N6	O	LV _{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV _{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV _{DD}	15
cfg_dram_type1	R10	O	LV _{DD}	5, 9
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	—
TSEC3_GTX_CLK	W8	O	TV _{DD}	—
TSEC3_RX_CLK	W2	I	TV _{DD}	—
TSEC3_RX_DV	W1	I	TV _{DD}	—
TSEC3_RX_ER	Y2	I	TV _{DD}	—
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	O	TV _{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV _{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV _{DD}	—
TSEC3_CRS	AA3	I/O	TV _{DD}	31
TSEC3_TX_ER	AB6	O	TV _{DD}	—
DUART				
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	O	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV _{DD}	—
I²C interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27

Table 77. Processor Core Clocking Specifications (MPC8543E)

Characteristic	Maximum Processor Core Frequency				Unit	Notes
	800 MHz		1000 MHz			
	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, “CCB/SYSCCLK PLL Ratio,”](#) and [Section 20.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 78. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1200, 1333 MHz			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, “CCB/SYSCCLK PLL Ratio,”](#) and [Section 20.3, “e500 Core PLL Ratio,”](#) for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

Table 79. Memory Bus Clocking Specifications (MPC8545E)

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1200 MHz			
	Min	Max		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, “CCB/SYSCCLK PLL Ratio,”](#) and [Section 20.3, “e500 Core PLL Ratio,”](#) for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

COP_TDO	1	2	NC
COP_TDI	3	4	$\overline{\text{COP_TRST}}$
COP_RUN/STOP	5	6	COP_VDD_SENSE
COP_TCK	7	8	$\overline{\text{COP_CHKSTP_IN}}$
COP_TMS	9	10	NC
$\overline{\text{COP_SRESET}}$	11	12	NC
$\overline{\text{COP_HRESET}}$	13	KEY No pin	
$\overline{\text{COP_CHKSTP_OUT}}$	15	16	GND

Figure 62. COP Connector Physical Pinout

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	<ul style="list-style-type: none"> Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. Removed Note from Section 5.1, "Power-On Ramp Rate". Changed the Table 10 title to "Power Supply Ramp Rate". Removed table 11. Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)"¹ from 4 and 25 to 2 and 10 respectively .
8	04/2011	<ul style="list-style-type: none"> Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	<ul style="list-style-type: none"> In Table 37, "MII Management AC Timing Specifications," modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	<ul style="list-style-type: none"> In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. In Table 13 deleted ramp rate requirement for XVDD/SVDD. In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	<ul style="list-style-type: none"> In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." Added a reference to Revision 2.1.2. Updated Table 55, "MII Management AC Timing Specifications." Added Section 5.1, "Power-On Ramp Rate."