E·XFL



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
PowerPC e500
1 Core, 32-Bit
800MHz
Signal Processing; SPE, Security; SEC
DDR, DDR2, SDRAM
No
-
10/100/1000Mbps (4)
-
-
1.8V, 2.5V, 3.3V
0°C ~ 105°C (TA)
Cryptography, Random Number Generator
783-BBGA, FCBGA
783-FCBGA (29x29)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8545evuanj

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

Power Characteristics

Power Characteristics 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Table 4. Device Power Dissipation

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on V_{DD} = 1.1 V, T_i = 65°C.

3. Typical-65 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 65^{\circ}\text{C}$, running Dhrystone. 4. Typical-105 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running Dhrystone. 5. Maximum is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running a smoke test.

Table 13 provides the recommended operating conditions for the DDR SDRAM controller when $GV_{DD}(typ) = 2.5 \text{ V}.$

Parameter/Condition	Symbol Min		Max	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.15	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.15	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35 V$)	I _{OL}	16.2	—	mA	—

Table 13	DDR SDRAM	DC Electrical	Characteristics	for GV	(tvn) = 2	25 V
Table 15.	DDIX SDIXAM		Gilaracteristics		(()) – 4	1.J V

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm V}_{\rm DD}$ at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 14 provides the DDR I/O capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 14. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μ A current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	^t ciskew	-300 -365 -390	300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ± (T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

Ethernet Management Interface Electrical Characteristics

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum f_{MDC} = f_{CCB} ÷ 64 and minimum f_{MDC} = f_{CCB} ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

Parameter		Symbol ²	Min	Мах	Unit	Notes
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	4 2	20 10	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	30 30		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO		t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

 Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.



Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.



Figure 30. JTAG Clock Input Timing Diagram



Figure 34 shows the AC timing diagram for the I^2C bus.



Figure 34. I²C Bus AC Timing Diagram

PCI/PCI-X

Table 54. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the PCI-X 1.0a Specification.

- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the PCI-X 1.0a Specification.

- 10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
- 11. Guaranteed by characterization.

12. Guaranteed by design.

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

PCI Express

Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{RX-CM-ACp}	AC peak common mode input voltage	_	_	150	mV	$\begin{split} & V_{RX\text{-}CM\text{-}ACp} = V_{RXD\text{+}} - V_{RXD\text{-}} /2 + V_{RX\text{-}CM\text{-}DC} \\ & V_{RX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } V_{RX\text{-}D\text{+}} + V_{RX\text{-}D\text{-}} \div 2. \\ & See Note 2. \end{split}$
RL _{RX-DIFF}	Differential return loss	15	—	_	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4.
RL _{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
Z _{RX-DIFF-DC}	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z _{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 \pm 20% tolerance). See Notes 2 and 5.
Z _{RX-HIGH-IMP-DC}	Powered down DC input impedance	200 k	—	_	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
V _{RX-IDLE-DET-DIFFp-p}	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFF_{p-p}} = 2 \times V_{RX-D+} - V_{RX-D-} .$ Measured at the package pins of the receiver
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Characteristic	Symbol	Range		Unit	Notos
Characteristic	Symbol	Min	Max	Onic	NULES
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	_	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10 ⁻¹²		—
Unit interval	UI	320	320	ps	±100 ppm

Table 68	. Receiver	AC	Timing	Specifications-	-3.125	GBaud
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Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Figure 53. Single Frequency Sinusoidal Jitter Limits

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	l	OV _{DD}	—
				_
				_
				_
				_
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV _{DD}	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV _{DD}	2
PCI2_CLK	AE28	I	OV _{DD}	39
PCI2_IRDY	AD26	I/O	OV _{DD}	2
PCI2_PERR	AD25	I/O	OV _{DD}	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	0	OV _{DD}	5, 9, 35
PCI2_GNT0	AG25	I/O	OV _{DD}	_
PCI2_SERR	AD24	I/O	OV _{DD}	2, 4
PCI2_STOP	AF24	I/O	OV _{DD}	2
PCI2_TRDY	AD27	I/O	OV _{DD}	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV _{DD}	—
PCI2_REQ0	AH25	I/O	OV _{DD}	—
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	_
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	_
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV _{DD}	
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	_
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	_
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV _{DD}	
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV _{DD}	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Powerfor CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26
SENSEVDD	M14	0	V _{DD}	13

Table 71. MPC8548E Pinout Listing (continued)

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_	_	2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	—
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	_
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Table 72	. MPC8547E	Pinout	Listing ((continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
	Local Bus Controller Interface		I	
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	_
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	0	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	—
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1
LCS6/DMA_DACK2	G20	0	BV _{DD}	1
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9
LALE	H24	0	BV _{DD}	5, 8, 9
LBCTL	G27	0	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—
LGPL5	E26	0	BV _{DD}	5, 9
LCKE	E24	0	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	0	BV _{DD}	_
	DMA		l	1
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 107
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	
	Programmable Interrupt Controller			
UDE	AH16	I	OV _{DD}	_
MCP	AG19	I	OV _{DD}	—

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
	Local Bus Controller Interface			
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	_
LA[27]	H21	0	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	—
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1
LCS6/DMA_DACK2	G20	0	BV _{DD}	1
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9
LALE	H24	0	BV _{DD}	5, 8, 9
LBCTL	G27	0	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—
LGPL5	E26	0	BV _{DD}	5, 9
LCKE	E24	0	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	0	BV _{DD}	—
	DMA		I	
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 106
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	-
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	-
	Programmable Interrupt Controller			

21 Thermal

This section describes the thermal specifications of the device.

21.1 Thermal for Version 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

This table shows the package thermal characteristics.

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	17	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	12	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	11	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	8	°C/W	1, 2
Die junction-to-board	N/A	$R_{ hetaJB}$	3	°C/W	3
Die junction-to-case	N/A	$R_{ extsf{ heta}JC}$	0.8	°C/W	4

Table 84. Package Thermal Characteristics for HiCTE FC-CBGA

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.2 Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid

This section describes the thermal specifications for the FC-PBGA package for revision 2.1.1, 2.1.2, and 3.0 silicon.

This table shows the package thermal characteristics.

Table 85. Package	Thermal	Characteristics	for FC-PBGA
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Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	18	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	9	°C/W	1, 2

System Design Information

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD}}_{\text{TX}}[7:0]$
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- <u>SD_RX</u>[7:0]
- SD_REF_CLK
- SD_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = $0xE_0F08$) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- <u>SD_TX</u>[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD}_{RX}}[7:0]$
- SD_REF_CLK

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Japan:

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Asia/Pacific:

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