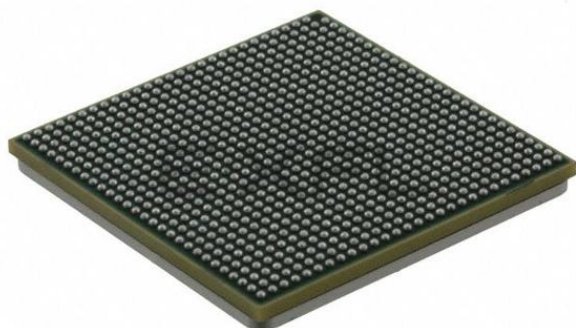




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8545hxaqg

- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

- VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
 - PCI 2.2 and PCI-X 1.0 compatible
 - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
 - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
 - Host and agent mode support
 - 64-bit dual address cycle (DAC) support
 - PCI-X supports multiple split transactions
 - Supports PCI-to-memory and memory-to-PCI streaming

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND -0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	10	μA	1, 2, 3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-15	—	μA	3

Notes:

1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#) and [Table 2](#).

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSECn's $TSECn_TX_CLK$, while the receive clock must be applied to pin $TSECn_RX_CLK$. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the $TSECn_GTX_CLK$ pin (while transmit data appears on $TSECn_TXD[7:0]$, for example). It is intended that external receivers capture eTSEC transmit data using the clock on $TSECn_GTX_CLK$ as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see [Section 4.5, "Platform to FIFO Restrictions."](#)

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters ($BV_{DD} = 2.5$ V)—PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/UPWAIT$)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

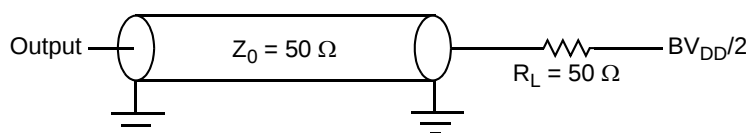


Figure 22. Local Bus AC Test Load

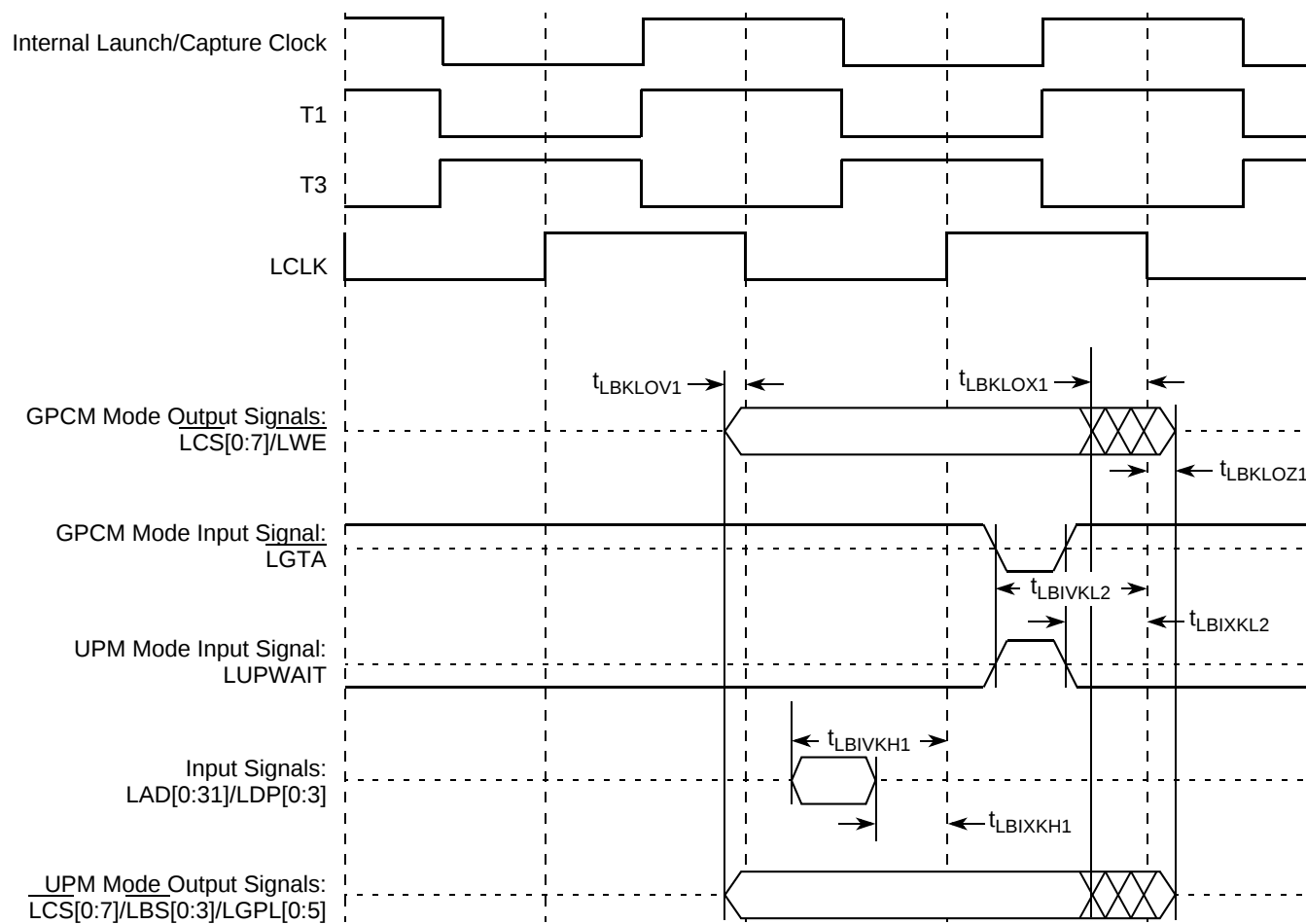


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

14 GP_{OUT}/GP_{IN}

This section describes the DC and AC electrical specifications for the GP_{OUT}/GP_{IN} bus of the device.

14.1 GP_{OUT}/GP_{IN} Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP_{OUT} interface.

Table 47. GP_{OUT} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level output voltage (BV _{DD} = min, I _{OH} = –2 mA)	V _{OH}	BV _{DD} – 0.2	—	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.2	V

Table 48. GP_{OUT} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level output voltage (BV _{DD} = min, I _{OH} = –1 mA)	V _{OH}	2.0	BV _{DD} + 0.3	V
Low-level output voltage (BV _{DD} min, I _{OL} = 1 mA)	V _{OL}	GND – 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP_{IN} interface.

Table 49. GP_{IN} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	–0.3	0.8	V
Input current (BV _{IN} ¹ = 0 V or BV _{IN} = BV _{DD})	I _{IN}	—	±5	μA

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current (BV _{IN} ¹ = 0 V or BV _{IN} = BV _{DD})	I _{IH}	—	10	μA

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in [Table 1](#).

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current (V _{IN} = 0 V or V _{IN} = V _{DD})	I _{IN}	—	±5	μA	2
High-level output voltage (OV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	2.4	—	V	—
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCIn_CLK when it is configured for asynchronous mode.

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

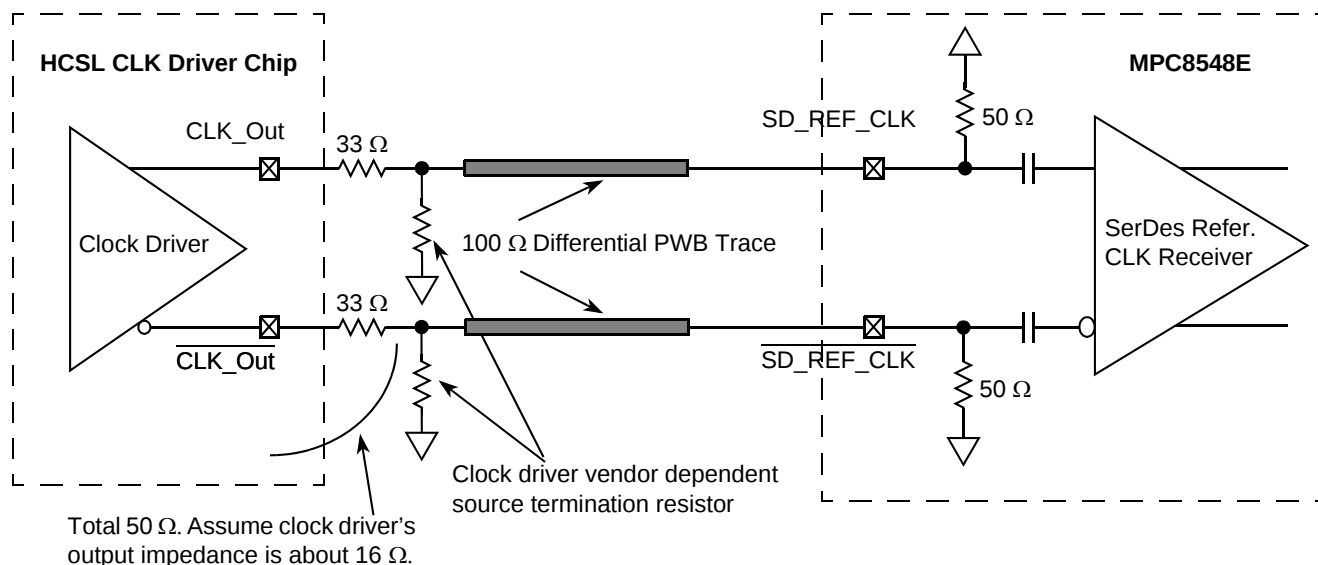


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

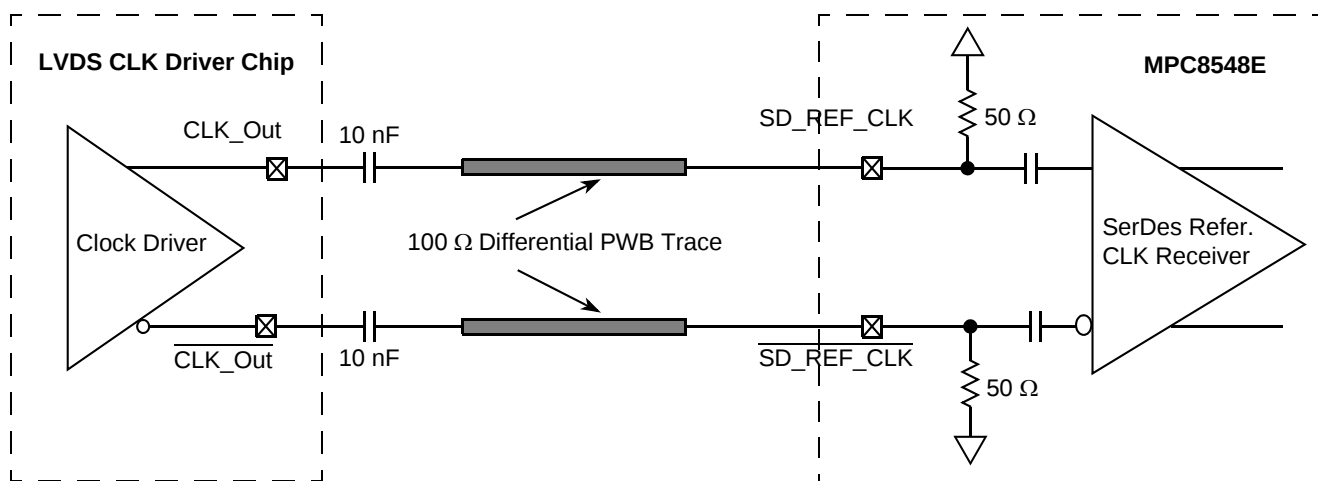


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires $R2 = 25 \Omega$. Consult a clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

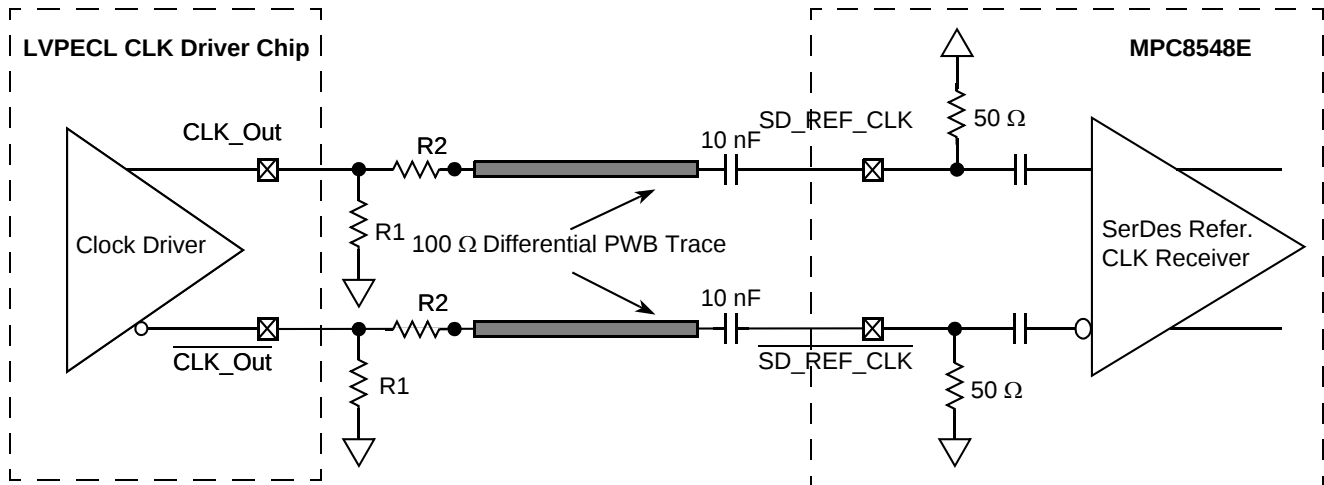


Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the SerDes reference clock input's DC requirement.

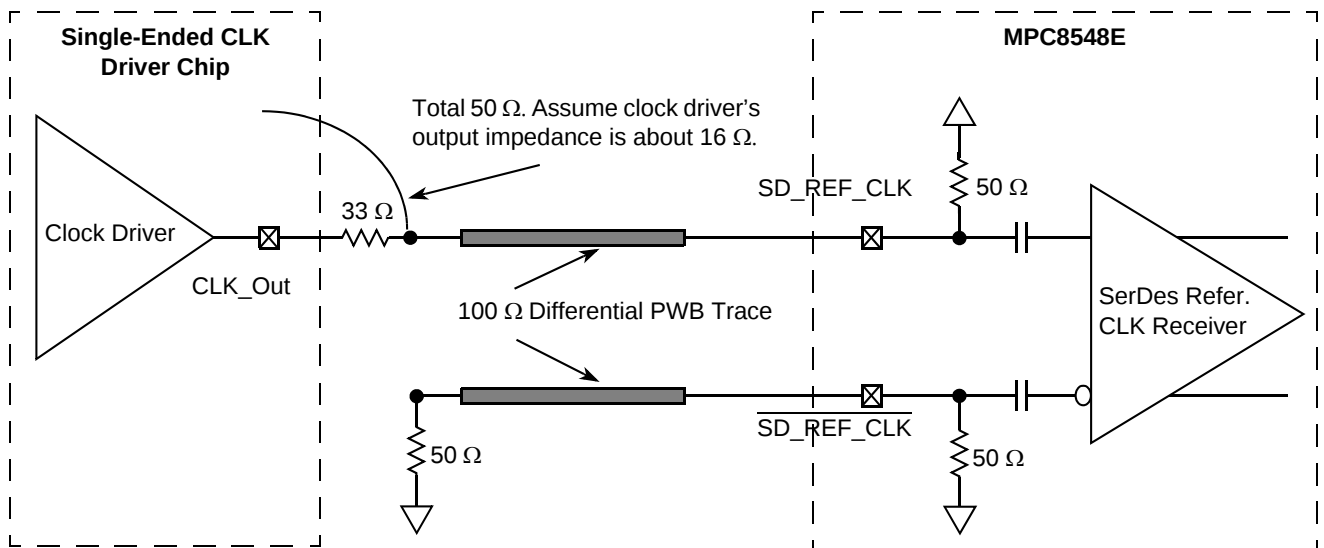


Figure 46. Single-Ended Connection (Reference Only)

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see [Section 16.2, “SerDes Reference Clocks.”](#)

17.2 AC Requirements for PCI Express SerDes Clocks

[Table 55](#) lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

Note:

1. Typical based on *PCI Express Specification 2.0*.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification, Rev. 1.0a*.

17.4.1 Differential Transmitter (TX) Output

[Table 56](#) defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{\text{crosslink}}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 50](#) and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in [Figure 48](#).)
3. A $T_{\text{TX-EYE}} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{\text{TX-JITTER-MAX}} = 0.30$ UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see [Figure 50](#)). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in [Figure 50](#) for both $V_{\text{TX-D+}}$ and $V_{\text{TX-D-}}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications Rev 1.0a*.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications Rev 1.0a*.
8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in [Figure 48](#) is specified using the passive compliance/test measurement load (see [Figure 50](#)) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

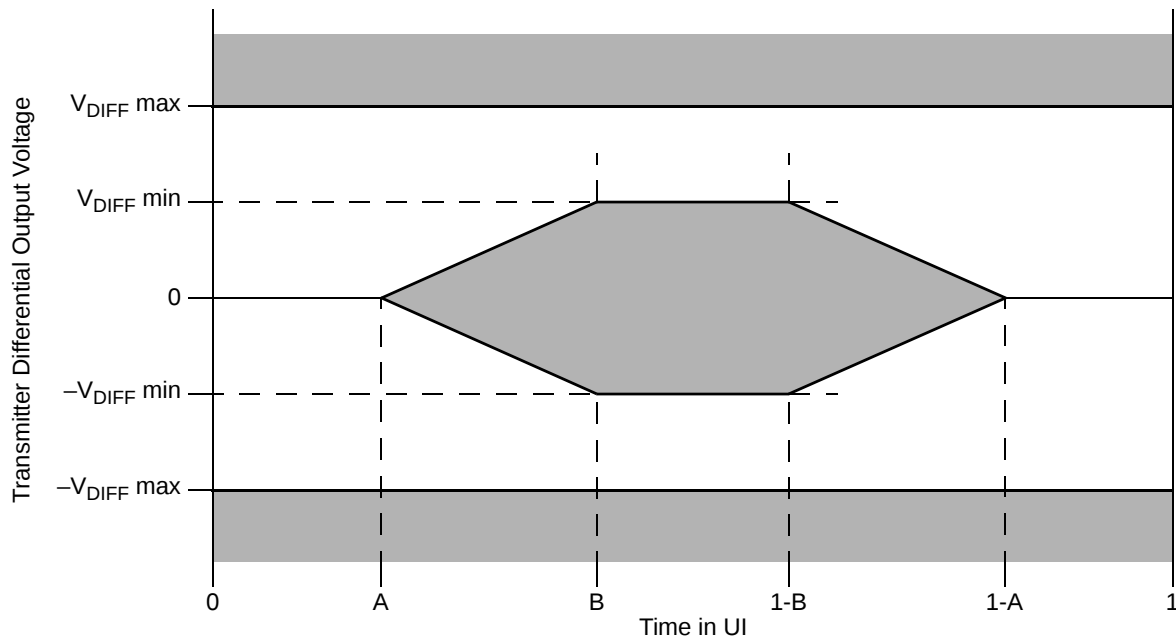


Figure 52. Transmitter Output Compliance Mask

Table 65. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times$ (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling

18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\text{-}\Omega \pm 5\%$ differential resistive load.

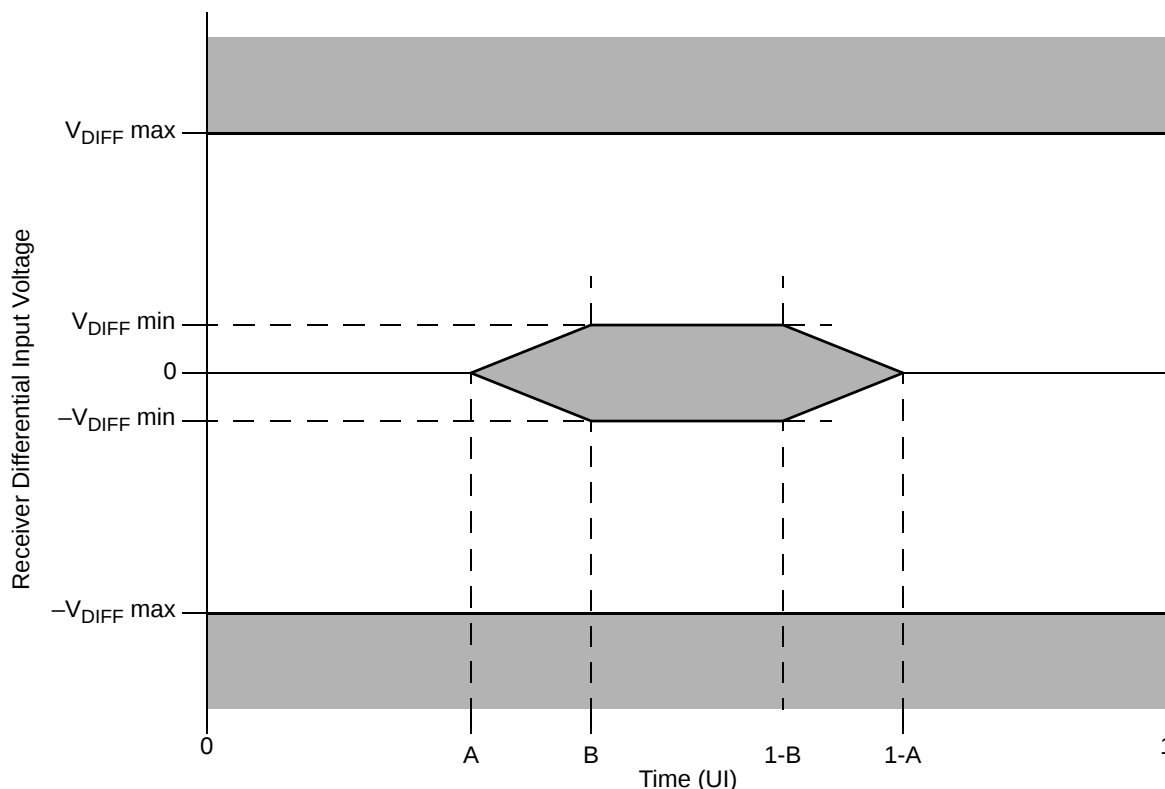


Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

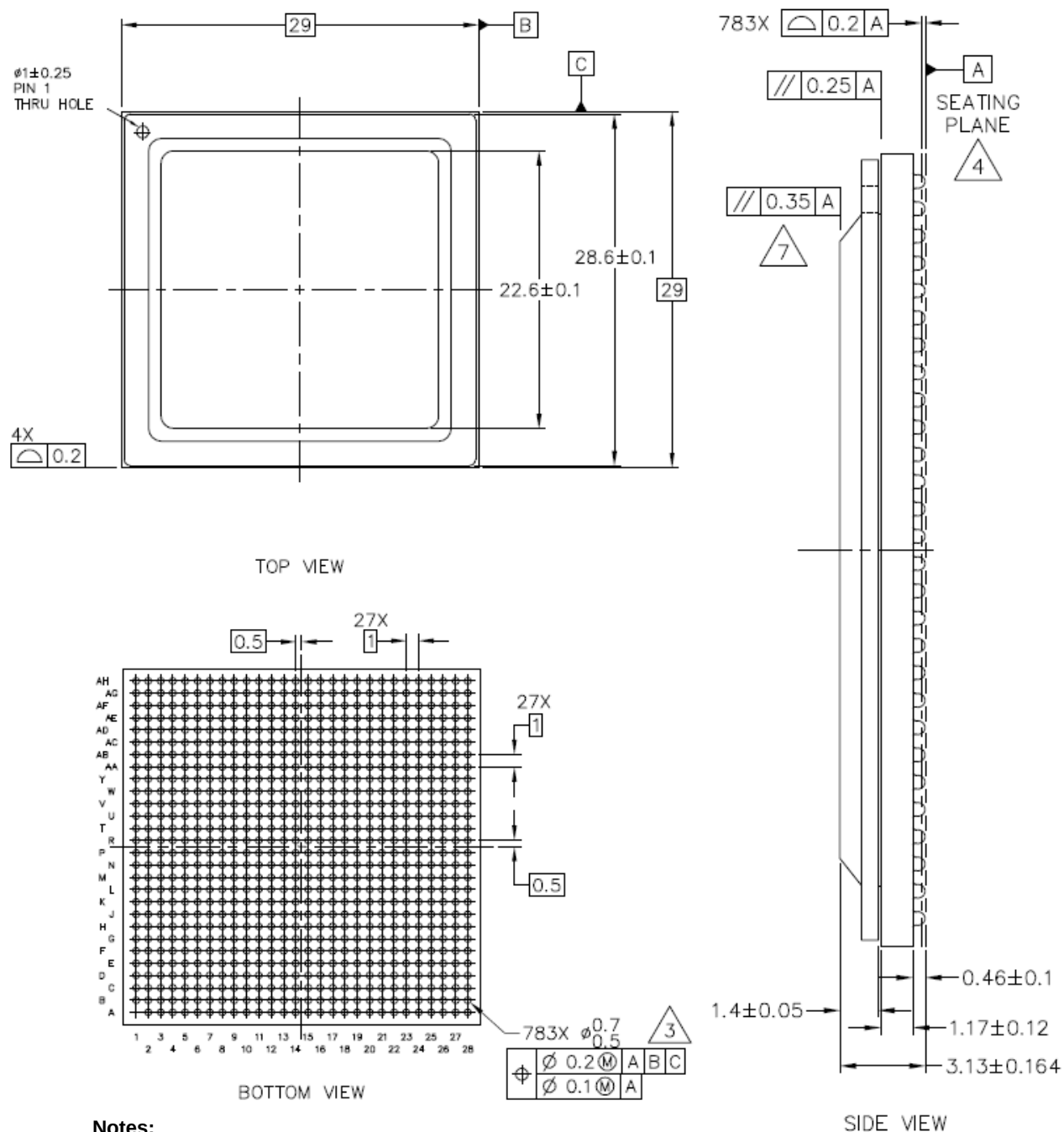
Receiver Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. Parallelism measurement shall exclude any effect of mark on top surface of package.
8. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Figure 56. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	O	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV _{DD}	5, 7, 9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV _{DD}	—
$\overline{\text{LCS5/DMA_DREQ2}}$	D23	I/O	BV _{DD}	1
$\overline{\text{LCS6/DMA_DACK2}}$	G20	O	BV _{DD}	1
$\overline{\text{LCS7/DMA_DDONE2}}$	E21	O	BV _{DD}	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV _{DD}	5, 9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV _{DD}	5, 9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV _{DD}	5, 9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV _{DD}	5, 9
LALE	H24	O	BV _{DD}	5, 8, 9
LBCTL	G27	O	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV _{DD}	5, 9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV _{DD}	5, 9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV _{DD}	5, 8, 9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV _{DD}	5, 9
LGPL4/ $\overline{\text{LGTA/LUPWAIT/LPBSE}}$	H23	I/O	BV _{DD}	—
LGPL5	E26	O	BV _{DD}	5, 9
LCKE	E24	O	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
$\overline{\text{DMA_DACK}}[0:1]$	AD3, AE1	O	OV _{DD}	5, 9, 106
$\overline{\text{DMA_DREQ}}[0:1]$	AD4, AE2	I	OV _{DD}	—
$\overline{\text{DMA_DDONE}}[0:1]$	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	AF28	O	OV _{DD}	—
TMS	AH27	I	OV _{DD}	12
TRST	AH23	I	OV _{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV _{DD}	25
L2_TSTCLK	AE22	I	OV _{DD}	25
LSSD_MODE	AH20	I	OV _{DD}	25
TEST_SEL	AH14	I	OV _{DD}	25
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV _{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	—
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2.5 V, 3.3 V)	TV _{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
DMA_DACK[0:1]	AD3, AE1	O	OV _{DD}	5, 9, 108
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	O	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	O	LV _{DD}	30
TSEC1_TX_ER	T7	O	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103

20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1000 MHz		1200 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSClk ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSClk frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, “CCB/SYSClk PLL Ratio,”](#) and [Section 20.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 76. Processor Core Clocking Specifications (MPC8545E)

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSClk ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSClk frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, “CCB/SYSClk PLL Ratio,”](#) and [Section 20.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

- First, the board must have at least 10×10 -nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1- μ F ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 63](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: $TSEC3_TXD[3]$, $\overline{HRESET_REQ}$, $TRIG_OUT/READY/QUIESCE$, $MSRCID[2:4]$, $ASLEEP$. The $\overline{DMA_DACK}[0:1]$, and $TEST_SEL/TEST_SEL$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 61](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.