Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8545pxatgd

- – VRRP and HSRP support for seamless router fail-over
- – Up to 16 exact-match MAC addresses supported
- – Broadcast address (accept/reject)
- – Hash table match on up to 512 multicast addresses
- – Promiscuous mode
- — Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- — RMON statistics support
- — 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- — MII management interface for control and status
- — Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
  - — Full crossbar packet switch
  - — Reorders packets from a source based on priorities
  - — Reorders packets to bypass blocked packets
  - — Implements starvation avoidance algorithms
  - — Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - — Four-channel controller
  - — All channels accessible by both the local and remote masters
  - — Extended DMA functions (advanced chaining and striding capability)
  - — Support for scatter and gather transfers
  - — Misaligned transfer capability
  - — Interrupt on completed segment, link, list, and error
  - — Supports transfers to or from any local memory or I/O port
  - — Selectable hardware-enforced coherency (snoop/no snoop)
  - — Ability to start and flow control each DMA channel from external 3-pin interface
  - — Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  - — PCI 2.2 and PCI-X 1.0 compatible
  - — One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  - — One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  - — Host and agent mode support
  - — 64-bit dual address cycle (DAC) support
  - — PCI-X supports multiple split transactions
  - — Supports PCI-to-memory and memory-to-PCI streaming

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- — Single inbound doorbell message structure
- — Facility to accept port-write messages
- PCI Express interface
  - — PCI Express 1.0a compatible
  - — Supports x8,x4,x2, and x1 link widths
  - — Auto-detection of number of connected lanes
  - — Selectable operation as root complex or endpoint
  - — Both 32- and 64-bit addressing
  - — 256-byte maximum payload size
  - — Virtual channel 0 only
  - — Traffic class 0 only
  - — Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
  - — 8 PCI Express
  - — 4 PCI Express and 4 serial RapidIO
- Power management
  - — Supports power saving modes: doze, nap, and sleep
  - — Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - — Supports eight 32-bit counters that count the occurrence of selected events
  - — Ability to count up to 512 counter-specific events
  - — Supports 64 reference events that can be counted on any of the eight counters
  - — Supports duration and quantity threshold counting
  - — Burstiness feature that permits counting of burst events with a programmable time between bursts
  - — Triggering and chaining capability
  - — Ability to generate an interrupt on overflow
- System access port
  - — Uses JTAG interface and a TAP controller to access entire system memory map
  - — Supports 32-bit accesses to configuration registers
  - — Supports cache-line burst accesses to main memory
  - — Supports large block (4-Kbyte) uploads and downloads
  - — Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1™

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NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	μs
Local bus PLL lock time	—	50	μs
PCI/PCI-X bus PLL lock time	—	50	μs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.

2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, "PLL Power Supply Filtering," the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

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6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8$ V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5$ V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	t_{CISKEW}	 −300 −365 −390	 300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

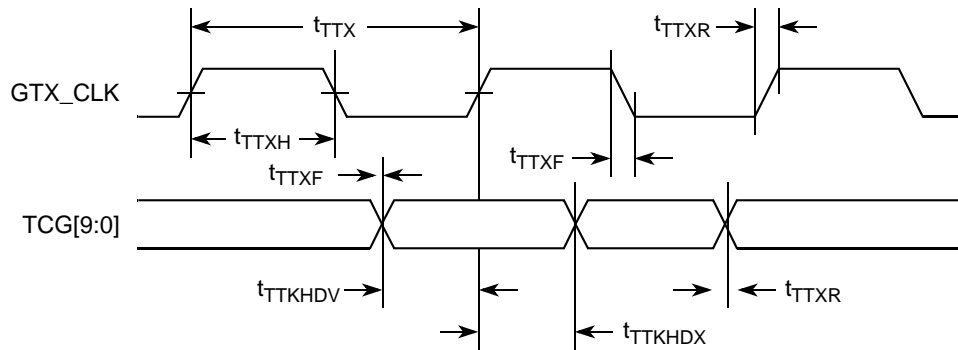Figure 14 shows the TBI transmit AC timing diagram.

Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2   TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 31. TBI Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TSECn_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns
TSECn_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSECn_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSECn_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
TSECn_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}[2]	0.7	—	2.4	ns
TSECn_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
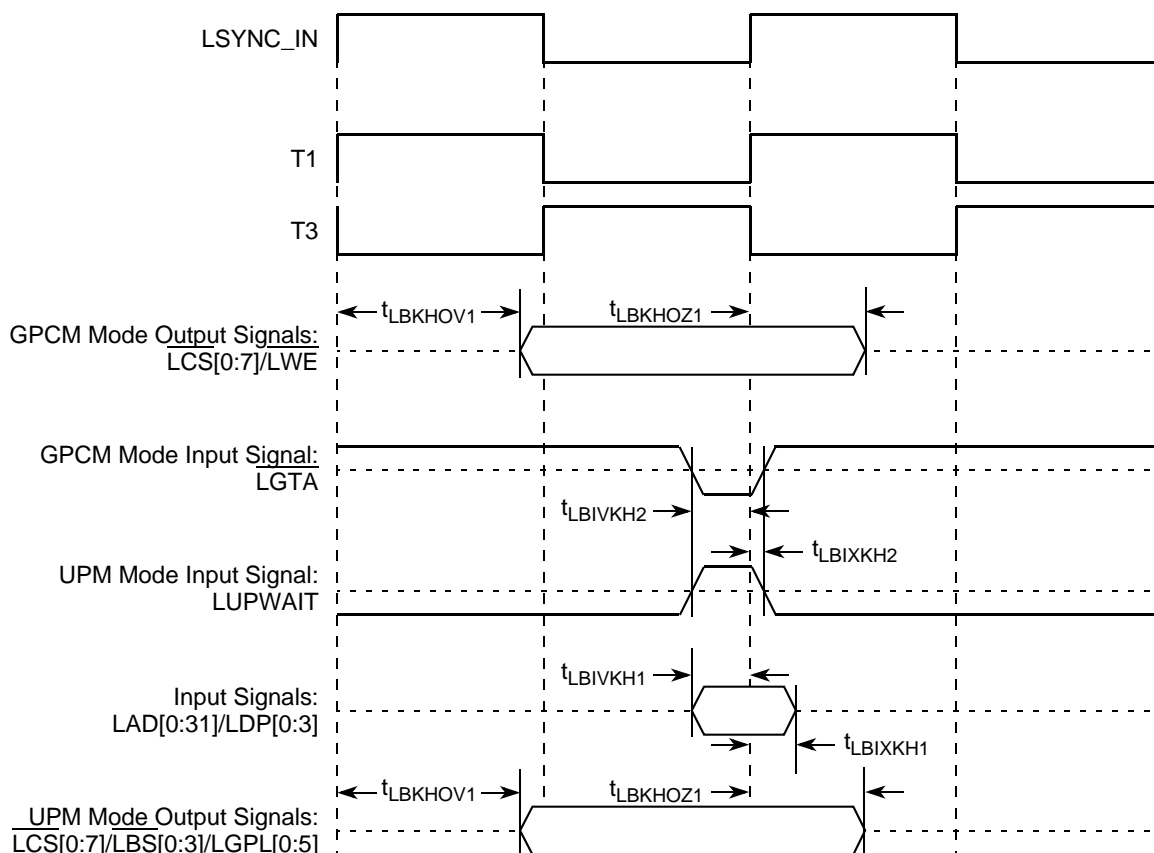
2. Guaranteed by design.

Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)
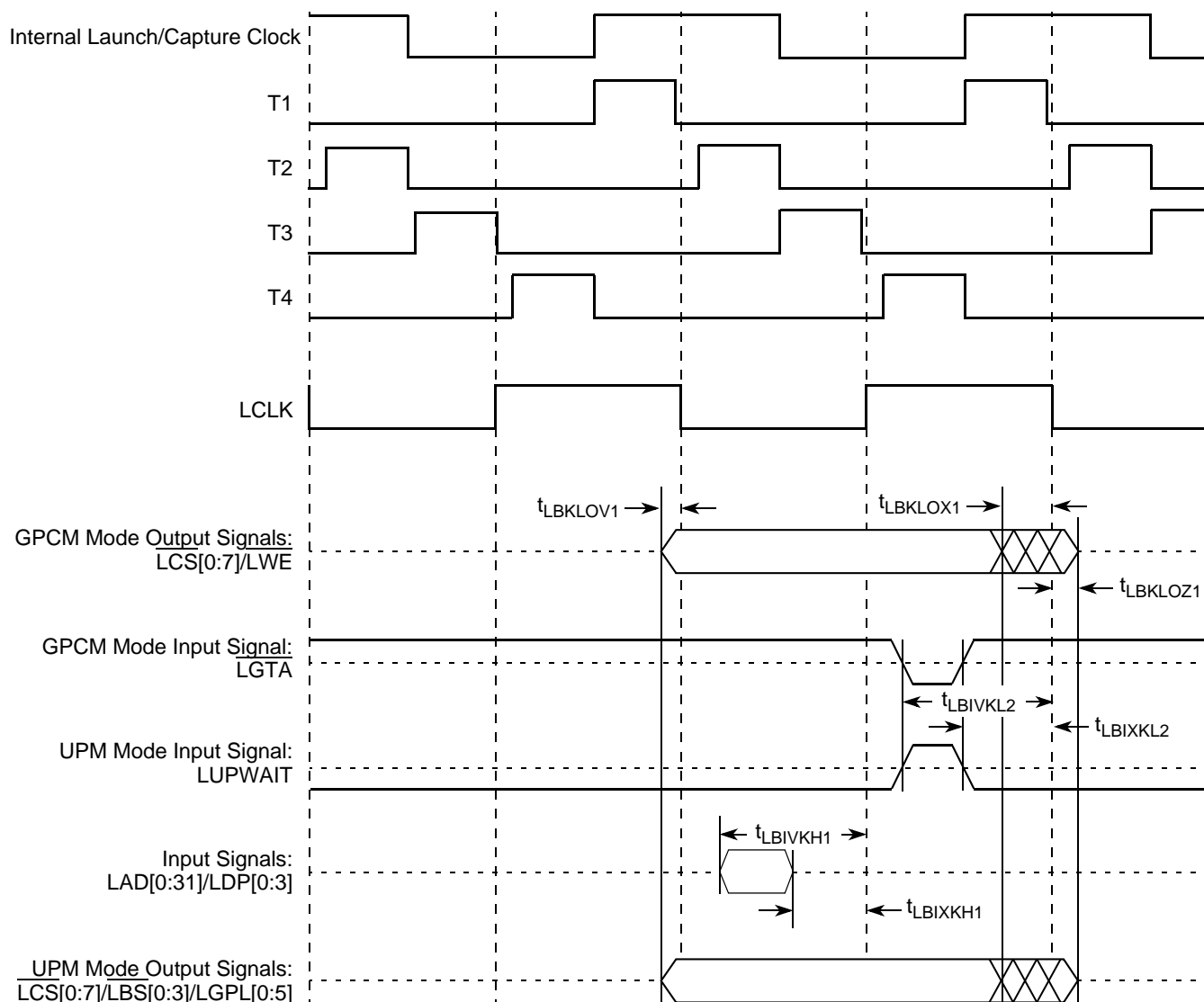
Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol[1]	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current (V_{IN}^{1} = 0 V or $V_{IN} = V_{DD}$)	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = −2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

12.2 JTAG AC Electrical Specifications

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 32.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

Note:
1. Typical based on *PCI Express Specification 2.0.*

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

18   Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8548E, for the LP-Serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

18.1   DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

18.2   AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

Table 58 lists the Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC requirements.

Table 58. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	−40	—	40	ps	—

Table 68. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	320	320	ps	±100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
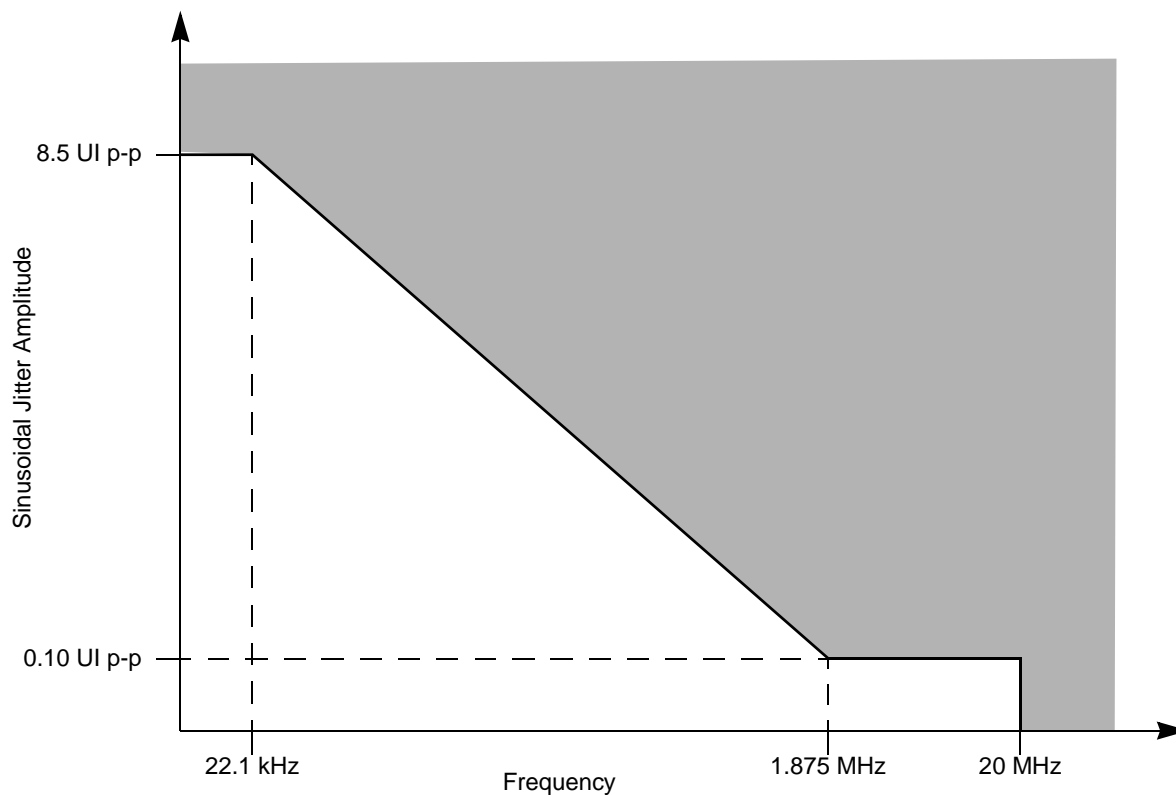
Figure 53. Single Frequency Sinusoidal Jitter Limits

802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100-Ω resistive $\pm$ 5% differential to 2.5 GHz.

18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive $\pm$ 5% differential to 2.5 GHz.

18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 18.7, "Receiver Specifications," and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 54 and Table 69. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 18.7, "Receiver Specifications," is then added to the signal and the test load is replaced by the receiver being tested.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

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Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV$_{DD}$	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV$_{DD}$	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV$_{DD}$	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV$_{DD}$	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV$_{DD}$	—
$\overline{MDQS}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV$_{DD}$	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV$_{DD}$	—
MBA[0:2]	F7, J7, M11	O	GV$_{DD}$	—
$\overline{MWE}$	E7	O	GV$_{DD}$	—
$\overline{MCAS}$	H7	O	GV$_{DD}$	—
$\overline{MRAS}$	L8	O	GV$_{DD}$	—
MCKE[0:3]	F10, C10, J11, H11	O	GV$_{DD}$	11
$\overline{MCS}$[0:3]	K8, J8, G8, F8	O	GV$_{DD}$	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV$_{DD}$	—
$\overline{MCK}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV$_{DD}$	—
MODT[0:3]	E6, K6, L7, M7	O	GV$_{DD}$	—
MDIC[0:1]	A19, B19	I/O	GV$_{DD}$	36

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV$_{DD}$	—
IRQ[8]	AF19	I	OV$_{DD}$	—
IRQ[9]/$\overline{DMA\_DREQ3}$	AF21	I	OV$_{DD}$	1
IRQ[10]/$\overline{DMA\_DACK3}$	AE19	I/O	OV$_{DD}$	1
IRQ[11]/$\overline{DMA\_DDONE3}$	AD20	I/O	OV$_{DD}$	1
$\overline{IRQ\_OUT}$	AD18	O	OV$_{DD}$	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV$_{DD}$	5, 9
EC_MDIO	AC8	I/O	OV$_{DD}$	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV$_{DD}$	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV$_{DD}$	5, 9
TSEC1_COL	R4	I	LV$_{DD}$	—
TSEC1_CRS	V5	I/O	LV$_{DD}$	20
TSEC1_GTX_CLK	U7	O	LV$_{DD}$	—
TSEC1_RX_CLK	U3	I	LV$_{DD}$	—
TSEC1_RX_DV	V2	I	LV$_{DD}$	—
TSEC1_RX_ER	T1	I	LV$_{DD}$	—
TSEC1_TX_CLK	T6	I	LV$_{DD}$	—
TSEC1_TX_EN	U9	O	LV$_{DD}$	30
TSEC1_TX_ER	T7	O	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV$_{DD}$	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV$_{DD}$	5, 9, 33
TSEC2_COL	P1	I	LV$_{DD}$	—
TSEC2_CRS	R6	I/O	LV$_{DD}$	20
TSEC2_GTX_CLK	P6	O	LV$_{DD}$	—
TSEC2_RX_CLK	N4	I	LV$_{DD}$	—
TSEC2_RX_DV	P5	I	LV$_{DD}$	—
TSEC2_RX_ER	R1	I	LV$_{DD}$	—
TSEC2_TX_CLK	P10	I	LV$_{DD}$	—
TSEC2_TX_EN	P7	O	LV$_{DD}$	30

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{SD\_TX}[0:3]$	M23, N21, P23, R21	O	XV$_{DD}$	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV$_{DD}$	24
SD_REF_CLK	T28	I	XV$_{DD}$	—
$\overline{SD\_REF\_CLK}$	T27	I	XV$_{DD}$	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV$_{DD}$	—
System Control				
$\overline{HRESET}$	AG17	I	OV$_{DD}$	—
$\overline{HRESET\_REQ}$	AG16	O	OV$_{DD}$	29
$\overline{SRESET}$	AG20	I	OV$_{DD}$	—
$\overline{CKSTP\_IN}$	AA9	I	OV$_{DD}$	—
$\overline{CKSTP\_OUT}$	AA8	O	OV$_{DD}$	2, 4
Debug				
TRIG_IN	AB2	I	OV$_{DD}$	—
TRIG_OUT/READY/$\overline{QUIESCE}$	AB1	O	OV$_{DD}$	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV$_{DD}$	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV$_{DD}$	6, 19, 29
MDVAL	AE5	O	OV$_{DD}$	6
CLK_OUT	AE21	O	OV$_{DD}$	11
Clock				
RTC	AF16	I	OV$_{DD}$	—
SYSCLK	AH17	I	OV$_{DD}$	—
JTAG				
TCK	AG28	I	OV$_{DD}$	—
TDI	AH28	I	OV$_{DD}$	12

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.
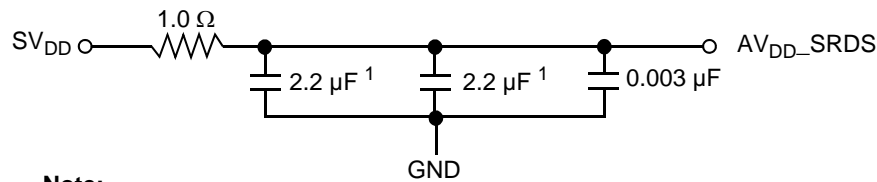
Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK

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Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	04/2008	• Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." • Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. • Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). • Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). • Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	• Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. • Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." • Added Section 4.4, "PCI/PCI-X Reference Clock Timing." • Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." • Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." • Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." • Clarified the reference clock used in Section 7.2, "DUART AC Electrical Specifications." • Corrected V_{IH}(min) in Table 22, "GMII, MII, RMII, and TBI DC Electrical Characteristics." • Corrected V_{IL}(max) in Table 23, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." • Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. • Corrected V_{IH}(min) in Table 36, "MII Management DC Electrical Characteristics." • Corrected t_{MDC}(min) in Table 37, "MII Management AC Timing Specifications." • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKH2}$, $t_{LBIXKH1}$, and $t_{LBIXKH2}$ in Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled" and Table 40, "Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled." • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKL2}$, $t_{LBIXKH1}$, and $t_{LBIXKL2}$ in Table 42, "Local Bus Timing Parameters—PLL Bypassed." Note that $t_{LBIVKL2}$ and $t_{LBIXKL2}$ were previously labeled $t_{LBIVKH2}$ and $t_{LBIXKH2}$. • Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." • Added LGTA signal to Figure 25, Figure 26, Figure 27 and Figure 28. • Corrected LUPWAIT assertion in Figure 26 and Figure 28. • Clarified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" • Added Section 17.1, "Package Parameters." • Added PBGA thermal information in Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid." • Updated." • Updated Table 87, "Part Numbering Nomenclature."
0	07/2007	• Initial Release