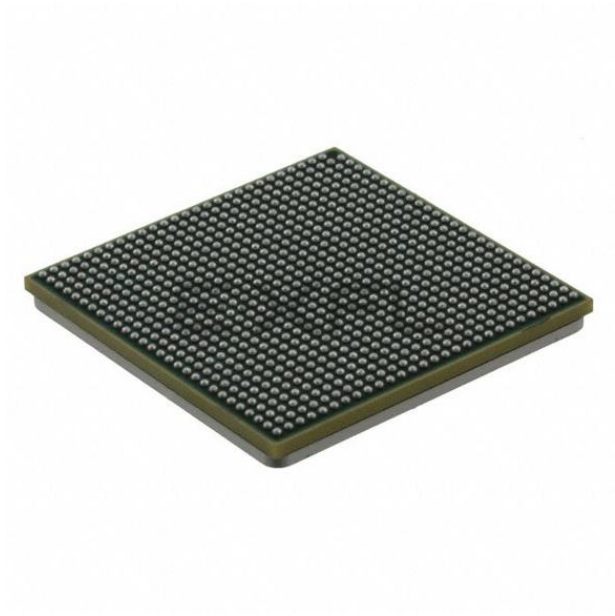

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547ecvjaqgd

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8$ V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5$ V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	t_{CISKEW}	 –300 –365 –390	 300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:
1. Guaranteed by design.
2. f_{CCB} refers to the internal platform clock.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/UPWAIT)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

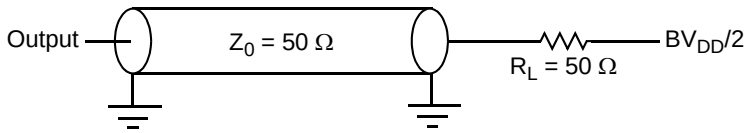

Figure 22. Local Bus AC Test Load

Figure 34 shows the AC timing diagram for the I²C bus.

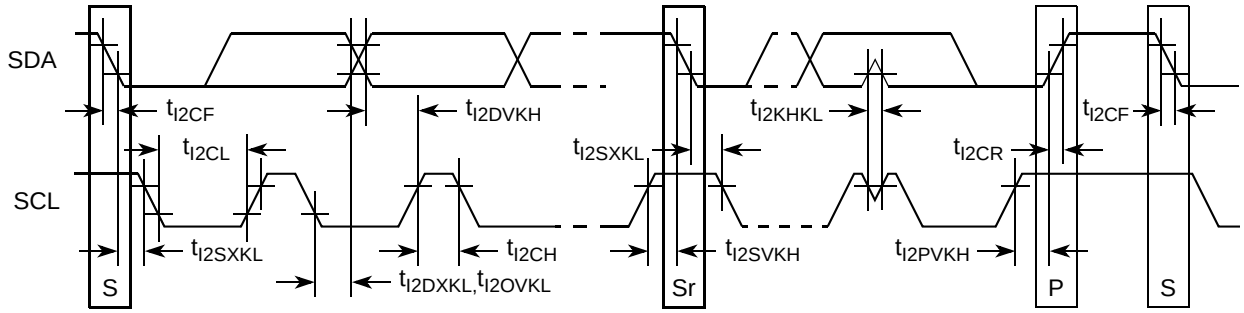

Figure 34. I²C Bus AC Timing Diagram

Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
10. Guaranteed by characterization.
11. Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Table 54. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.2	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

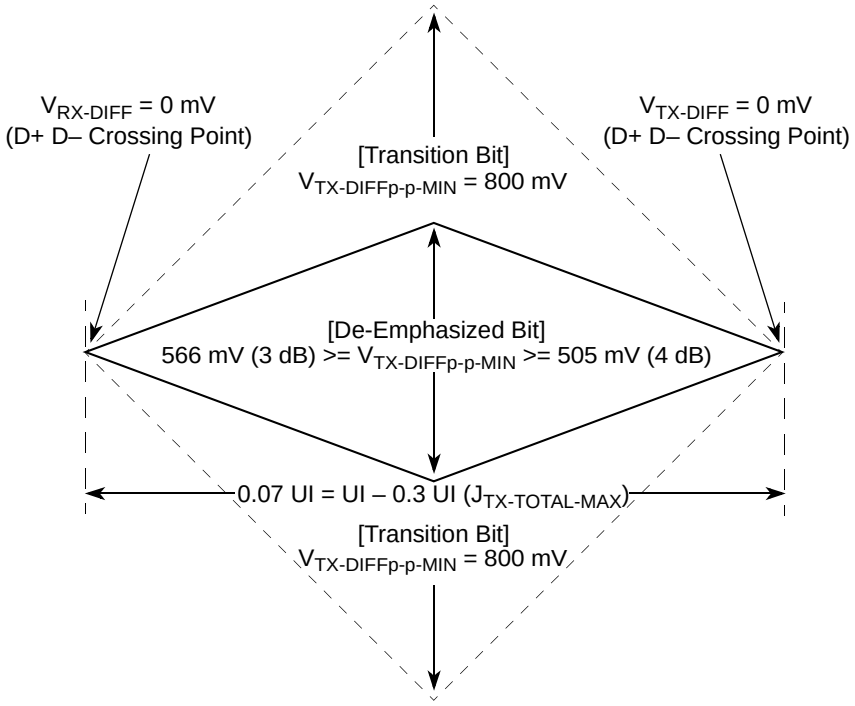

Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$. See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

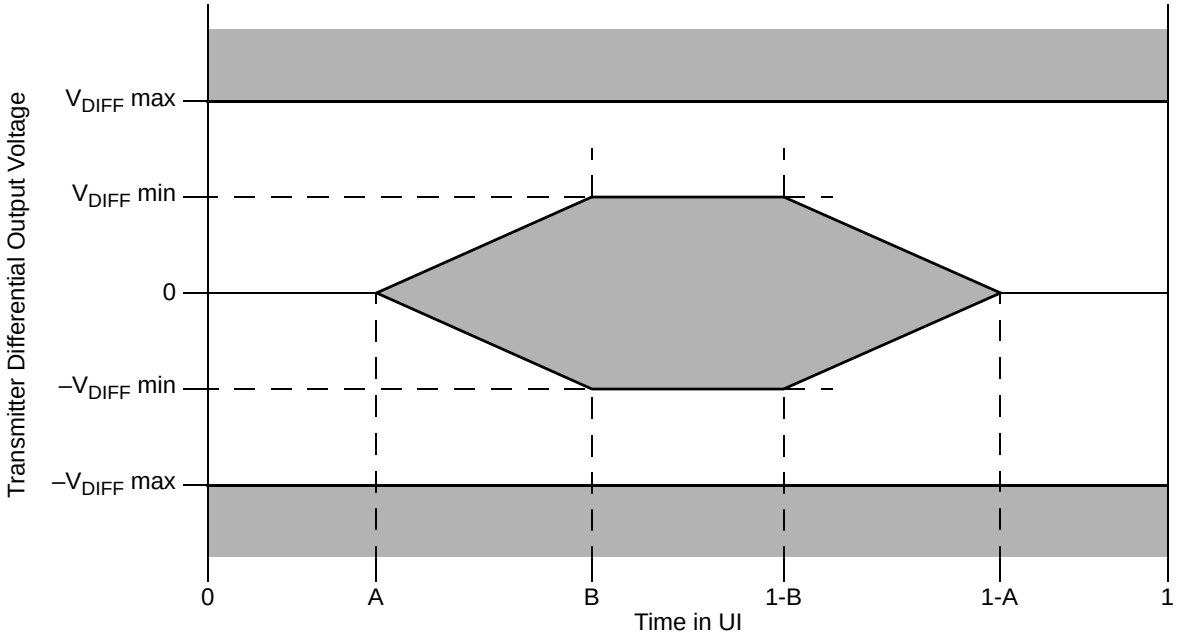

Figure 52. Transmitter Output Compliance Mask

Table 65. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
				—
				—
				—
				—
PCI1_REQ0	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
PCI1_DEVSEL	AH11	I/O	OV_{DD}	2
PCI1_FRAME	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV_{DD}	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV_{DD}	2
PCI2_CLK	AE28	I	OV_{DD}	39
PCI2_IRDY	AD26	I/O	OV_{DD}	2
PCI2_PERR	AD25	I/O	OV_{DD}	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	O	OV_{DD}	5, 9, 35
PCI2_GNT0	AG25	I/O	OV_{DD}	—
PCI2_SERR	AD24	I/O	OV_{DD}	2, 4
PCI2_STOP	AF24	I/O	OV_{DD}	2
PCI2_TRDY	AD27	I/O	OV_{DD}	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV_{DD}	—
PCI2_REQ0	AH25	I/O	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—
MDIC[0:1]	A19, B19	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV_{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV_{DD}	—
LA[27]	H21	O	BV_{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:4]	J25, C20, J24, G26, A26	O	BV_{DD}	
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	D23	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	G20	O	BV_{DD}	1
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	E21	O	BV_{DD}	1
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0]	G25	O	BV_{DD}	5, 9
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1]	C23	O	BV_{DD}	5, 9
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2]	J21	O	BV_{DD}	5, 9
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3]	A24	O	BV_{DD}	5, 9
LALE	H24	O	BV_{DD}	5, 8, 9
LBCTL	G27	O	BV_{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	G22	O	BV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	B27	O	BV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	F24	O	BV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	H23	I/O	BV_{DD}	—
LGPL5	E26	O	BV_{DD}	5, 9
LCKE	E24	O	BV_{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV_{DD}	—

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 72. MPC8547E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 64-Bit or One 32-Bit)				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
PCI1_C_$\overline{BE}$[7:4]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
PCI1_C_$\overline{BE}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
PCI1_PAR64	W15	I/O	OV_{DD}	—
$\overline{PCI1\_GNT}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{PCI1\_GNT0}$	AG5	I/O	OV_{DD}	—
$\overline{PCI1\_IRDY}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{PCI1\_PERR}$	AC12	I/O	OV_{DD}	2
$\overline{PCI1\_SERR}$	V13	I/O	OV_{DD}	2, 4
$\overline{PCI1\_STOP}$	W12	I/O	OV_{DD}	2
$\overline{PCI1\_TRDY}$	AG11	I/O	OV_{DD}	2
$\overline{PCI1\_REQ}$[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
$\overline{PCI1\_REQ0}$	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
$\overline{PCI1\_DEVSEL}$	AH11	I/O	OV_{DD}	2
$\overline{PCI1\_FRAME}$	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
$\overline{PCI1\_REQ64}$	AF14	I/O	OV_{DD}	2, 5,10
$\overline{PCI1\_ACK64}$	V15	I/O	OV_{DD}	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	—

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
PCI1_C_$\overline{BE}$[7:4]/PCI2_C_$\overline{BE}$[3:0]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
PCI1_C_$\overline{BE}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV_{DD}	—
$\overline{PCI1\_GNT}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{PCI1\_GNT0}$	AG5	I/O	OV_{DD}	—
$\overline{PCI1\_IRDY}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{PCI1\_PERR}$	AC12	I/O	OV_{DD}	2
$\overline{PCI1\_SERR}$	V13	I/O	OV_{DD}	2, 4
$\overline{PCI1\_STOP}$	W12	I/O	OV_{DD}	2
$\overline{PCI1\_TRDY}$	AG11	I/O	OV_{DD}	2
$\overline{PCI1\_REQ}$[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
$\overline{PCI1\_REQ0}$	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
$\overline{PCI1\_DEVSEL}$	AH11	I/O	OV_{DD}	2

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV_{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
PCI1_REQ0	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
PCI1_DEVSEL	AH11	I/O	OV_{DD}	2
PCI1_FRAME	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
cfg_pci1_width	AF14	I/O	OV_{DD}	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV_{DD}	—
LSYNC_OUT	F28	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV_{DD}	5, 9, 108
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	—
IRQ[8]	AF19	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	5, 9
EC_MDIO	AC8	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	5, 9
TSEC1_COL	R4	I	LV_{DD}	—
TSEC1_CRS	V5	I/O	LV_{DD}	20
TSEC1_GTX_CLK	U7	O	LV_{DD}	—
TSEC1_RX_CLK	U3	I	LV_{DD}	—
TSEC1_RX_DV	V2	I	LV_{DD}	—
TSEC1_RX_ER	T1	I	LV_{DD}	—
TSEC1_TX_CLK	T6	I	LV_{DD}	—
TSEC1_TX_EN	U9	O	LV_{DD}	30
TSEC1_TX_ER	T7	O	LV_{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV_{DD}	103

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
TEST_SEL	AH14	I	OV_{DD}	109
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—

20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1000 MHz		1200 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 76. Processor Core Clocking Specifications (MPC8545E)

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 87. Part Numbering Nomenclature

MPC	*nnnn*	*t*	*pp*	*ff*	*c*	*r*
Product Code	**Part Identifier**	**Temperature**	**Package[1, 2, 3]**	**Processor Frequency[4]**	**Core Frequency**	**Silicon Version**
MPC	8548E	Blank = 0 to 105°C C = –40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500[3] AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500[5] G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)

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+46 8 52200080 (English)
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+33 1 69 35 48 48 (French)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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