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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8547ecvtaqgb

- Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
 - Flexible configuration.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
 - Four inbound windows plus a default window on RapidIO™
 - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
 - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface
 - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
 - DRAM chip configurations from 64 Mbits to 4 Gbits with $\times 8/\times 16$ data ports
 - Full ECC support
 - Page mode support
 - Up to 16 simultaneous open pages for DDR

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	μs
Local bus PLL lock time	—	50	μs
PCI/PCI-X bus PLL lock time	—	50	μs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.
2. VDD itself is not vulnerable to false ESD triggering; however, as per [Section 22.2, “PLL Power Supply Filtering,”](#) the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

Table 13 provides the recommended operating conditions for the DDR SDRAM controller when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 13. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 2.5 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.15$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($V_{OUT} = 1.95 \text{ V}$)	I_{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35 \text{ V}$)	I_{OL}	16.2	—	mA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail must track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 14 provides the DDR I/O capacitance when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 14. DDR SDRAM Capacitance for $GV_{DD}(\text{typ}) = 2.5 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF} .

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:

- The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

Figure 13 shows the MII receive AC timing diagram.

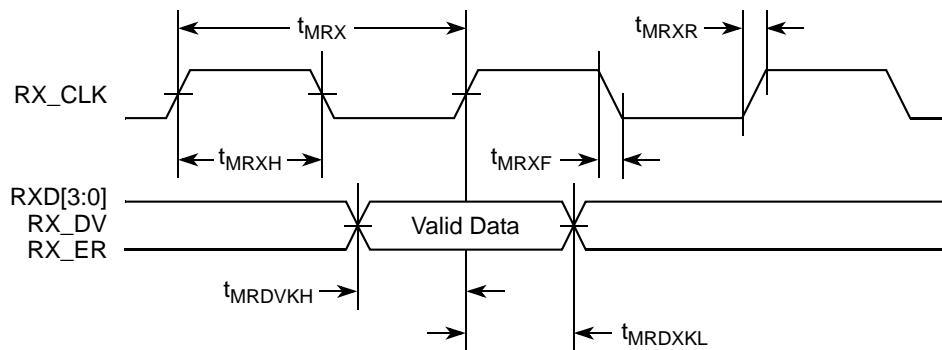


Figure 13. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 30. TBI Transmit AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR}^2	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the device.

10.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3$ V DC.

Table 38. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = BV_{DD}$)	I_{IN}	—	± 5	μ A
High-level output voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2$ mA)	V_{OH}	2.4	—	V
Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V

Note:

- Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

[Table 39](#) provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5$ V DC.

Table 39. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	1.70	$BV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.7	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = BV_{DD}$)	I_{IH}	—	10	μ A
	I_{IL}		-15	
High-level output voltage ($BV_{DD} = \text{min}$, $I_{OH} = -1$ mA)	V_{OH}	2.0	—	V
Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 1$ mA)	V_{OL}	—	0.4	V

Note:

- Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Figure 34 shows the AC timing diagram for the I²C bus.

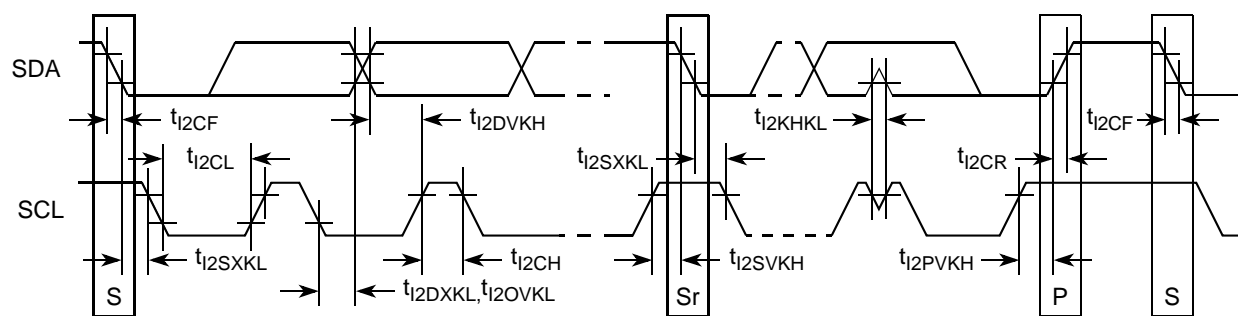


Figure 34. I²C Bus AC Timing Diagram

Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHX}	0	50	ns	6, 11

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.
10. Guaranteed by characterization.
11. Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Table 54. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.2	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

Table 54. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification*.
10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.
11. Guaranteed by characterization.
12. Guaranteed by design.

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

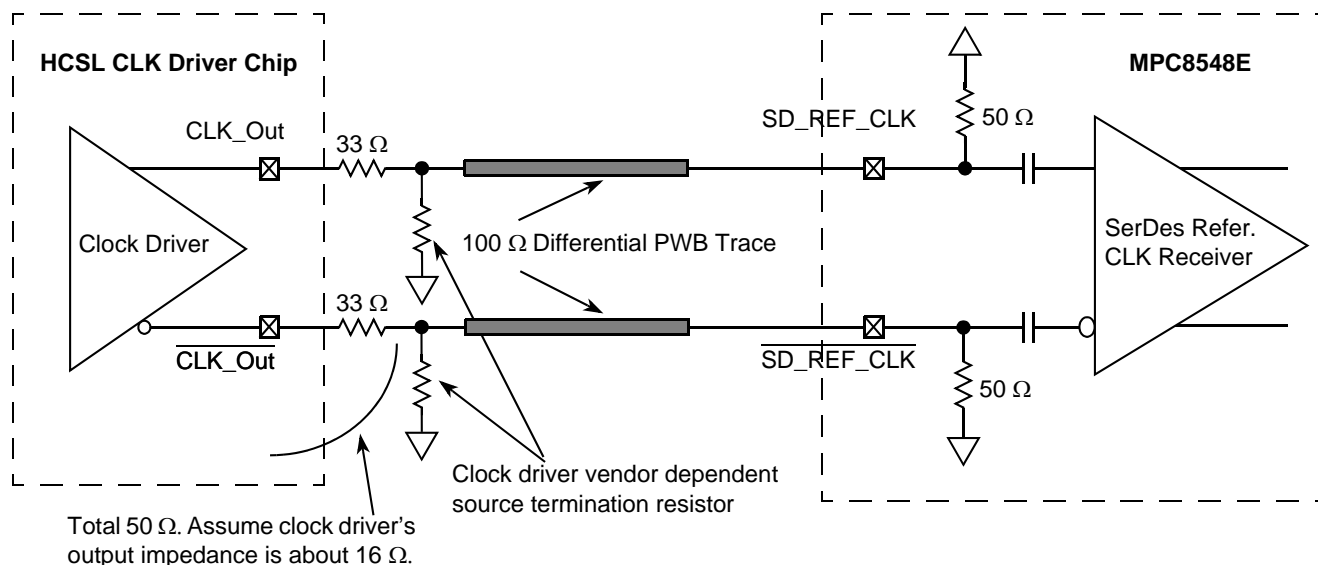


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

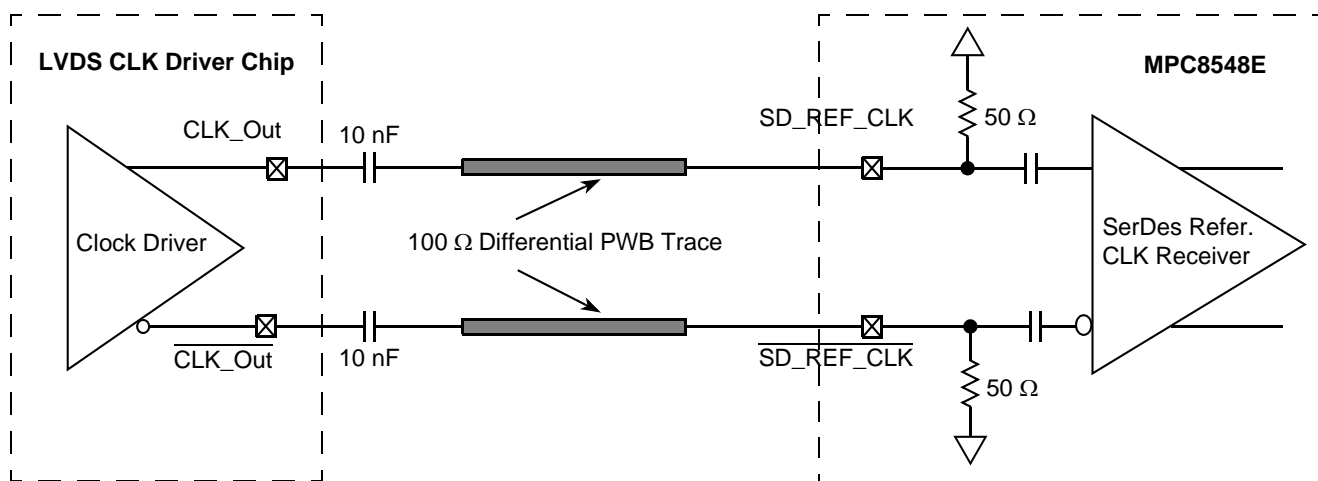


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see [Section 16.2, “SerDes Reference Clocks.”](#)

17.2 AC Requirements for PCI Express SerDes Clocks

[Table 55](#) lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

Note:

1. Typical based on *PCI Express Specification 2.0*.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification, Rev. 1.0a*.

17.4.1 Differential Transmitter (TX) Output

[Table 56](#) defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DC-CM}$	The TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50	—		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
$RL_{TX-DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL_{TX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z_{TX-DC}	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC impedance during all states
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

18 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8548E, for the LP-Serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

18.1 DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see [Section 16.2, “SerDes Reference Clocks.”](#)

18.2 AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

[Table 58](#) lists the Serial RapidIO SD_REF_CLK and SD_REF_CLK AC requirements.

Table 58. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–40	—	40	ps	—

transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

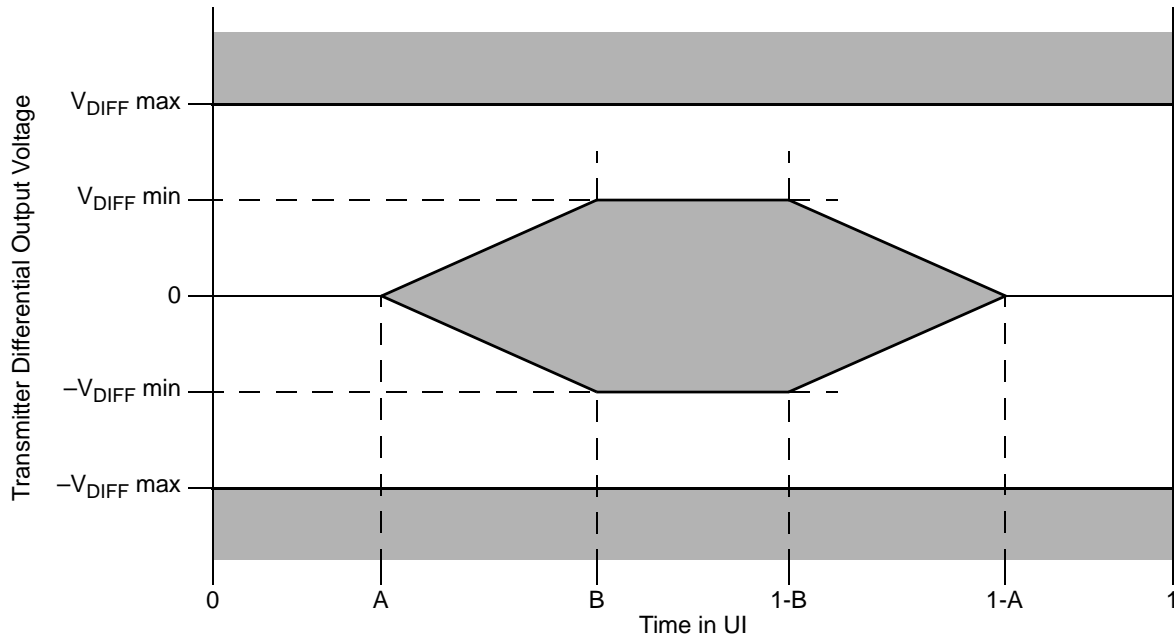


Figure 52. Transmitter Output Compliance Mask

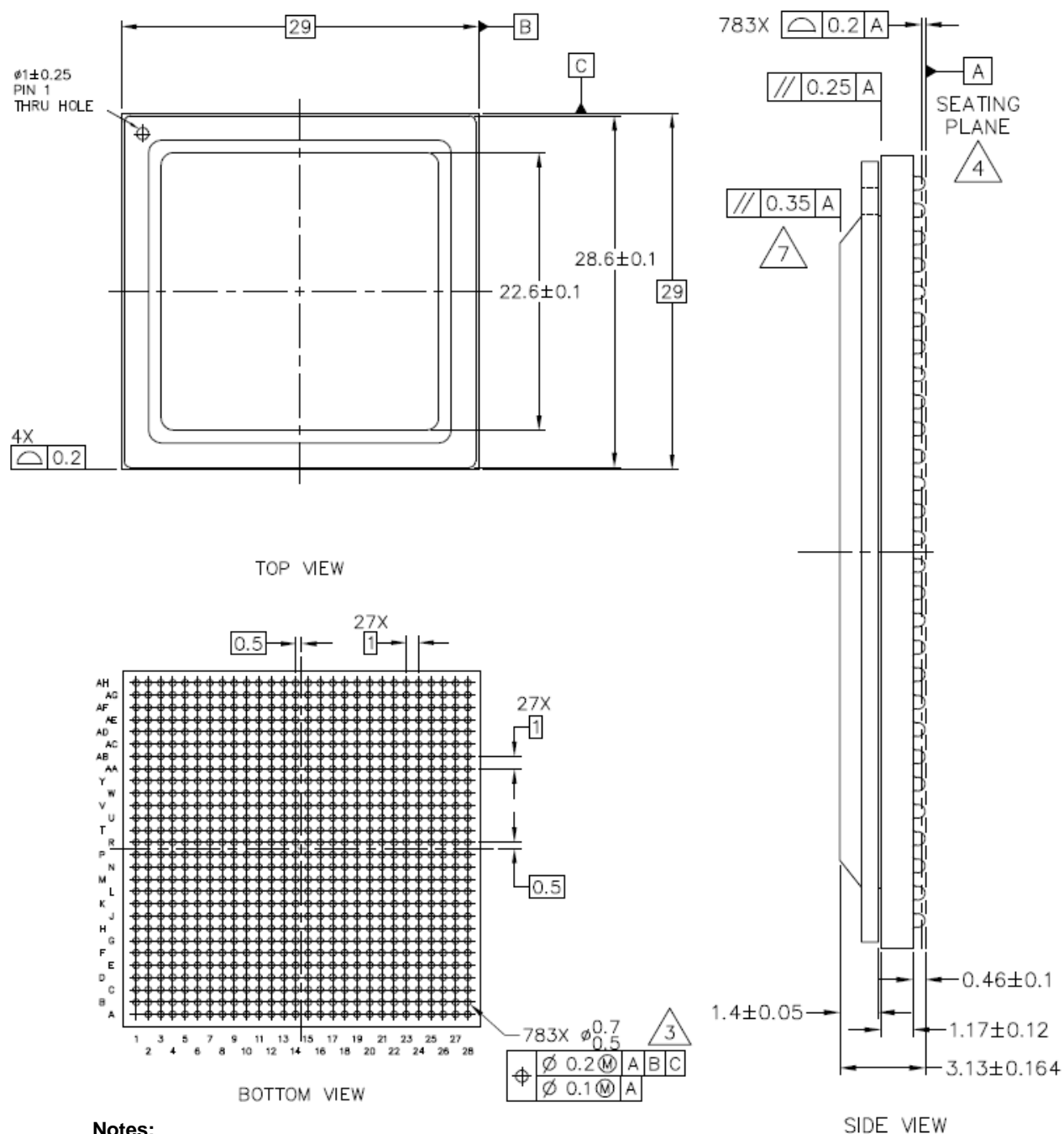
Table 65. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

18.7 Receiver Specifications

LP-serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times$ (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. Parallelism measurement shall exclude any effect of mark on top surface of package.
8. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Figure 56. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV _{DD}	5, 9, 33
TSEC2_COL	P1	I	LV _{DD}	—
TSEC2_CRS	R6	I/O	LV _{DD}	20
TSEC2_GTX_CLK	P6	O	LV _{DD}	
TSEC2_RX_CLK	N4	I	LV _{DD}	—
TSEC2_RX_DV	P5	I	LV _{DD}	—
TSEC2_RX_ER	R1	I	LV _{DD}	—
TSEC2_TX_CLK	P10	I	LV _{DD}	—
TSEC2_TX_EN	P7	O	LV _{DD}	30
TSEC2_TX_ER	R10	O	LV _{DD}	5, 9, 33
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	—
TSEC3_GTX_CLK	W8	O	TV _{DD}	—
TSEC3_RX_CLK	W2	I	TV _{DD}	—
TSEC3_RX_DV	W1	I	TV _{DD}	—
TSEC3_RX_ER	Y2	I	TV _{DD}	—
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	O	TV _{DD}	30
Three-Speed Ethernet Controller (Gigabit Ethernet 4)				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV _{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1
TSEC4_GTX_CLK	AA5	O	TV _{DD}	—
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV _{DD}	1, 30
DUART				
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	O	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV _{DD}	—

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 72. MPC8547E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 64-Bit or One 32-Bit)				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
PCI1_REQ64	AF14	I/O	OV _{DD}	2, 5, 10
PCI1_ACK64	V15	I/O	OV _{DD}	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	O	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	O	LV _{DD}	30
TSEC1_TX_ER	T7	O	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	—
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O	LV _{DD}	5, 9, 33
TSEC2_COL	P1	I	LV _{DD}	—
TSEC2_CRS	R6	I/O	LV _{DD}	20
TSEC2_GTX_CLK	P6	O	LV _{DD}	—
TSEC2_RX_CLK	N4	I	LV _{DD}	—
TSEC2_RX_DV	P5	I	LV _{DD}	—
TSEC2_RX_ER	R1	I	LV _{DD}	—
TSEC2_TX_CLK	P10	I	LV _{DD}	—
TSEC2_TX_EN	P7	O	LV _{DD}	30

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FIFO1_RXC2	P5	I	LV _{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV _{DD}	15
cfg_dram_type1	R10	I	LV _{DD}	5
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	—
TSEC3_GTX_CLK	W8	O	TV _{DD}	—
TSEC3_RX_CLK	W2	I	TV _{DD}	—
TSEC3_RX_DV	W1	I	TV _{DD}	—
TSEC3_RX_ER	Y2	I	TV _{DD}	—
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	O	TV _{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV _{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV _{DD}	—
TSEC3_CRS	AA3	I/O	TV _{DD}	31
TSEC3_TX_ER	AB6	O	TV _{DD}	—
DUART				
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	O	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV _{DD}	—
I²C interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV _{DD}	—
SD_RX[0:3]	M27, N25, P27, R25	I	XV _{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	O	XV _{DD}	—

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 23.1, “Part Numbers Fully Addressed by this Document.”](#)

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 87. Part Numbering Nomenclature

MPC	nnnnn	t	pp	ff	c	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8548E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 ³ AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 ⁵ G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	04/2009	<ul style="list-style-type: none"> In Table 1, “Absolute Maximum Ratings ¹,” and in Table 2, “Recommended Operating Conditions,” moved text, “MII management voltage” from LV_{DD}/TV_{DD} to OV_{DD}, added “Ethernet management” to OVDD row of input voltage section. In Table 5, “SYSCLK AC Timing Specifications,” added notes 7 and 8 to SYSCLK frequency and cycle time. In Table 36, “MII Management DC Electrical Characteristics,” changed all instances of LV_{DD}/OV_{DD} to OV_{DD}. Modified Section 16, “High-Speed Serial Interfaces (HSSI),” to reflect that there is only one SerDes. Modified DDR clk rate min from 133 to 166 MHz. Modified note in Table 75, “Processor Core Clocking Specifications (MPC8548E and MPC8547E), “. ” In Table 56, “Differential Transmitter (TX) Output Specifications,” modified equations in Comments column, and changed all instances of “LO” to “L0.” Also added note 8. In Table 57, “Differential Receiver (RX) Input Specifications,” modified equations in Comments column, and in note 3, changed “TRX-EYE-MEDIAN-to-MAX-JITTER,” to “T_{RX-EYE-MEDIAN-to-MAX-JITTER}.” Modified Table 83, “Frequency Options of SYSCLK with Respect to Memory Bus Speeds.” Added a note on Section 4.1, “System Clock Timing,” to limit the SYSCLK to 100 MHz if the core frequency is less than 1200 MHz In Table 71, “MPC8548E Pinout Listing”Table 72, “MPC8547E Pinout Listing”Table 73, “MPC8545E Pinout Listing”Table 74, “MPC8543E Pinout Listing,” added note 5 to LA[28:31]. Added note to Table 83, “Frequency Options of SYSCLK with Respect to Memory Bus Speeds.”
3	01/2009	<ul style="list-style-type: none"> [Section 4.6, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.” Changed minimum frequency equation to be 527 MHz for PCI x8. In Table 5, added note 7. Section 4.5, “Platform to FIFO Restrictions.” Changed platform clock frequency to 4.2. Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” Added MII after GMII and add ‘or 2.5 V’ after 3.3 V. In Table 23, modified table title to include GMII, MII, RMII, and TBI. In Table 24 and Table 25, changed clock period minimum to 5.3. In Table 25, added a note. In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title. In Table 30 and Figure 15, changed all instances of PMA to TSEC_n. In Section 8.2.5, “TBI Single-Clock Mode AC Specifications.” Replaced first paragraph. In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC_n_TX_CLK. In Table 36, changed all instances of OV_{DD} to LV_{DD}/TV_{DD}. In Table 37, “MII Management AC Timing Specifications,” changed MDC minimum clock pulse width high from 32 to 48 ns. Added new section, Section 16, “High-Speed Serial Interfaces (HSSI).” Section 16.1, “DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK.” Added new paragraph. Section 17.1, “DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK.” Added new paragraph. Added information to Figure 63, both in figure and in note. Section 22.3, “Decoupling Recommendations.” Modified the recommendation. Table 87, “Part Numbering Nomenclature.” In Silicon Version column added Ver. 2.1.2.