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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547epxaujd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview



Figure 1. Device Block Diagram

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
 - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
 - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
 - 36-bit real addressing
 - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
 - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
 - Enhanced hardware and software debug support

Overview

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high-resolution timers/counters that can generate interrupts
 - Supports a variety of other internal interrupt sources
 - Supports fully nested interrupt delivery
 - Interrupts can be routed to external pin for external processing.
 - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
 - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - PKEU—public key execution unit
 - RSA and Diffie-Hellman; programmable field size up to 2048 bits
 - Elliptic curve cryptography with F_2m and F(p) modes and programmable field size up to 511 bits
 - DEU—Data Encryption Standard execution unit
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	1
	45(default) 45(default)	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	
PCI signals	25	OV _{DD} = 3.3 V	2
	45(default)		
DDR signal	18 36 (half strength mode)	GV _{DD} = 2.5 V	3
DDR2 signal	18 36 (half strength mode)	GV _{DD} = 1.8 V	3
TSEC/10/100 signals	45	L/TV _{DD} = 2.5/3.3 V	
DUART, system control, JTAG	45	OV _{DD} = 3.3 V	—
12C	150	OV _{DD} = 3.3 V	_

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.

3. The drive strength of the DDR interface in half-strength mode is at $T_i = 105^{\circ}C$ and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

- 1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
- 2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	AC Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t _{TRX}	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t _{SKTRX}	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t _{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t _{TRDXKH}	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t _{TRXR} ²	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t _{TRXF} ²	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}

2. Guaranteed by design.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 19 provides the AC test load for eTSEC.



Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.



Figure 20. RMII Receive AC Timing Diagram

Ethernet Management Interface Electrical Characteristics

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum f_{MDC} = f_{CCB} ÷ 64 and minimum f_{MDC} = f_{CCB} ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

Parameter	Symbol ¹	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-1.3		ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5		ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	_	-0.3	ns	
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	_	-0.1	ns	4
Local bus clock to address valid for LAD	t _{LBKLOV3}	_	0	ns	4
Local bus clock to LALE assertion	t _{LBKLOV4}	_	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-3.7	_	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-3.7	_	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	_	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}		0.2	ns	7

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

 All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.

3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.

5. Input timings are measured at the pin.

6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.

7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 8. Guaranteed by characterization.
- 9. Guaranteed by design.



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Local Bus



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

l²C

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the device.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 45. I²C DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7 \times OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	
Low level output voltage	V _{OL}	0	$0.2\times \text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	3
Capacitance for each I/O pin	CI		10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2. See the MPC8548E PowerQUICC[™] III Integrated Processor Family Reference Manual, for information on the digital filter used.
- 3. I/O pins obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 46. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Мах	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μS	4
High period of the SCL clock	t _{I2CH}	0.6	—	μS	4
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS	4
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs	4
Data setup time	t _{I2DVKH}	100	—	ns	4
Data input hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0		μS	2
Data output delay time:	t _{I2OVKL}	—	0.9	—	3
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS	

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 18.2, "AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK"

16.2.4.1 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK are designed to work with a spread spectrum clock (+0% to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 47. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, "PCI Express"
- Section 18, "Serial RapidIO"

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

Table 56. Differential Transmitter	· (TX) Output	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{TX-DC-CM}	The TX DC common mode voltage	0	_	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX short circuit current limit	_	_	90	mA	The total current the transmitter can provide when shorted to its ground
T _{TX-IDLE-MIN}	Minimum time spent in electrical idle	50	_		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
RL _{TX-DIFF}	Differential return loss	12	_	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL _{TX-CM}	Common mode return loss	6		—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z _{TX-DIFF-DC}	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z _{TX-DC}	Transmitter DC impedance	40	_	_	Ω	Required TX D+ as well as D– DC impedance during all states
L _{TX-SKEW}	Lane-to-lane output skew	_	_	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C _{TX}	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

Package Description



- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
- 7. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 8. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Figure 56. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
				_
				_
				_
				_
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV _{DD}	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV _{DD}	2
PCI2_CLK	AE28	I	OV _{DD}	39
PCI2_IRDY	AD26	I/O	OV _{DD}	2
PCI2_PERR	AD25	I/O	OV _{DD}	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	0	OV _{DD}	5, 9, 35
PCI2_GNT0	AG25	I/O	OV _{DD}	_
PCI2_SERR	AD24	I/O	OV _{DD}	2, 4
PCI2_STOP	AF24	I/O	OV _{DD}	2
PCI2_TRDY	AD27	I/O	OV _{DD}	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV _{DD}	—
PCI2_REQ0	AH25	I/O	OV _{DD}	—
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	_
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	_
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 71. MPC8548E Pinout Listing (continued)

Package Description

Table 73.	MPC8545E	Pinout	Listing	(continued)
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Signal	Pin Type	Power Supply	Notes						
SD_TX[0:3]	M23, N21, P23, R21	0	XV _{DD}	—					
Reserved	W26, Y28, AA26, AB28	—	—	40					
Reserved	W25, Y27, AA25, AB27	—	—	40					
Reserved	U20, V22, W20, Y22	_	—	15					
Reserved	U21, V23, W21, Y23	—	—	15					
SD_PLL_TPD	U28	0	XV _{DD}	24					
SD_REF_CLK	T28	I	XV _{DD}	—					
SD_REF_CLK	T27	I	XV _{DD}	—					
Reserved	AC1, AC3	—	—	2					
Reserved	M26, V28	—	—	32					
Reserved	M25, V27	—	—	34					
Reserved	M20, M21, T22, T23	—	—	38					
	General-Purpose Output								
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—					
	System Control								
HRESET	AG17	I	OV _{DD}	—					
HRESET_REQ	AG16	0	OV _{DD}	29					
SRESET	AG20	I	OV _{DD}	—					
CKSTP_IN	AA9	I	OV _{DD}	—					
CKSTP_OUT	AA8	0	OV _{DD}	2, 4					
	Debug								
TRIG_IN	AB2	I	OV _{DD}	—					
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29					
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9					
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29					
MDVAL	AE5	0	OV _{DD}	6					
CLK_OUT	AE21	0	OV _{DD}	11					
Clock									
RTC	AF16	I	OV _{DD}	—					
SYSCLK	AH17	I	OV _{DD}	—					
JTAG									
ТСК	AG28	I	OV _{DD}	—					
TDI	AH28	I	OV _{DD}	12					

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—		
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9		
GPOUT7	N6	0	LV _{DD}	—		
Reserved	P1		_	104		
Reserved	R6	—	—	104		
Reserved	P6		_	15		
Reserved	N4	—	—	105		
FIFO1_RXC2	P5	I	LV _{DD}	104		
Reserved	R1	—	—	104		
Reserved	P10	—				
FIFO1_TXC2	P7	0	LV _{DD}	15		
cfg_dram_type1	R10	0	LV _{DD}	5, 9		
Thr	ee-Speed Ethernet Controller (Gigabit I	Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29		
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_		
TSEC3_GTX_CLK	W8	0	TV _{DD}	_		
TSEC3_RX_CLK	W2	I	TV _{DD}	_		
TSEC3_RX_DV	W1	I	TV _{DD}	_		
TSEC3_RX_ER	Y2	I	TV _{DD}	_		
TSEC3_TX_CLK	V10	I	TV _{DD}	—		
TSEC3_TX_EN	V9	0	TV _{DD}	30		
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	5, 9, 29		
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	_		
Reserved	AA5	—	—	15		
TSEC3_COL	Y5	I	TV _{DD}	—		
TSEC3_CRS	AA3	I/O	TV _{DD}	31		
TSEC3_TX_ER	AB6	0	TV _{DD}	—		
	DUART	1				
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	_		
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—		
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	_		
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	—		
	I ² C interface	1 1				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27		

Table 74. MPC8543E Pinout Listing (continued)

20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

Characteristic	Maximum Process		Process	essor Core Frequency		y MH-	lluit	Neteo
Characteristic			1200		1000		Unit	notes
	Min	Мах	Min	Мах	Min	Мах		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

 Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)

Notes:

 Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.) The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 76. Processor Core Clocking Specifications (MPC8545E)

	Maximum Processor Core Frequency							
Characteristic	800	MHz	1000 MHz		1200 MHz		Unit	Notes
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a $1-\mu F$ ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA_DACK[0:1], and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout

23 Ordering Information

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Ordering information for the parts fully covered by this specification document is provided in Section 23.1, "Part Numbers Fully Addressed by this Document."

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	t	pp	11	C	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8548E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 ³ AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 ⁵ G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)

Table 87. Part Numbering Nomenclature

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