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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547evjaqgd

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high-resolution timers/counters that can generate interrupts
 - Supports a variety of other internal interrupt sources
 - Supports fully nested interrupt delivery
 - Interrupts can be routed to external pin for external processing.
 - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
 - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - PKEU—public key execution unit
 - RSA and Diffie-Hellman; programmable field size up to 2048 bits
 - Elliptic curve cryptography with F_2^m and $F(p)$ modes and programmable field size up to 511 bits
 - DEU—Data Encryption Standard execution unit
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES

- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		
400 MHz		–365	365		
333 MHz		–390	390		

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

A summary of the FIFO AC specifications appears in [Table 24](#) and [Table 25](#).

Table 24. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See [Section 4.5, “Platform to FIFO Restrictions.”](#)

Timing diagrams for FIFO appear in [Figure 6](#) and [Figure 7](#).

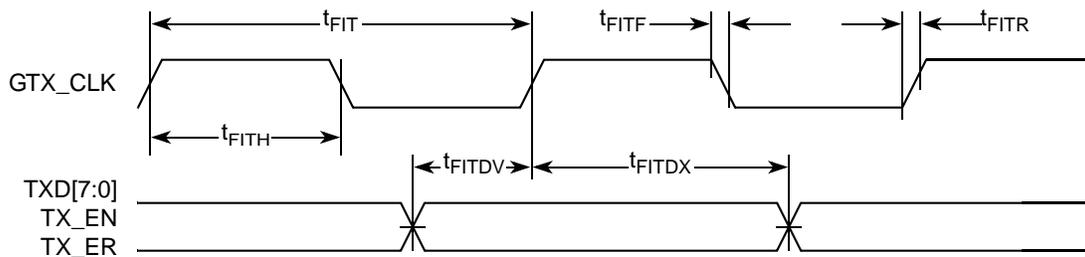


Figure 6. FIFO Transmit AC Timing Diagram

Figure 8 shows the GMII transmit AC timing diagram.

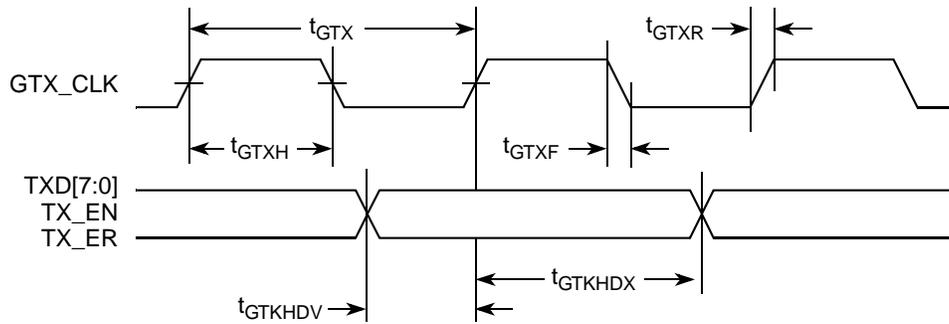


Figure 8. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}^2	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 9 provides the AC test load for eTSEC.

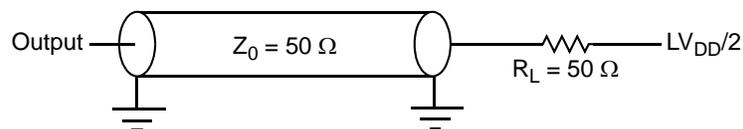


Figure 9. eTSEC AC Test Load

Table 34. RMIIT Transmit AC Timing Specifications (continued)

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSEC _n _TX_CLK to RMIIT data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 18 shows the RMIIT transmit AC timing diagram.

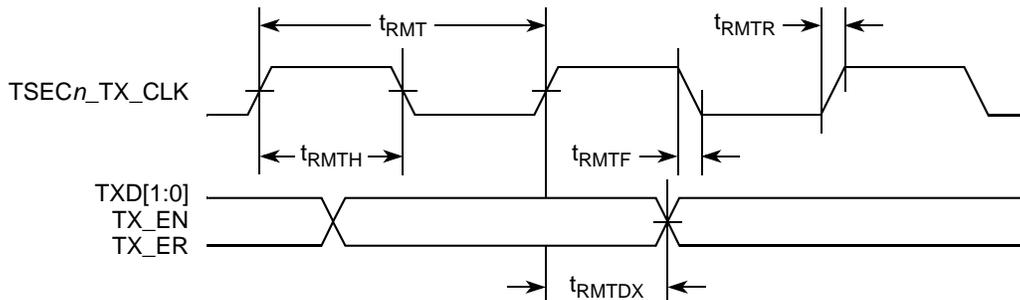


Figure 18. RMIIT Transmit AC Timing Diagram

8.2.7.2 RMIIT Receive AC Timing Specifications

Table 35. RMIIT Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TSEC _n _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC _n _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC _n _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	—	250	ps
Rise time TSEC _n _TX_CLK(20%–80%)	t _{RMRR}	1.0	—	2.0	ns
Fall time TSEC _n _TX_CLK (80%–20%)	t _{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDV}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 provides the AC test load for eTSEC.

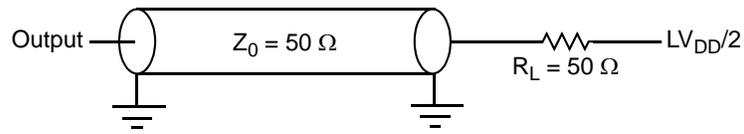


Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.

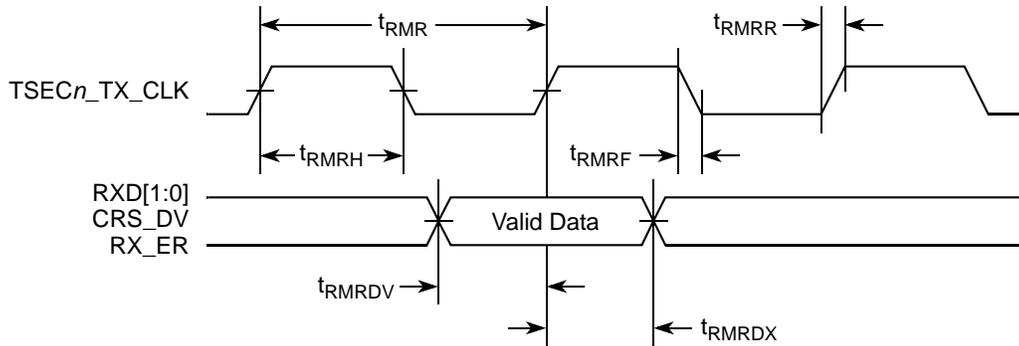


Figure 20. RMII Receive AC Timing Diagram

Local Bus

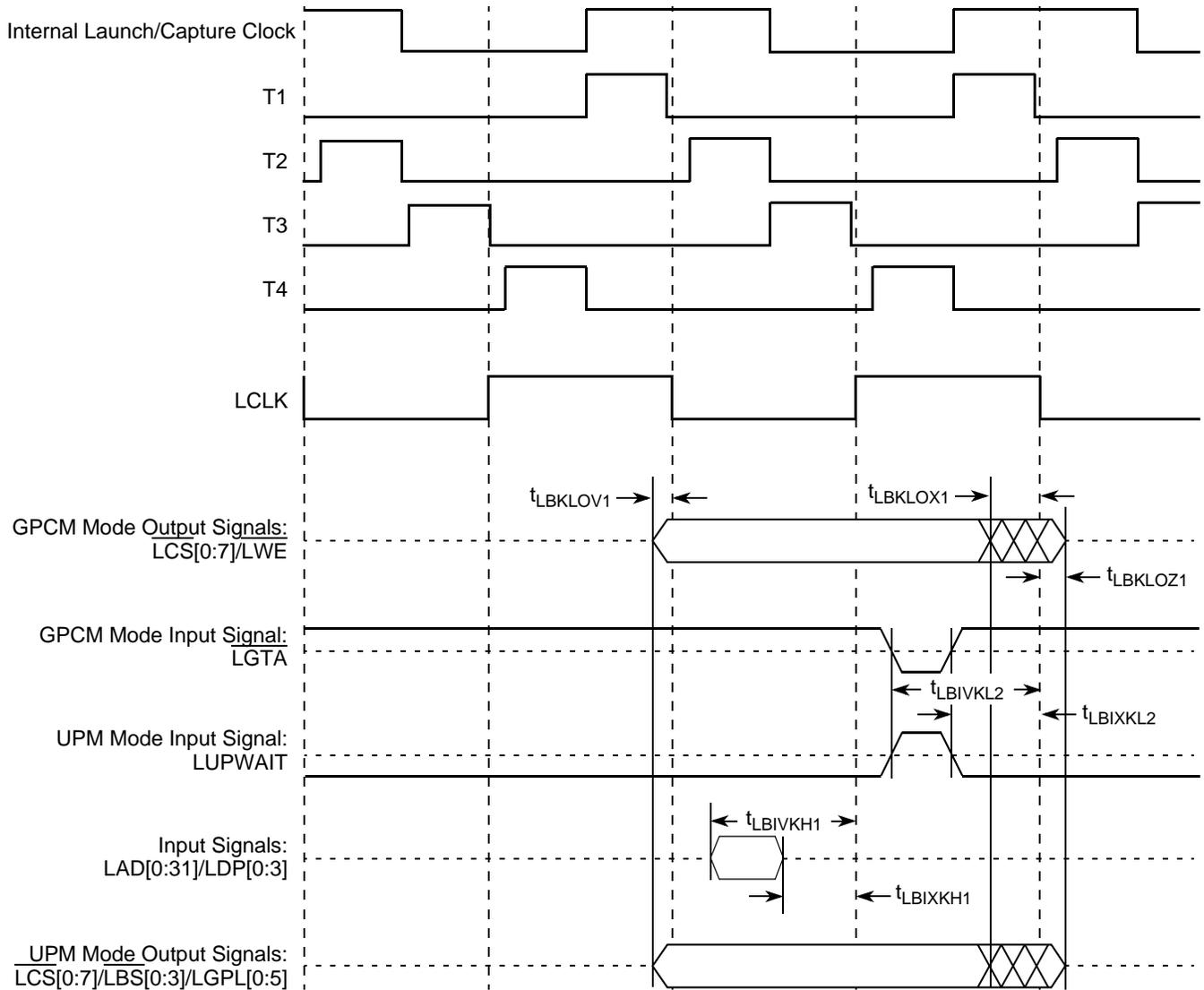


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol ¹	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = V_{DD}$)	I_{IN}	—	± 5	μ A
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2$ mA)	V_{OH}	2.4	—	V
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} .

12.2 JTAG AC Electrical Specifications

This table provides the JTAG AC timing specifications as defined in [Figure 30](#) through [Figure 32](#).

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
\overline{TRST} assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	— —		4

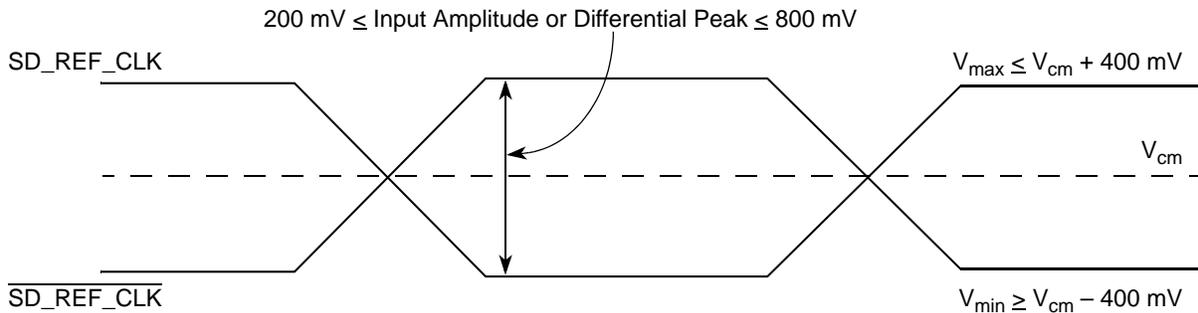


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

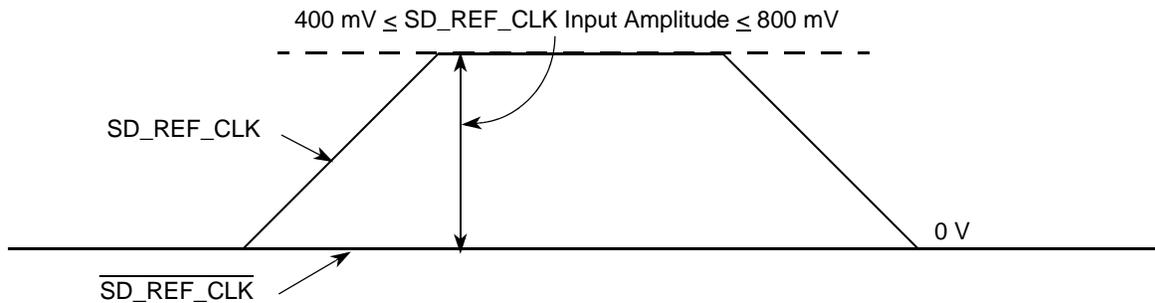


Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to $SGND_SRDSn$ ($xcorevss$), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{\text{crosslink}}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 50](#) and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in [Figure 48](#).)
3. A $T_{\text{TX-EYE}} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{\text{TX-JITTER-MAX}} = 0.30$ UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see [Figure 50](#)). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in [Figure 50](#) for both $V_{\text{TX-D+}}$ and $V_{\text{TX-D-}}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications Rev 1.0a*.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications Rev 1.0a*.
8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in [Figure 48](#) is specified using the passive compliance/test measurement load (see [Figure 50](#)) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

components are included in this requirement. The reference impedance for return loss measurements is 100- Ω resistive for differential return loss and 25- Ω resistive for common mode.

Table 66. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	800	800	ps	± 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 53](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	400	400	ps	± 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 53](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

19 Package Description

This section details package parameters, pin assignments, and dimensions.

19.1 Package Parameters

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are provided in [Table 70](#).

Table 70. Package Parameters

Parameter	CBGA ¹	PBGA ²
Package outline	29 mm × 29 mm	29 mm × 29 mm
Interconnects	783	783
Ball pitch	1 mm	1 mm
Ball diameter (typical)	0.6 mm	0.6 mm
Solder ball	63% Sn 37% Pb 0% Ag	63% Sn 37% Pb 0% Ag
Solder ball (lead-free)	95% Sn 4.5% Ag 0.5% Cu	96.5% Sn 3.5% Ag

Notes:

1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
2. The FC-PBGA package is available on only versions 2.1.1 and 2.1.2, and 3.0 of the device.

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AC25	I	OV _{DD}	25
L2_TSTCLK	AE22	I	OV _{DD}	25
$\overline{\text{LSSD_MODE}}$	AH20	I	OV _{DD}	25
$\overline{\text{TEST_SEL}}$	AH14	I	OV _{DD}	25
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV _{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	—
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2.5 V, 3.3 V)	TV _{DD}	—
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}	—

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 32-Bit)				
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	—	—	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	O	OV _{DD}	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV _{DD}	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
Reserved	AF15, AD14, AE15, AD15	—	—	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
Reserved	W15	—	—	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2

Table 85. Package Thermal Characteristics for FC-PBGA (continued)

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-board	N/A	$R_{\theta JB}$	5	°C/W	3
Die junction-to-case	N/A	$R_{\theta JC}$	0.8	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed-circuit board is the recommended procedure using a maximum of 10 lbs force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

22 System Design Information

This section provides electrical design recommendations for successful application of the device.

22.1 System Clocking

This device includes five PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 20.2, “CCB/SYSCLK PLL Ratio.”](#)
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 20.3, “e500 Core PLL Ratio.”](#)
3. The PCI PLL generates the clocking for the PCI bus.
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CORE} , AV_{DD_PCI} , AV_{DD_LBIU} , and AV_{DD_SRDS} , respectively). The AV_{DD}

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 63](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 63](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in [Figure 62](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 62](#) is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD_TX}}[7:0]$
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}[7:0]$
- SD_REF_CLK
- $\overline{\text{SD_REF_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin `cfg_srds_en` on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD_TX}}[7:0]$
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}[7:0]$
- SD_REF_CLK

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 87. Part Numbering Nomenclature

MPC	nnnnn	t	pp	ff	c	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8548E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 ³ AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 ⁵ G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)