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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547evjatgd

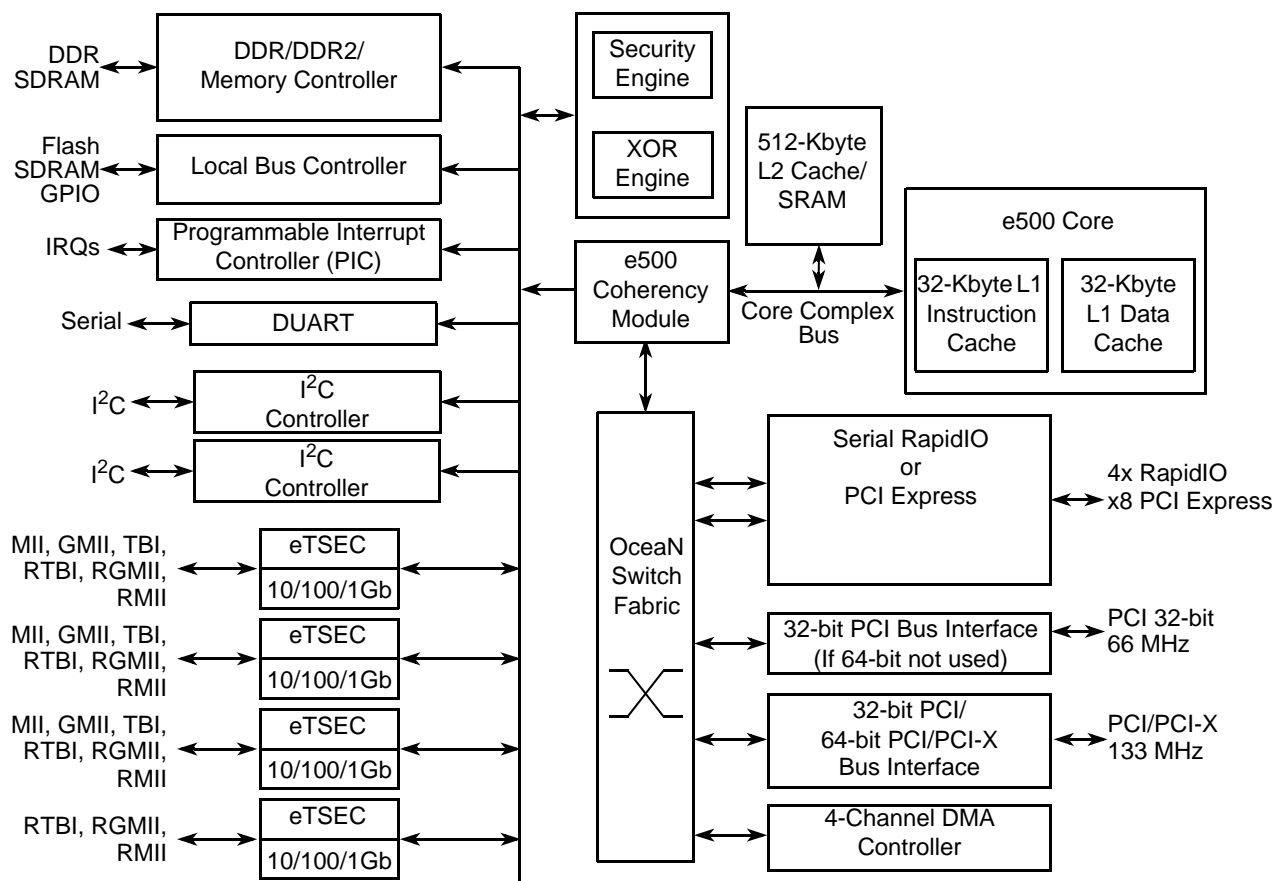


Figure 1. Device Block Diagram

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
 - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
 - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
 - 36-bit real addressing
 - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
 - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
 - Enhanced hardware and software debug support

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high-resolution timers/counters that can generate interrupts
 - Supports a variety of other internal interrupt sources
 - Supports fully nested interrupt delivery
 - Interrupts can be routed to external pin for external processing.
 - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
 - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - PKEU—public key execution unit
 - RSA and Diffie-Hellman; programmable field size up to 2048 bits
 - Elliptic curve cryptography with F_2m and $F(p)$ modes and programmable field size up to 511 bits
 - DEU—Data Encryption Standard execution unit
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the device. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	2
Three-speed Ethernet I/O voltage		LV_{DD} (for eTSEC1 and eTSEC2) TV_{DD} (for eTSEC3 and eTSEC4)	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 3.63 –0.3 to 2.75	V	3
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to ($GV_{DD} + 0.3$)	V	4
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to ($GV_{DD}/2 + 0.3$)	V	—
	Three-speed Ethernet I/O signals	LV_{IN} TV_{IN}	–0.3 to ($LV_{DD} + 0.3$) –0.3 to ($TV_{DD} + 0.3$)	V	4
	Local bus signals	BV_{IN}	–0.3 to ($BV_{DD} + 0.3$)	—	—
	DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV_{IN}	–0.3 to ($OV_{DD} + 0.3$)	V	4
	PCI/PCI-X	OV_{IN}	–0.3 to ($OV_{DD} + 0.3$)	V	4

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see [Table 2](#)) with $OV_{DD} = 3.3\text{ V} \pm 165\text{ mV}$.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	16	—	133	MHz	1 , 6 , 7 , 8
SYSCLK cycle time	t_{SYSCLK}	7.5	—	60	ns	6 , 7 , 8
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	± 150	ps	4 , 5

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2](#), “CCB/SYSCLK PLL Ratio,” and [Section 20.3](#), “e500 Core PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth must be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
7. For spread spectrum clocking. Guidelines are + 0% to –1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{\text{CCB}}$, and minimum clock low time is $2 \times t_{\text{CCB}}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 13 provides the recommended operating conditions for the DDR SDRAM controller when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 13. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 2.5 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.15$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($V_{OUT} = 1.95 \text{ V}$)	I_{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35 \text{ V}$)	I_{OL}	16.2	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail must track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 14 provides the DDR I/O capacitance when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 14. DDR SDRAM Capacitance for $GV_{DD}(\text{typ}) = 2.5 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF} .

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}[n]$ crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	1.48 1.95 2.40	— — —	ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}[n]$ output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}[n]$ output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCX}	1.48 1.95 2.40	— — —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	$t_{\text{DDKHDS}},$ t_{DDKLDS}	538 700 900	— — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	$t_{\text{DDKHDX}},$ t_{DDKLDX}	538 700 900	— — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{\text{MCK}} - 0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	6

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = V_{DD}$)	I_{IN}	—	± 5	μ A
High-level output voltage ($OV_{DD} = \min$, $I_{OH} = -2$ mA)	V_{OH}	2.4	—	V
Low-level output voltage ($OV_{DD} = \min$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB}/1,048,576$	baud	1, 2
Maximum baud rate	$f_{CCB}/16$	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:

- Guaranteed by design.
- f_{CCB} refers to the internal platform clock.
- Actual attainable baud rate is limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND -0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	10	μA	1, 2, 3
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-15	—	μA	3

Notes:

1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#) and [Table 2](#).

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSECn's TSECn_TX_CLK, while the receive clock must be applied to pin TSECn_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSECn_GTX_CLK pin (while transmit data appears on TSECn_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSECn_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see [Section 4.5, "Platform to FIFO Restrictions."](#)

Figure 11 shows the MII transmit AC timing diagram.

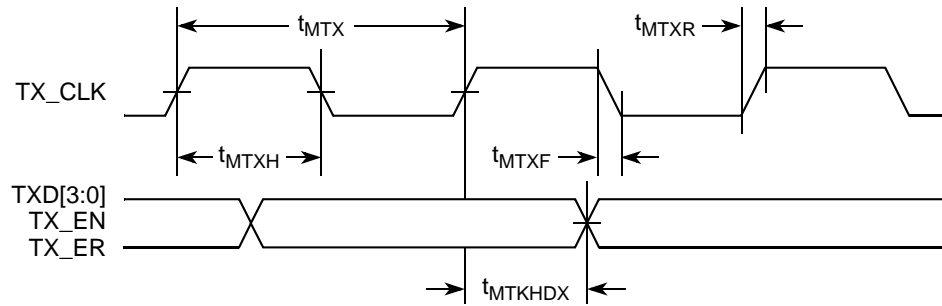


Figure 11. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}^2	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}^2	1.0	—	4.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

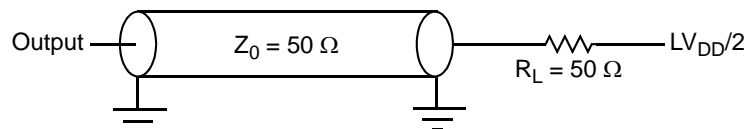


Figure 12. eTSEC AC Test Load

components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 66. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	800	800	ps	±100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 53](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	400	400	ps	±100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 53](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

19 Package Description

This section details package parameters, pin assignments, and dimensions.

19.1 Package Parameters

The package parameters for both the HiCTE FC-CBGA and FC-PBGA are provided in [Table 70](#).

Table 70. Package Parameters

Parameter	CBGA ¹	PBGA ²
Package outline	29 mm × 29 mm	29 mm × 29 mm
Interconnects	783	783
Ball pitch	1 mm	1 mm
Ball diameter (typical)	0.6 mm	0.6 mm
Solder ball	63% Sn 37% Pb 0% Ag	63% Sn 37% Pb 0% Ag
Solder ball (lead-free)	95% Sn 4.5% Ag 0.5% Cu	96.5% Sn 3.5% Ag

Notes:

1. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
2. The FC-PBGA package is available on only versions 2.1.1 and 2.1.2, and 3.0 of the device.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2.5 V, 3.3 V)	TV _{DD}	—
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV _{DD}	—
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	—
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	—
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV _{DD}	—
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV _{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V _{DD}	13

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	O	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV _{DD}	5, 7, 9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV _{DD}	—
$\overline{\text{LCS5/DMA_DREQ2}}$	D23	I/O	BV _{DD}	1
$\overline{\text{LCS6/DMA_DACK2}}$	G20	O	BV _{DD}	1
$\overline{\text{LCS7/DMA_DDONE2}}$	E21	O	BV _{DD}	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV _{DD}	5, 9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV _{DD}	5, 9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV _{DD}	5, 9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV _{DD}	5, 9
LALE	H24	O	BV _{DD}	5, 8, 9
LBCTL	G27	O	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV _{DD}	5, 9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV _{DD}	5, 9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV _{DD}	5, 8, 9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV _{DD}	5, 9
LGPL4/ $\overline{\text{LGTA/LUPWAIT/LPBSE}}$	H23	I/O	BV _{DD}	—
LGPL5	E26	O	BV _{DD}	5, 9
LCKE	E24	O	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
$\overline{\text{DMA_DACK}}[0:1]$	AD3, AE1	O	OV _{DD}	5, 9, 106
$\overline{\text{DMA_DREQ}}[0:1]$	AD4, AE2	I	OV _{DD}	—
$\overline{\text{DMA_DDONE}}[0:1]$	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_TX[0:3]	M23, N21, P23, R21	O	XV _{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	—
SD_REF_CLK	T27	I	XV _{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
HRESET	AG17	I	OV _{DD}	—
HRESET_REQ	AG16	O	OV _{DD}	29
SRESET	AG20	I	OV _{DD}	—
CKSTP_IN	AA9	I	OV _{DD}	—
CKSTP_OUT	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11
Clock				
RTC	AF16	I	OV _{DD}	—
SYSCLK	AH17	I	OV _{DD}	—
JTAG				
TCK	AG28	I	OV _{DD}	—
TDI	AH28	I	OV _{DD}	12

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for [Table 71](#). See [Table 71](#) for the meanings of these notes.

[Table 74](#) provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for [Table 71](#). See [Table 71](#) for the meanings of these notes.

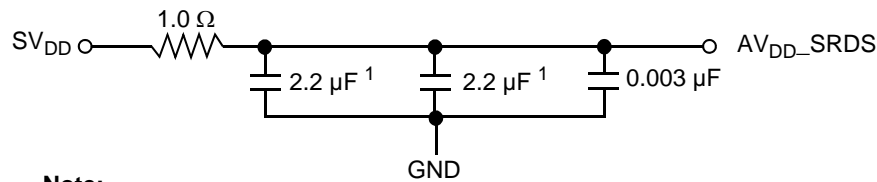
Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 32-Bit)				
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	—	—	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	O	OV _{DD}	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV _{DD}	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
Reserved	AF15, AD14, AE15, AD15	—	—	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
Reserved	W15	—	—	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PCI1_TRDY}}$	AG11	I/O	OV_{DD}	2
$\text{PCI1_REQ}[4:1]$	AH2, AG4, AG3, AH4	I	OV_{DD}	—
$\overline{\text{PCI1_REQ0}}$	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
$\overline{\text{PCI1_DEVSEL}}$	AH11	I/O	OV_{DD}	2
$\overline{\text{PCI1_FRAME}}$	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
cfg_pci1_width	AF14	I/O	OV_{DD}	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
$\overline{\text{MDQS}}[0:8]$	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



Note:

1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- $AV_{DD-SRDS}$ must be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 μF . Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD_TX}}$ [7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}$ [7:0]
- SD_REF_CLK
- $\overline{\text{SD_REF_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin `cfg_srds_en` on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD_TX}}$ [7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD_RX}}$ [7:0]
- SD_REF_CLK

23.2 Part Marking

Parts are marked as the example shown in [Figure 64](#).



Notes:

TWLYWW is final test traceability code.

MMMMM is 5 digit mask number.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device

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