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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547evjaujd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four controllers designed to comply with IEEE Std. 802.3[®], 802.3^u, 802.3^x, 802.3^z, 802.3^{ac}, and 802.3^{ab}
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2[™], PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	^t ciskew	-300 -365 -390	300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ± (T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.







Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII 1	Transmit AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSEC <i>n</i> _TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the device.

10.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3 \text{ V DC}$.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($V_{IN}^{1} = 0 V \text{ or } V_{IN} = BV_{DD}$)	I _{IN}	_	±5	μΑ
High-level output voltage ($BV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V
Low-level output voltage ($BV_{DD} = min$, $I_{OL} = 2 mA$)	V _{OL}	_	0.4	V

Table 38. Local Bus DC Electrical Characteristics (3.3 V DC)

Note:

1. Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 39 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5 \text{ V DC}$.

Table 39. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = BV_{DD})$	I _{IH}	—	10	μA
	IIL		-15	
High-level output voltage ($BV_{DD} = min, I_{OH} = -1 mA$)	V _{OH}	2.0	—	V
Low-level output voltage ($BV_{DD} = min$, $I_{OL} = 1 mA$)	V _{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Local Bus



Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).

JTAG

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.







Figure 32. Boundary-Scan Timing Diagram

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	Ι _{ΙΗ}	_	10	μΑ

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$ in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	2
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.

2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCIn_CLK when it is configured for asynchronous mode.

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
V _{TX-DIFFp-p}	Differential peak-to-peak output voltage	0.8	_	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
V _{TX-DE-RATIO}	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T _{TX-EYE}	Minimum TX eye width	0.70	_	_	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
T _{TX-EYE-MEDIAN-to-} MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median.	_	_	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
T _{TX-RISE} , T _{TX-FALL}	D+/D-TX output rise/fall time	0.125	_	—	UI	See Notes 2 and 5.
V _{TX-CM-ACp}	RMS AC peak common mode output voltage	_	_	20	mV	$\begin{split} & V_{TX\text{-}CM\text{-}ACp} = RMS(V_{TXD+} + V_{TXD-} /2 - V_{TX\text{-}CM\text{-}DC}) \\ & V_{TX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } V_{TX\text{-}D+} + V_{TX\text{-}D-} /2. \\ & See Note 2. \end{split}$
V _{TX-CM-DC-ACTIVE-} IDLE-DELTA	Absolute delta of dc common mode voltage during L0 and electrical idle	0	_	100	mV	$\begin{split} V_{TX-CM-DC} & (during \ L0) + V_{TX-CM-Idle-DC} & (during \\ electrical \ idle) &\leq 100 \ mV \\ V_{TX-CM-DC} &= DC_{(avg)} \ of \ V_{TX-D+} + V_{TX-D-} /2 \ [L0] \\ V_{TX-CM-Idle-DC} &= DC_{(avg)} \ of \ V_{TX-D+} + V_{TX-D-} /2 \\ [electrical \ idle] \\ See \ Note \ 2. \end{split}$
VTX-CM-DC-LINE-DELTA	Absolute delta of DC common mode between D+ and D–	0		25	mV	$\begin{split} V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} &\leq 25 \text{ mV} \\ V_{TX-CM-DC-D+} &= DC_{(avg)} \text{ of } V_{TX-D+} \\ V_{TX-CM-DC-D-} &= DC_{(avg)} \text{ of } V_{TX-D-} . \\ \text{See Note 2.} \end{split}$
V _{TX} -IDLE-DIFFp	Electrical idle differential peak output voltage	0	_	20	mV	$\begin{split} & V_{\text{TX-IDLE-DIFFp}} = V_{\text{TX-IDLE-D+}} - V_{\text{TX-IDLE-D-}} \\ & \leq 20 \text{ mV.} \\ & \text{See Note 2.} \end{split}$
V _{TX-RCV-DETECT}	The amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

Symbol	Parameter	Min	Nom	Max	Unit	Comments
T _{crosslink}	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.

- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in Figure 48.)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 50 for both V_{TX-D+} and V_{TX-D-}.
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
- 8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 48 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

PCI Express



Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
V _{RX-DIFFp-p}	Differential peak-to-peak input voltage	0.175	_	1.200	V	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $. See Note 2.
T _{RX-EYE}	Minimum receiver eye width	0.4	_	_	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
T _{RX-EYE-MEDIAN-to-} MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median	_	_	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

Table 57. Differential Receiver (RX) Input Specifications

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

19.3 Pinout Listings

NOTE

The DMA_DACK[0:1] and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on PCI1_AD[63:32]/PC2_AD[31:0] pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2

Table 71. MPC8548E Pinout Listing

Package Description

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
25. These are test signals for factory use only and must be pulled up (100 Ω -1 k Ω) to OV _{DD} for normal machine operation.			ation.	
26.Independent supplies derived from	26.Independent supplies derived from board V _{DD} .			
27.Recommend a pull-up resistor (~1	$k\Omega$) be placed on this pin to OV _{DD} .			
29. The following pins must NOT be p HRESET_REQ, TRIG_OUT/READ	29. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], TSEC4_TXD3/TSEC3_TXD7, HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP.			
30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.				
31. This pin is only an output in eTSE	C3 FIFO mode when used as Rx flow control.			
32. These pins must be connected to 2	XV _{DD} .			
33.TSEC2_TXD1, TSEC2_TX_ER an HRESET assertion.	e multiplexed as cfg_dram_type[0:1]. They must	be valid at powe	r-up, even befo	ore
34. These pins must be pulled to group	nd through a 300- Ω (±10%) resistor.			
35.When a PCI block is disabled, eith down to select external arbiter if the connect' or terminated through 2–1 connected to any other PCI device. POR config pins—irrespective of w any other PCI device connected or	er the POR config pin that selects between interrere is any other PCI device connected on the PCI $0 \ k\Omega$ pull-up resistors with the default of internal. The PCI block drives the PCI <i>n_</i> AD pins if it is context. The block drives the DEVDISR register or the bus.	hal and external a l bus, or leave th arbiter if the PCI nfigured to be th not. It may caus	arbiter must be e PCI <i>n_</i> AD pir <i>n_</i> AD pins are e PCI arbiter— e contention if	e pulled ns as 'no not through there is
36.MDIC0 is grounded through an 18. 1% resistor. These pins are used for	2- Ω precision 1% resistor and MDIC1 is connected or automatic calibration of the DDR IOs.	ed to GV _{DD} throu	gh an 18.2-Ω p	recision
38. These pins must be left floating.				
39. If PCI1 or PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK or PCI2_CLK. Otherwise the processor will not boot up.				I2_CLK.
40.These pins must be connected to GND.				
101.This pin requires an external 4.7-	101. This pin requires an external 4.7-k Ω resistor to GND.			
102.For Rev. 2.x silicon, DMA_DACK POR configuration are don't care.	[0:1] must be 0b11 during POR configuration; for	rev. 1.x silicon, t	he pin values o	during
103.If these pins are not used as GPI $2-10 \text{ k}\Omega$ resistors.	Nn (general-purpose input), they must be pulled	low (to GND) or	high (to LV _{DD})	through
104.These must be pulled low to GNE	D through 2–10 k Ω resistors if they are not used.			
105.These must be pulled low or high	to LV_{DD} through 2–10 k Ω resistors if they are no	ot used.		
106.For rev. 2.x silicon, DMA_DACK[0 configuration are don't care.):1] must be 0b10 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR
107.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	107.For rev. 2.x silicon, DMA_DACK[0:1] must be 0b01 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.			ng POR
108.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	108.For rev. 2.x silicon, DMA_DACK[0:1] must be 0b11 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.			ng POR
109. This is a test signal for factory us	109. This is a test signal for factory use only and must be pulled down (100 Ω – 1 k Ω) to GND for normal machine operation.			eration.
111. If these pins are not used as GPI	Nn (general-purpose input), they must be pulled I	ow (to GND) or h	nigh (to OV _{DD})	through
2-10 K22 HESISIUIS.	during DOP configuration			
112. This pin must not be pulled down during POK configuration.				
	$\int \int \nabla \nabla D = \int \nabla \nabla \nabla \nabla D = \int \nabla \nabla \nabla \nabla \nabla D = \int \nabla \nabla$			

Table 72.	MPC8547E	Pinout Listing	(continued)
		i mout Listing	(continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
	DFT				
L1_TSTCLK	AC25	I	OV _{DD}	25	
L2_TSTCLK	AE22	I	OV _{DD}	25	
LSSD_MODE	AH20	I	OV _{DD}	25	
TEST_SEL	AH14	I	OV _{DD}	25	
	Thermal Management				
THERMO	AG1			14	
THERM1	AH1			14	
	Power Management				
ASLEEP	AH18	0	OV_{DD}	9, 19, 29	
	Power and Ground Signals				
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 	_	_	_	
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}		
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—	
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_	
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}		

Package Description

Signal	Pin Type	Power Supply	Notes		
UDE	AH16	I	OV _{DD}	—	
MCP	AG19	I	OV _{DD}	—	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	_	
IRQ[8]	AF19	I	OV _{DD}	—	
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1	
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1	
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1	
IRQ_OUT	AD18	0	OV _{DD}	2, 4	
	Ethernet Management Interface				
EC_MDC	AB9	0	OV _{DD}	5, 9	
EC_MDIO	AC8	I/O	OV _{DD}	—	
	Gigabit Reference Clock		•	•	
EC_GTX_CLK125	V11	I	LV _{DD}	—	
Tł	Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9	
TSEC1_COL	R4	I	LV _{DD}	—	
TSEC1_CRS	V5	I/O	LV _{DD}	20	
TSEC1_GTX_CLK	U7	0	LV _{DD}	—	
TSEC1_RX_CLK	U3	I	LV _{DD}	—	
TSEC1_RX_DV	V2	I	LV _{DD}	—	
TSEC1_RX_ER	T1	I	LV _{DD}	—	
TSEC1_TX_CLK	Т6	I	LV _{DD}	—	
TSEC1_TX_EN	U9	0	LV _{DD}	30	
TSEC1_TX_ER	Τ7	0	LV _{DD}	—	
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103	
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—	
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9	
GPOUT7	N6	0	LV _{DD}	-	
Reserved	P1	_	—	104	
Reserved	R6	_	—	104	
Reserved	P6	_	-	15	
Reserved	N4			105	

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27	
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27	
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27	
	SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	—	
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—	
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—	
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—	
SD_PLL_TPD	U28	0	XV _{DD}	24	
SD_REF_CLK	T28	I	XV _{DD}	—	
SD_REF_CLK	T27	I	XV _{DD}	—	
Reserved	AC1, AC3	—	—	2	
Reserved	M26, V28	—	_	32	
Reserved	M25, V27	_	_	34	
Reserved	M20, M21, T22, T23	—	—	38	
	General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—	
System Control					
HRESET	AG17	I	OV _{DD}	—	
HRESET_REQ	AG16	0	OV _{DD}	29	
SRESET	AG20	I	OV _{DD}	—	
CKSTP_IN	AA9	I	OV _{DD}	—	
CKSTP_OUT	AA8	0	OV _{DD}	2, 4	
	Debug				
TRIG_IN	AB2	I	OV _{DD}	—	
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29	
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9	
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29	
MDVAL	AE5	0	OV _{DD}	6	
CLK_OUT	AE21	0	OV _{DD}	11	
	Clock				
RTC	AF16	I	OV _{DD}		
SYSCLK	AH17		OV _{DD}		

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV_{DD} , OV_{DD} , GV_{DD} , DV_{DD} , DV

These capacitors must have a value of 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

System Design Information



Notes:

- 1. The COP port and target board must be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
- 2. Populate this with a 10– Ω resistor for short-circuit/current-limiting protection.
- 3. The KEY location (pin 14) is not physically present on the COP header.
- 4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
- This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch must be closed to position B.
- 6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 63. JTAG Interface Connection

System Design Information

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD}}_{\text{TX}}[7:0]$
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- <u>SD_RX</u>[7:0]
- SD_REF_CLK
- SD_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = $0xE_0F08$) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- <u>SD_TX</u>[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD}_{RX}}[7:0]$
- SD_REF_CLK

Rev. Number	Date	Substantive Change(s)
2	04/2008	 Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit.") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	 Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." Added Section 4.4, "PCI/PCL-X Reference Clock Timing." Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 29, "GMII, MII, RMII, and TBI DC Electrical Characteristics." Corrected V_{IL}(max) in Table 22, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. Corrected V_{IH}(min) in Table 36, "MII Management DC Electrical Characteristics." Corrected V_{IH}(min) in Table 37, "MII Management AC Timing Specifications." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKH2}, t_{LBIXKH1}, and t_{LBIXKH2} in Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled" and Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKL2}, t_{LBIXKH1}, and t_{LBIXKL2} in Table 42, "Local Bus Timing Parameters —PLL Bypassed." Note that t_{LBIVKL2} and t_{LBIXKL2} in Table 42, "Local Bus Signals (PLL Bypass Mode)." Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." Added LOPWAIT assertion in Figure 26, Figure 27 and Figure 28. Carrified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" Added LOP
0	07/2007	Initial Release

Table 88. Document Revision History (continued)