

Welcome to E-XFL.COM

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8547evtaqgb

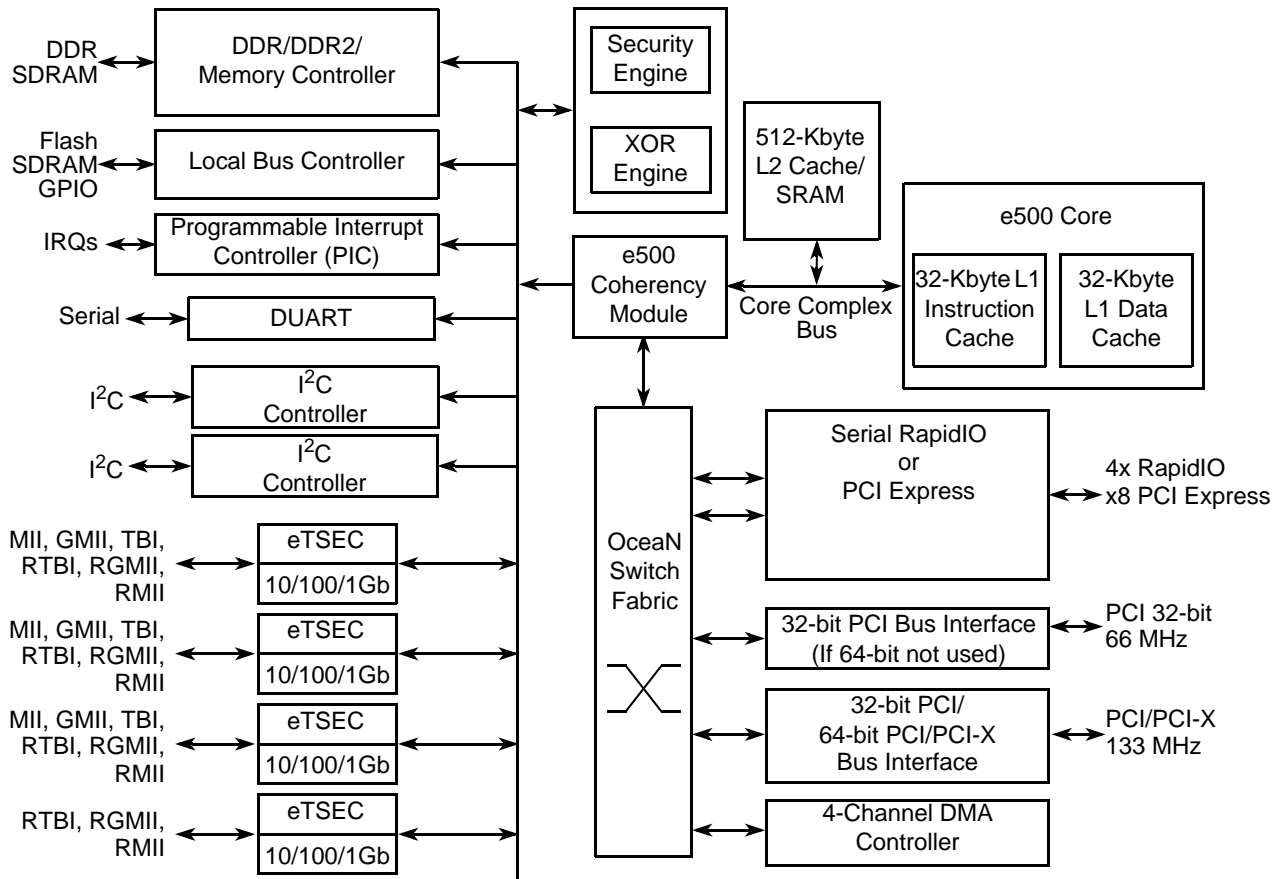


Figure 1. Device Block Diagram

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
 - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
 - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
 - 36-bit real addressing
 - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
 - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
 - Enhanced hardware and software debug support

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the device. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	-0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	-0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	-0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	2
Three-speed Ethernet I/O voltage		LV_{DD} (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	3
		TV_{DD} (for eTSEC3 and eTSEC4)	-0.3 to 3.63 -0.3 to 2.75		
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	-0.3 to 3.63 -0.3 to 2.75	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	4
	DDR/DDR2 DRAM reference	MV_{REF}	-0.3 to ($GV_{DD}/2 + 0.3$)	V	—
	Three-speed Ethernet I/O signals	LV_{IN} TV_{IN}	-0.3 to ($LV_{DD} + 0.3$) -0.3 to ($TV_{DD} + 0.3$)	V	4
	Local bus signals	BV_{IN}	-0.3 to ($BV_{DD} + 0.3$)	—	—
	DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	4
	PCI/PCI-X	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	4

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	$BV_{DD} = 3.3\text{ V}$	1
	25	$BV_{DD} = 2.5\text{ V}$	
PCI signals	45(default)	$BV_{DD} = 3.3\text{ V}$	2
	45(default)	$BV_{DD} = 2.5\text{ V}$	
DDR signal	25	$OV_{DD} = 3.3\text{ V}$	3
	45(default)		
DDR2 signal	18	$GV_{DD} = 2.5\text{ V}$	3
	36 (half strength mode)		
TSEC/10/100 signals	18	$GV_{DD} = 1.8\text{ V}$	3
	36 (half strength mode)		
TSEC/10/100 signals	45	$L/TV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, JTAG	45	$OV_{DD} = 3.3\text{ V}$	—
I2C	150	$OV_{DD} = 3.3\text{ V}$	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.
3. The drive strength of the DDR interface in half-strength mode is at $T_j = 105^\circ\text{C}$ and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

1. V_{DD} , AV_{DD-n} , BV_{DD} , LV_{DD} , OV_{DD} , SV_{DD} , TV_{DD} , XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

A summary of the FIFO AC specifications appears in [Table 24](#) and [Table 25](#).

Table 24. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See [Section 4.5, “Platform to FIFO Restrictions.”](#)

Timing diagrams for FIFO appear in [Figure 6](#) and [Figure 7](#).

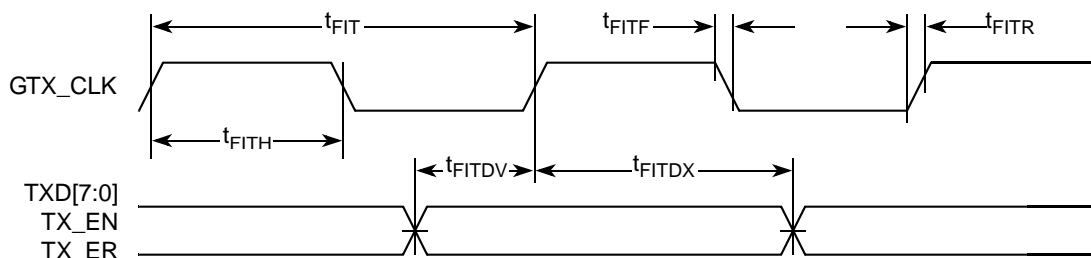


Figure 6. FIFO Transmit AC Timing Diagram

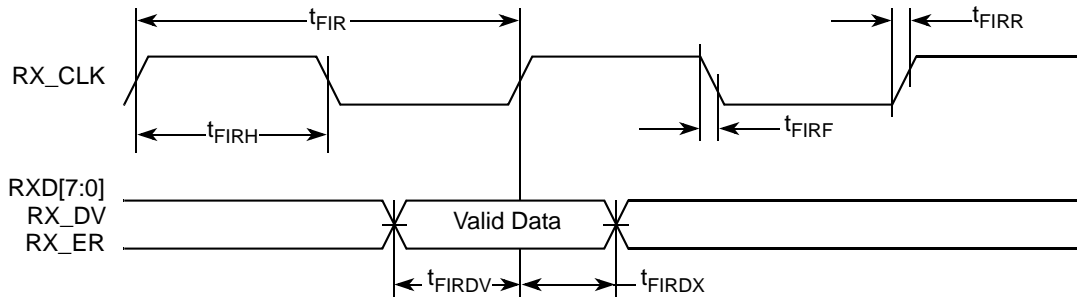


Figure 7. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t _{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%–80%)	t _{GTXR} ²	—	—	1.0	ns
GTX_CLK data clock fall time (80%–20%)	t _{GTXF} ²	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 11 shows the MII transmit AC timing diagram.

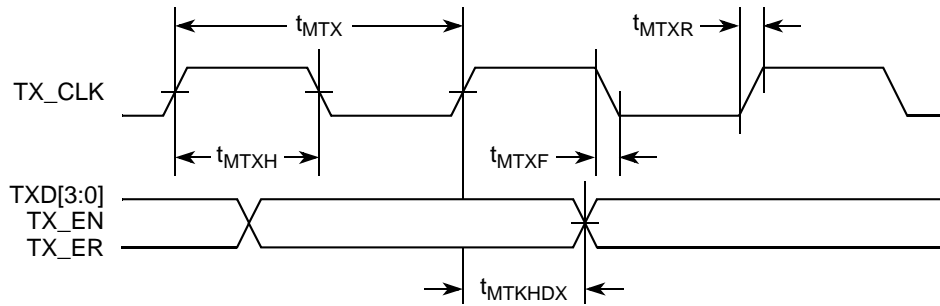


Figure 11. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}^2	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}^2	1.0	—	4.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

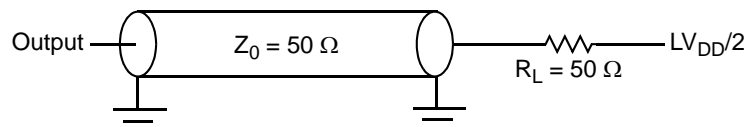


Figure 12. eTSEC AC Test Load

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.

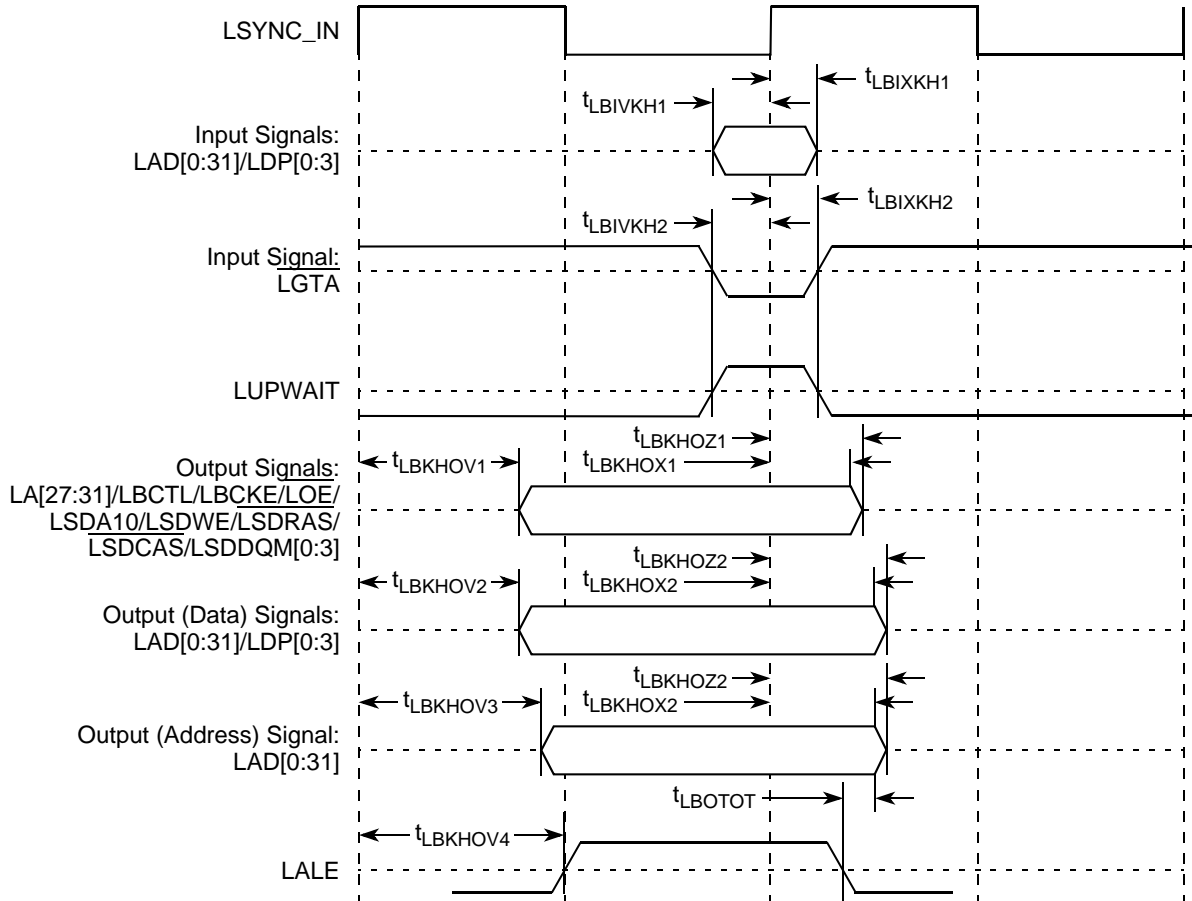


Figure 23. Local Bus Signals (PLL Enabled)

This table describes the timing parameters of the local bus interface at $V_{DD} = 3.3\text{ V}$ with PLL disabled.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHK}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{LGTA}/\overline{LUPWAIT}$)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{LGTA}/\overline{LUPWAIT}$ input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{LGTA}/\overline{LUPWAIT}$)	$t_{LBIXKH1}$	-1.8	—	ns	4, 5

Local Bus

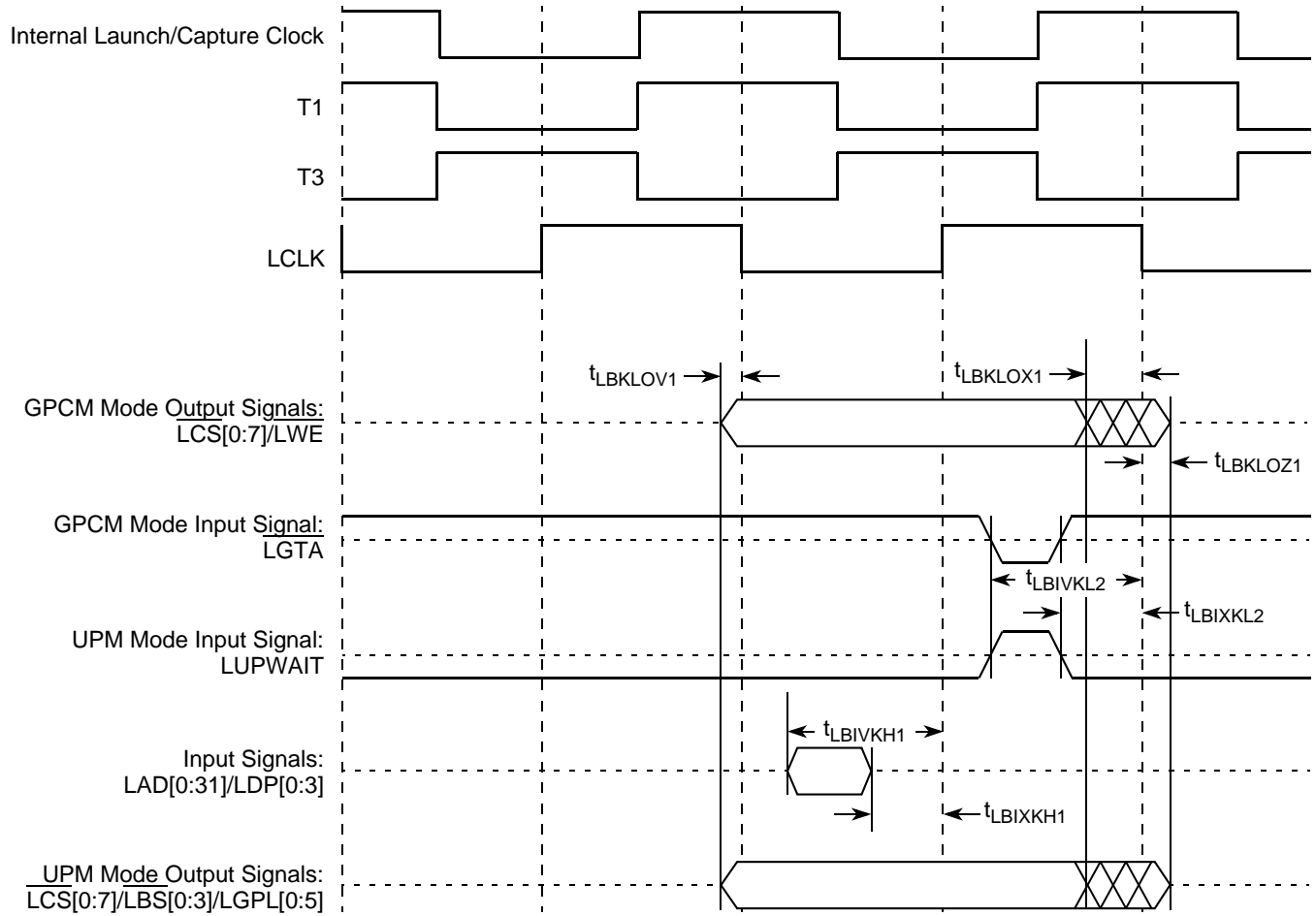


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD_TX}} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.

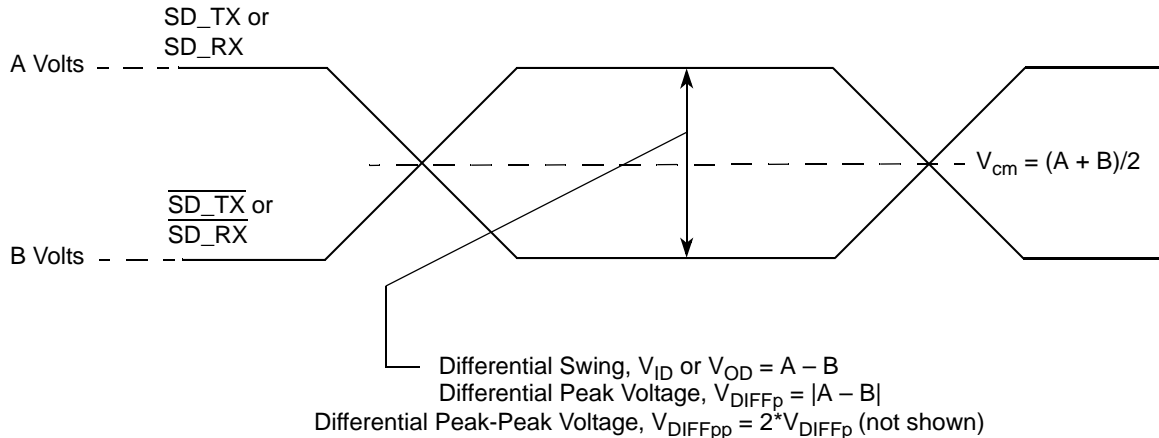


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and \overline{TD} , has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFpp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{SD_REF_CLK}$ for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

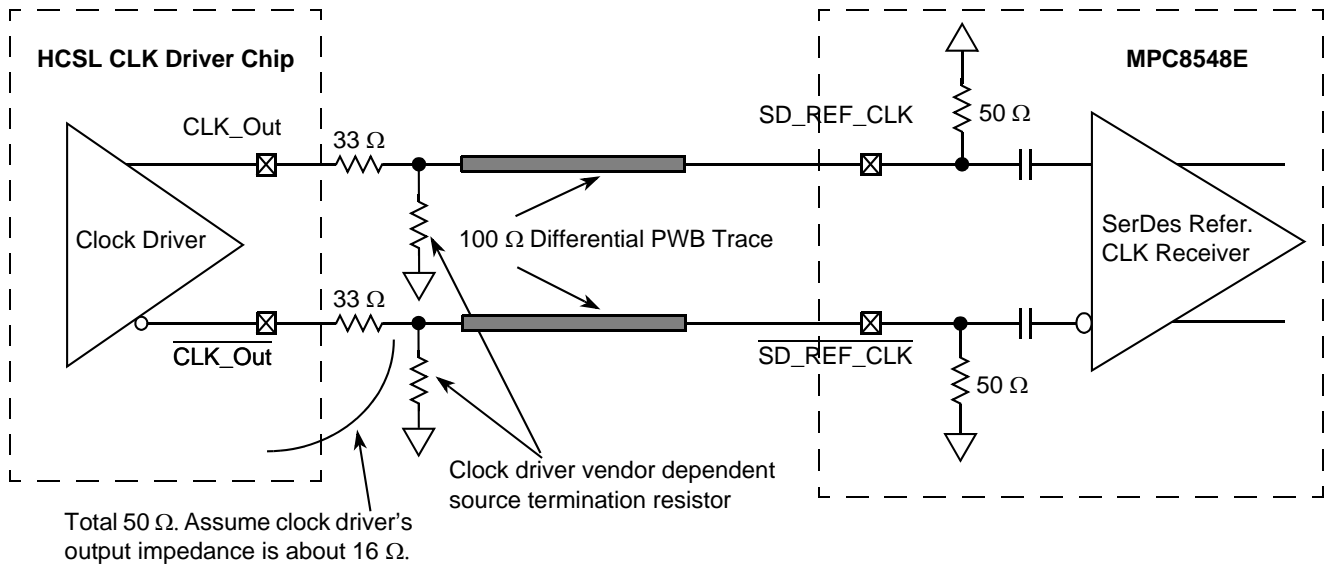


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

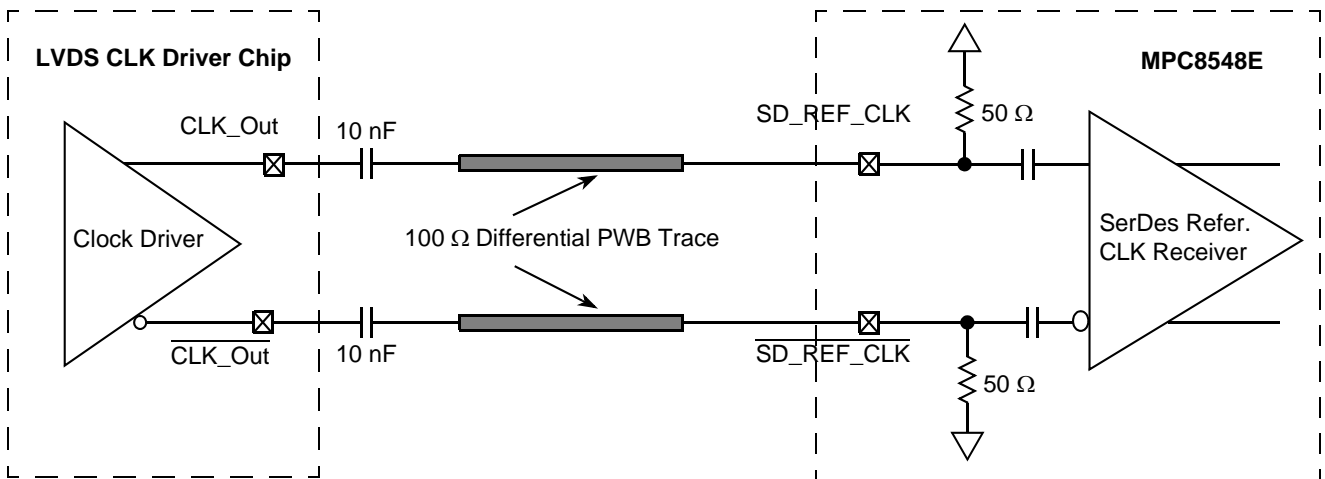


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} + V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$ V_{TX-CM-DC}(\text{during L0}) + V_{TX-CM-Idle-DC}(\text{during electrical idle}) \leq 100$ mV $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [L0] $V_{TX-CM-Idle-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D-	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = \text{DC}_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = \text{DC}_{(avg)}$ of $ V_{TX-D-} $. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

19.3 Pinout Listings

NOTE

The $\overline{\text{DMA_DACK}}[0:1]$ and $\overline{\text{TEST_SEL}}/\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details.

For MPC8548/47/45, GPIOs are still available on $\text{PCI1_AD}[63:32]/\text{PC2_AD}[31:0]$ pins if they are not used for PCI functionality.

For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 71 provides the pinout listing for the MPC8548E 783 FC-PBGA package.

Table 71. MPC8548E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
$\text{PCI1_AD}[63:32]/\text{PCI2_AD}[31:0]$	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
$\text{PCI1_AD}[31:0]$	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[7:4]/\text{PCI2_C_}\overline{\text{BE}}[3:0]$	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
$\text{PCI1_C_}\overline{\text{BE}}[3:0]$	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
$\text{PCI1_PAR}64/\text{PCI2_PAR}$	W15	I/O	OV_{DD}	
$\overline{\text{PCI1_GNT}}[4:1]$	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1_GNT}}0$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1_TRDY}}$	AG11	I/O	OV_{DD}	2

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
I²C interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	—
$\overline{\text{SD_RX}}[0:7]$	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV _{DD}	—
$\overline{\text{SD_TX}}[0:7]$	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV _{DD}	—
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	3
$\overline{\text{SD_REF_CLK}}$	T27	I	XV _{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV _{DD}	—
$\overline{\text{HRESET_REQ}}$	AG16	O	OV _{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV _{DD}	—
$\overline{\text{CKSTP_IN}}$	AA9	I	OV _{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2

Table 80. Memory Bus Clocking Specifications (MPC8543E)

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000 MHz			
	Min	Max		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See [Section 20.2, "CCB/SYSCLK PLL Ratio,"](#) and [Section 20.3, "e500 Core PLL Ratio,"](#) for ratio settings.
- The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

20.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in [Table 81](#):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, see the *PCI 2.2 Specification*.

Table 81. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	20:1
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

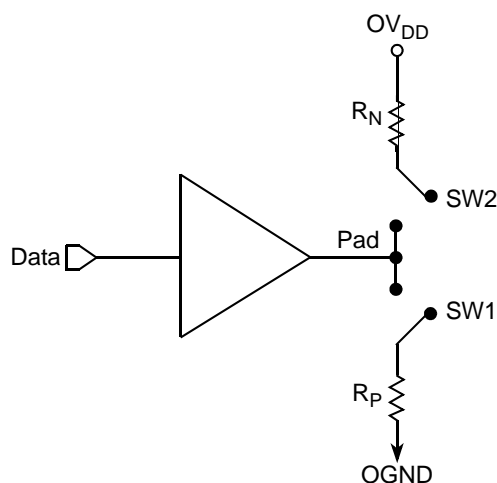


Figure 61. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 86. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1, $T_j = 105^\circ\text{C}$.

22.8 Configuration Pin Muxing

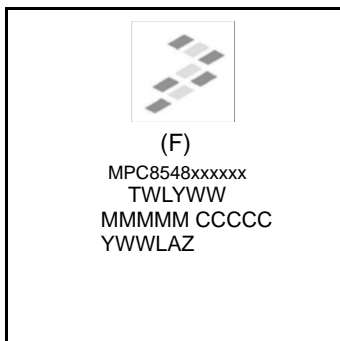
The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value must permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor minimizes the disruption of signal quality or speed for output pins thus configured.

23.2 Part Marking

Parts are marked as the example shown in [Figure 64](#).



Notes:

TWLYYWW is final test traceability code.

MMMMM is 5 digit mask number.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	<ul style="list-style-type: none"> Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. Removed Note from Section 5.1, "Power-On Ramp Rate". Changed the Table 10 title to "Power Supply Ramp Rate". Removed table 11. Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)"¹ from 4 and 25 to 2 and 10 respectively .
8	04/2011	<ul style="list-style-type: none"> Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	<ul style="list-style-type: none"> In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	<ul style="list-style-type: none"> In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. In Table 13 deleted ramp rate requirement for XVDD/SVDD. In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	<ul style="list-style-type: none"> In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." Added a reference to Revision 2.1.2. Updated Table 55, "MII Management AC Timing Specifications." Added Section 5.1, "Power-On Ramp Rate."

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	04/2009	<ul style="list-style-type: none"> In Table 1, “Absolute Maximum Ratings ¹,” and in Table 2, “Recommended Operating Conditions,” moved text, “MII management voltage” from LV_{DD}/TV_{DD} to OV_{DD}, added “Ethernet management” to OV_{DD} row of input voltage section. In Table 5, “SYSCLK AC Timing Specifications,” added notes 7 and 8 to SYSCLK frequency and cycle time. In Table 36, “MII Management DC Electrical Characteristics,” changed all instances of LV_{DD}/OV_{DD} to OV_{DD}. Modified Section 16, “High-Speed Serial Interfaces (HSSI),” to reflect that there is only one SerDes. Modified DDR clk rate min from 133 to 166 MHz. Modified note in Table 75, “Processor Core Clocking Specifications (MPC8548E and MPC8547E), “. ” In Table 56, “Differential Transmitter (TX) Output Specifications,” modified equations in Comments column, and changed all instances of “LO” to “L0.” Also added note 8. In Table 57, “Differential Receiver (RX) Input Specifications,” modified equations in Comments column, and in note 3, changed “TRX-EYE-MEDIAN-to-MAX-JITTER,” to “TRX-EYE-MEDIAN-to-MAX-JITTER.” Modified Table 83, “Frequency Options of SYSCLK with Respect to Memory Bus Speeds.” Added a note on Section 4.1, “System Clock Timing,” to limit the SYSCLK to 100 MHz if the core frequency is less than 1200 MHz In Table 71, “MPC8548E Pinout Listing”Table 72, “MPC8547E Pinout Listing”Table 73, “MPC8545E Pinout Listing”Table 74, “MPC8543E Pinout Listing,” added note 5 to LA[28:31]. Added note to Table 83, “Frequency Options of SYSCLK with Respect to Memory Bus Speeds.”
3	01/2009	<ul style="list-style-type: none"> [Section 4.6, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.” Changed minimum frequency equation to be 527 MHz for PCI x8. In Table 5, added note 7. Section 4.5, “Platform to FIFO Restrictions.” Changed platform clock frequency to 4.2. Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” Added MII after GMII and add ‘or 2.5 V’ after 3.3 V. In Table 23, modified table title to include GMII, MII, RMII, and TBI. In Table 24 and Table 25, changed clock period minimum to 5.3. In Table 25, added a note. In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title. In Table 30 and Figure 15, changed all instances of PMA to TSEC_n. In Section 8.2.5, “TBI Single-Clock Mode AC Specifications.” Replaced first paragraph. In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC_n_TX_CLK. In Table 36, changed all instances of OV_{DD} to LV_{DD}/TV_{DD}. In Table 37, “MII Management AC Timing Specifications,” changed MDC minimum clock pulse width high from 32 to 48 ns. Added new section, Section 16, “High-Speed Serial Interfaces (HSSI).” Section 16.1, “DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK.” Added new paragraph. Section 17.1, “DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK.” Added new paragraph. Added information to Figure 63, both in figure and in note. Section 22.3, “Decoupling Recommendations.” Modified the recommendation. Table 87, “Part Numbering Nomenclature.” In Silicon Version column added Ver. 2.1.2.