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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547hxatg

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2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	1
	45(default) 45(default)	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	
PCI signals	25	OV _{DD} = 3.3 V	2
	45(default)		
DDR signal	18 36 (half strength mode)	GV _{DD} = 2.5 V	3
DDR2 signal	18 36 (half strength mode)	GV _{DD} = 1.8 V	3
TSEC/10/100 signals	45	L/TV _{DD} = 2.5/3.3 V	
DUART, system control, JTAG	45	OV _{DD} = 3.3 V	—
12C	150	OV _{DD} = 3.3 V	_

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.

3. The drive strength of the DDR interface in half-strength mode is at $T_i = 105^{\circ}C$ and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

- 1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
- 2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

DDR and DDR2 SDRAM

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8548E PowerQUICC III Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 3 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Enhanced Three-Speed Ethernet (eTSEC)

Figure 10 shows the GMII receive AC timing diagram.



Figure 10. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

fable 2	28.	MII	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX} ²	_	400	_	ns
TX_CLK clock period 100 Mbps	t _{MTX}		40	_	ns
TX_CLK duty cycle	t _{MTXH/} t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t _{MTXR} ²	1.0	_	4.0	ns
TX_CLK data clock fall (80%–20%)	t _{MTXF} ²	1.0		4.0	ns

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH/TRRX}	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}	_	_	250	ps
Rise time RX_CLK (20%–80%)	t _{TRRR}	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXKH}	1.0	_	_	ns

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	—	0.90	V
Input high current ($OV_{DD} = Max, V_{IN}^{1} = 2.1 V$)	I _{IH}	—	40	μA
Input low current ($OV_{DD} = Max, V_{IN} = 0.5 V$)	I _{IL}	-600	—	μΑ

Table 36. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t _{MDC}	120.5		1389	ns	—
MDC clock pulse width high	t _{MDCH}	32		—	ns	—
MDC to MDIO valid	t _{MDKHDV}	$16 \times t_{CCB}$		—	ns	5
MDC to MDIO delay	t _{MDKHDX}	(16 × t _{CCB} × 8) – 3		$(16 \times t_{\rm CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t _{MDDVKH}	5		—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0		—	ns	—
MDC rise time	t _{MDCR}	_	_	10	ns	4

10.2 Local Bus AC Electrical Specifications

This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.3	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}		2.5	ns	5

Table 40. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.



This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V with PLL disabled.

Table 42. Local Bus Timing	Parameters—PLL Bypassed
----------------------------	-------------------------

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	—	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t _{lbkhkt}	2.3	4.4	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	6.2	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.1	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	—	ns	4, 5

l²C

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the device.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interfaces.

Table 45. I²C DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7 \times OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	
Low level output voltage	V _{OL}	0	$0.2\times \text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	3
Capacitance for each I/O pin	CI		10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2. See the MPC8548E PowerQUICC[™] III Integrated Processor Family Reference Manual, for information on the digital filter used.
- 3. I/O pins obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 46. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Мах	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μS	4
High period of the SCL clock	t _{I2CH}	0.6	—	μS	4
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS	4
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs	4
Data setup time	t _{I2DVKH}	100	—	ns	4
Data input hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0		μS	2
Data output delay time:	t _{I2OVKL}	—	0.9	—	3
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS	

PCI/PCI-X

Table 54. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the PCI-X 1.0a Specification.

- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the PCI-X 1.0a Specification.

- 10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
- 11. Guaranteed by characterization.

12. Guaranteed by design.

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

18 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8548E, for the LP-Serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

18.1 <u>DC Requirements</u> for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

18.2 <u>AC Requirements</u> for Serial RapidIO SD_REF_CLK and SD_REF_CLK

Table 58 lists the Serial RapidIO SD_REF_CLK and SD_REF_CLK AC requirements.

Symbol	Parameter Description	Min	Тур	Max	Unit	Comments
t _{REF}	REFCLK cycle time	_	10(8)	_	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	80	ps	_
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-40	—	40	ps	_

Table 58. SD_REF_CLK and SD_REF_CLK AC Requirements

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Serial RapidIO

802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be $100-\Omega$ resistive $\pm 5\%$ differential to 2.5 GHz.

18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ± 5% differential to 2.5 GHz.

18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 18.7, "Receiver Specifications," and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 54 and Table 69. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 18.7, "Receiver Specifications," is then added to the signal and the test load is replaced by the receiver being tested.

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 (One 64-Bit or One 32-Bit)		1	
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	ļ	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
PCI1_REQ64	AF14	I/O	OV _{DD}	2, 5,10
PCI1_ACK64	V15	I/O	OV _{DD}	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25		—	2

Table 72. MPC8547E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27		
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27		
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27		
	SerDes					
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	—		
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—		
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—		
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—		
SD_PLL_TPD	U28	0	XV _{DD}	24		
SD_REF_CLK	T28	I	XV _{DD}	—		
SD_REF_CLK	T27	I	XV _{DD}	—		
Reserved	AC1, AC3	—	—	2		
Reserved	M26, V28	—	_	32		
Reserved	M25, V27	_	_	34		
Reserved	M20, M21, T22, T23	—	—	38		
	General-Purpose Output					
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—		
	System Control					
HRESET	AG17	I	OV _{DD}	—		
HRESET_REQ	AG16	0	OV _{DD}	29		
SRESET	AG20	I	OV _{DD}	—		
CKSTP_IN	AA9	I	OV _{DD}	—		
CKSTP_OUT	AA8	0	OV _{DD}	2, 4		
	Debug					
TRIG_IN	AB2	I	OV _{DD}	—		
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29		
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9		
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29		
MDVAL	AE5	0	OV _{DD}	6		
CLK_OUT	AE21	0	OV _{DD}	11		
Clock						
RTC	AF16	I	OV _{DD}			
SYSCLK	AH17		OV _{DD}			

Clocking

Characteristic	Maxim 800	num Process MHz	or Core Frequency 1000 MHz		Unit	Notes
	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	MHz	1, 2

Table 77. Processor Core Clocking Specifications (MPC8543E)

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 78. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)

	Maximum Process	Unit	Notes	
Characteristic	1000, 1200			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

Table 79. Memory Bus Clocking Specifications (MPC8545E)

	Maximum Process			
Characteristic	Characteristic 800, 1000, 1200 MHz		Unit	Notes
	Min	Мах		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

 Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

Table 82	. e500	Core t	o CCB	Clock Ratio
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20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	25	33.33	41.66	66.66	83	100	111	133.33
			ļ	Platform/C	CB Freque	ency (MHz)		
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500		-	
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533		-				
20	333	500		-					

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout

23 Ordering Information

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Ordering information for the parts fully covered by this specification document is provided in Section 23.1, "Part Numbers Fully Addressed by this Document."

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	t	pp	11	C	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8548E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 ³ AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 ⁵ G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)

Table 87. Part Numbering Nomenclature

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Rev. Number	Date	Substantive Change(s)
4	04/2009	 In Table 1, "Absolute Maximum Ratings ¹," and in Table 2, "Recommended Operating Conditions," moved text, "MII management voltage" from LV_{DD}/TV_{DD} to OV_{DD}, added "Ethernet management" to OVDD row of input voltage section. In Table 5, "SYSCLK AC Timing Specifications," added notes 7 and 8 to SYSCLK frequency and cycle
		 time. In Table 36, "MII Management DC Electrical Characteristics," changed all instances of LV_{DD}/OV_{DD} to OV_{DD}. Modified Section 16, "High-Speed Serial Interfaces (HSSI)," to reflect that there is only one SerDes. Modified DDR clk rate min from 133 to 166 MHz. Modified note in Table 75, "Processor Core Clocking Specifications (MPC8548E and MPC8547E), "." In Table 56, "Differential Transmitter (TX) Output Specifications," modified equations in Comments column, and changed all instances of "LO" to "LO." Also added note 8. In Table 57, "Differential Receiver (RX) Input Specifications," modified equations in Comments column, and in note 3, changed "TRX-EYE-MEDIAN-to-MAX-JITTER," to "T_{RX-EYE-MEDIAN-to-MAX-JITTER}." Modified Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds." Added a note on Section 4.1, "System Clock Timing," to limit the SYSCLK to 100 MHz if the core
		 frequency is less than 1200 MHz In Table 71, "MPC8548E Pinout ListingTable 72, "MPC8547E Pinout ListingTable 73, "MPC8545E Pinout ListingTable 74, "MPC8543E Pinout Listing," added note 5 to LA[28:31]. Added note to Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."
3	01/2009	 [Section 4.6, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." Changed minimum frequency equation to be 527 MHz for PCI x8. In Table 5, added note 7. Section 4.5, "Platform to FIFO Restrictions." Changed platform clock frequency to 4.2. Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." Added MII after GMII and add 'or 2.5 V' after 3.3 V. In Table 23, modified table title to include GMII, MII, RMII, and TBI. In Table 24 and Table 25, changed clock period minimum to 5.3. In Table 25, added a note
		 In Table 25, added a note. In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title. In Table 30 and Figure 15, changed all instances of PMA to TSEC<i>n</i>. In Section 8.2.5, "TBI Single-Clock Mode AC Specifications." Replaced first paragraph. In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC<i>n</i>_TX_CLK. In Table 36, changed all instances of OVpp to LVpp.
		 In Table 37, "MII Management AC Timing Specifications," changed MDC minimum clock pulse width high from 32 to 48 ns. Added new section, Section 16, "High-Speed Serial Interfaces (HSSI)." Section 16.1, "DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK." Added new paragraph. Section 17.1, "DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK." Added new paragraph. Added information to Figure 63, both in figure and in note. Section 22.3, "Decoupling Recommendations." Modified the recommendation.
		Table 87, "Part Numbering Nomenclature." In Silicon Version column added Ver. 2.1.2.

Table 88. Document Revision History (continued)