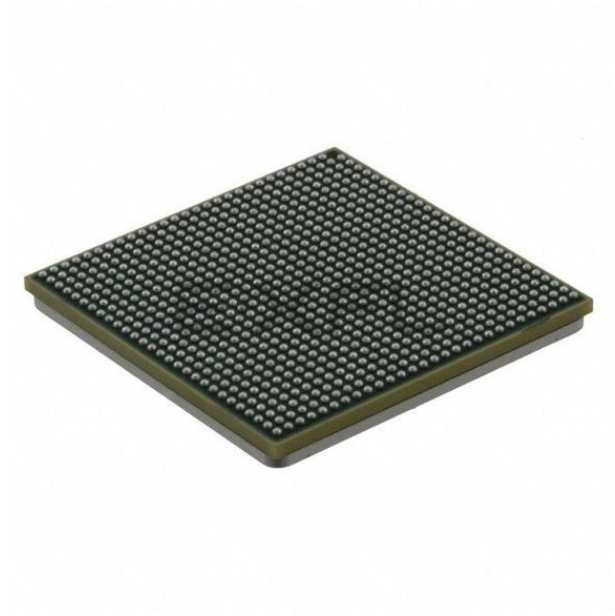

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547hxauj

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default)	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	45(default)		
DDR signal	18 36 (half strength mode)	GV_{DD} = 2.5 V	3
DDR2 signal	18 36 (half strength mode)	GV_{DD} = 1.8 V	3
TSEC/10/100 signals	45	L/TV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I2C	150	OV_{DD} = 3.3 V	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.
3. The drive strength of the DDR interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	μs
Local bus PLL lock time	—	50	μs
PCI/PCI-X bus PLL lock time	—	50	μs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.
2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, "PLL Power Supply Filtering," the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that GV_{DD}(typ) = 2.5 V for DDR SDRAM, and GV_{DD}(typ) = 1.8 V for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Figure 4 shows the DDR SDRAM output timing diagram.+

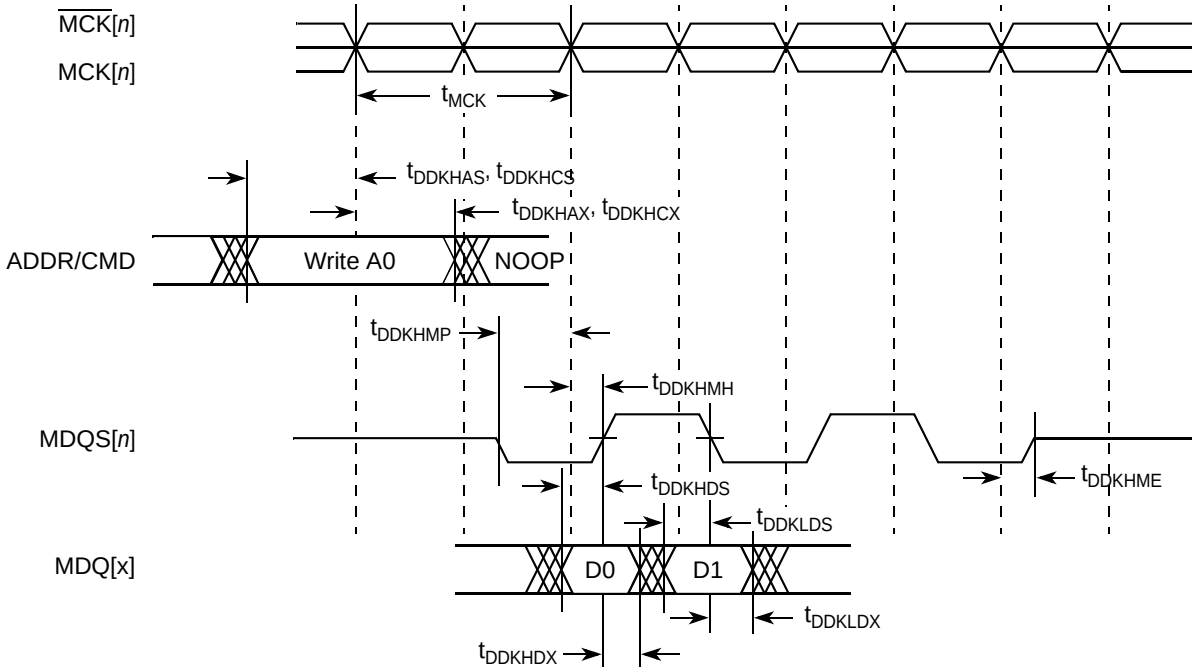

Figure 4. DDR SDRAM Output Timing Diagram

Figure 5 provides the AC test load for the DDR bus.

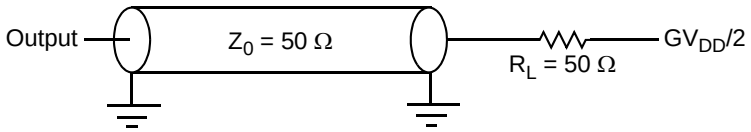

Figure 5. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:
1. Guaranteed by design.
2. f_{CCB} refers to the internal platform clock.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

Table 34. RMII Transmit AC Timing Specifications (continued)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 18 shows the RMII transmit AC timing diagram.

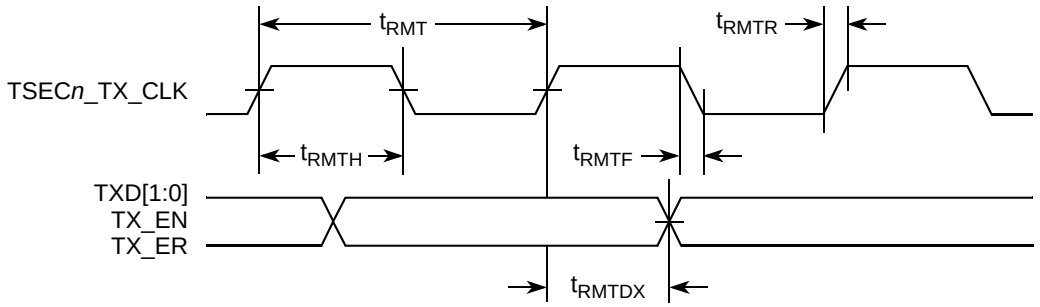

Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSEC*n*_TX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK(20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

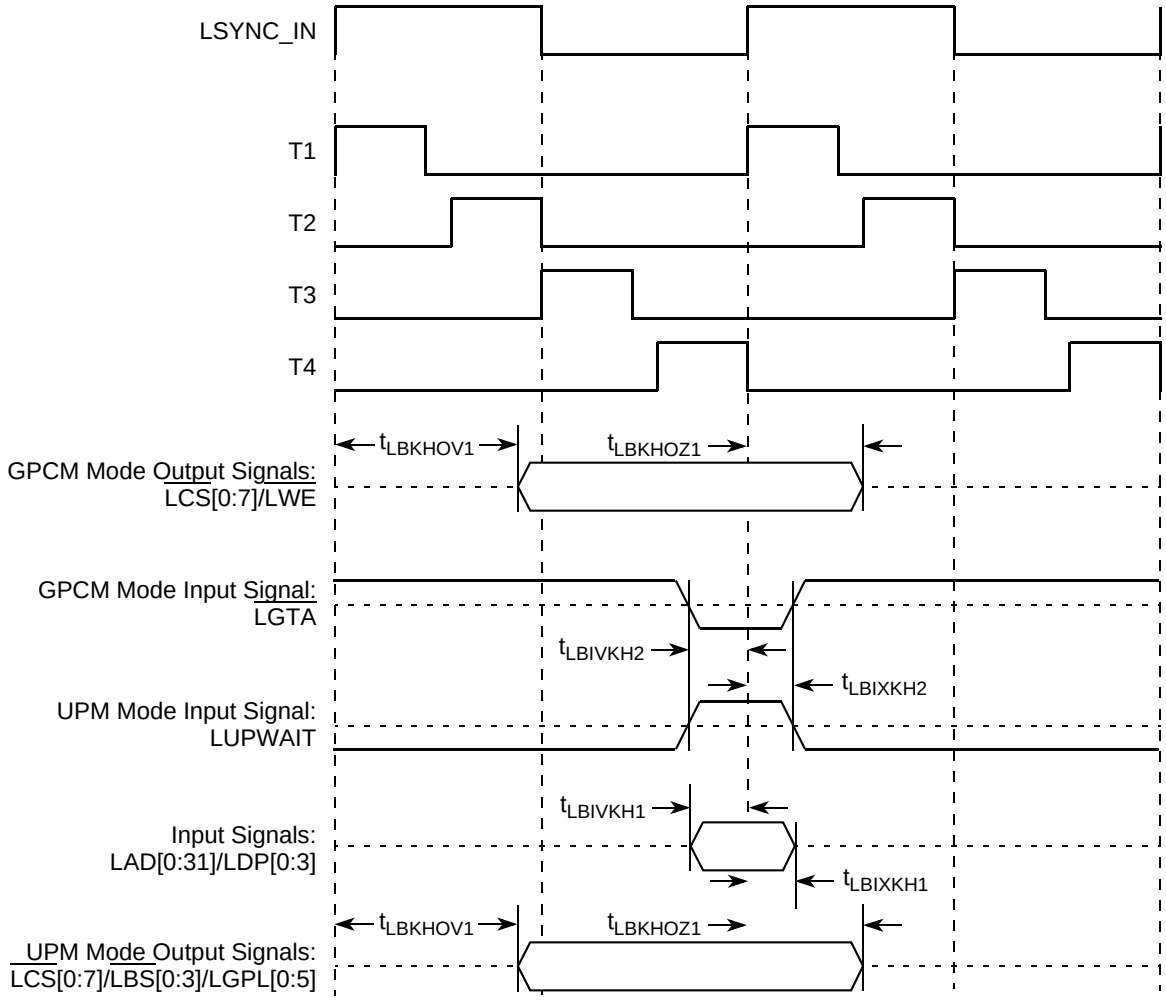

Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Figure 36 shows the PCI/PCI-X input AC timing conditions.

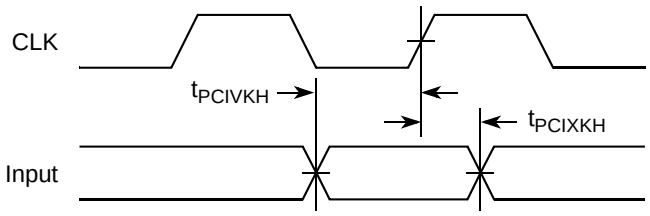

Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.

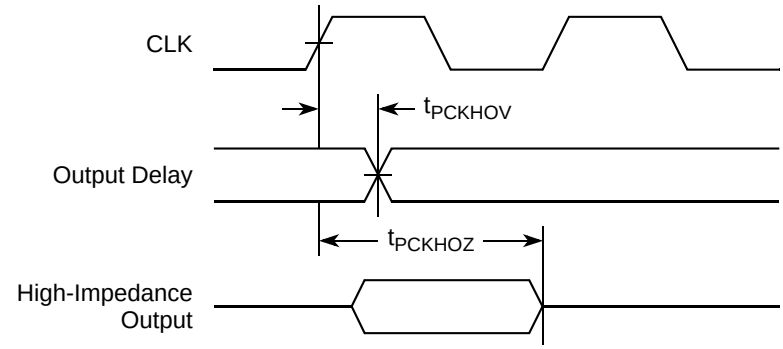

Figure 37. PCI/PCI-X Output AC Timing Measurement Condition

Table 53 provides the PCI-X AC timing specifications at 66 MHz.

Table 53. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11

16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- Single-ended swing
  The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.
- Differential output voltage, V_{OD} (or differential output swing):
  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.
- Differential input voltage, V_{ID} (or differential input swing):
  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.
- Differential peak voltage, V_{DIFFp}
  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- Differential peak-to-peak, $V_{DIFFp-p}$
  Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
- Common mode voltage, V_{cm}
  The common mode voltage is equal to one half of the sum of the voltages between each conductor

  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (see the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement:
  - This requirement is described in detail in the following sections.

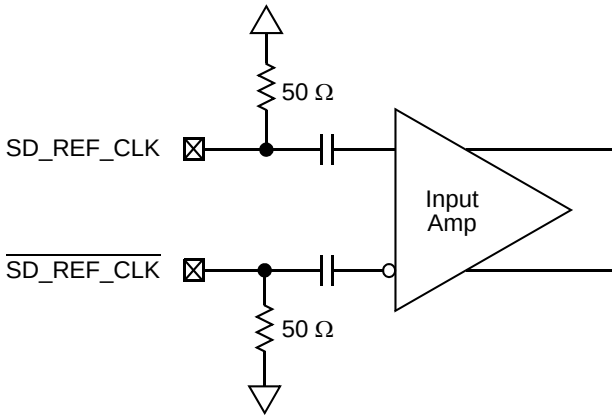

Figure 39. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

- Differential mode

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

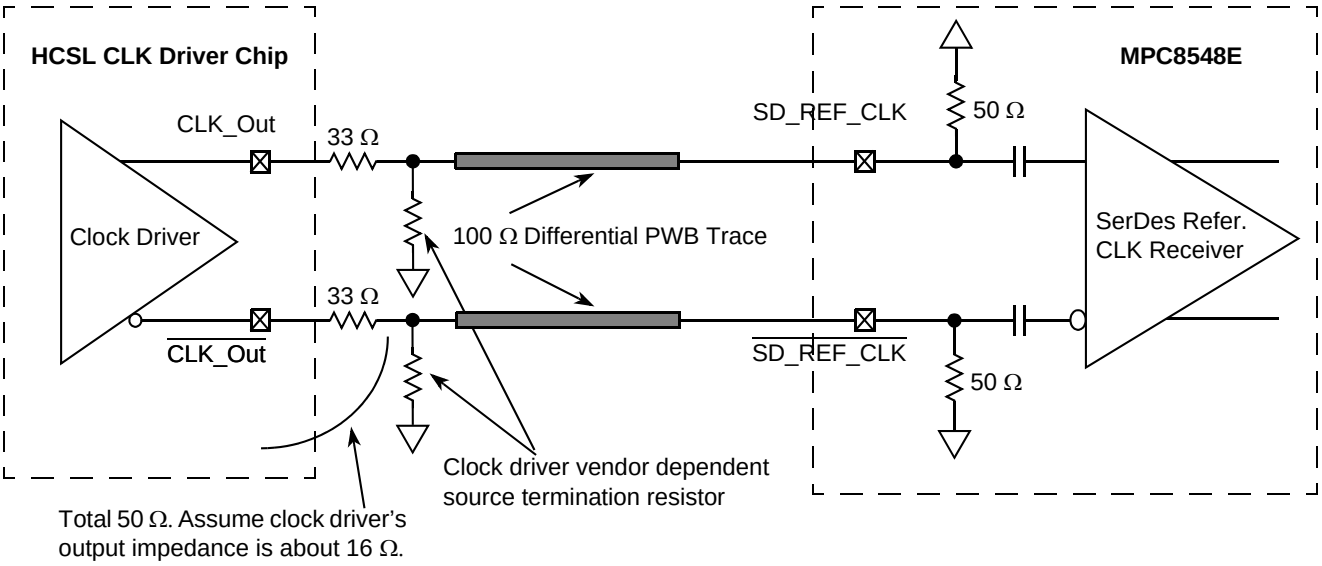

Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

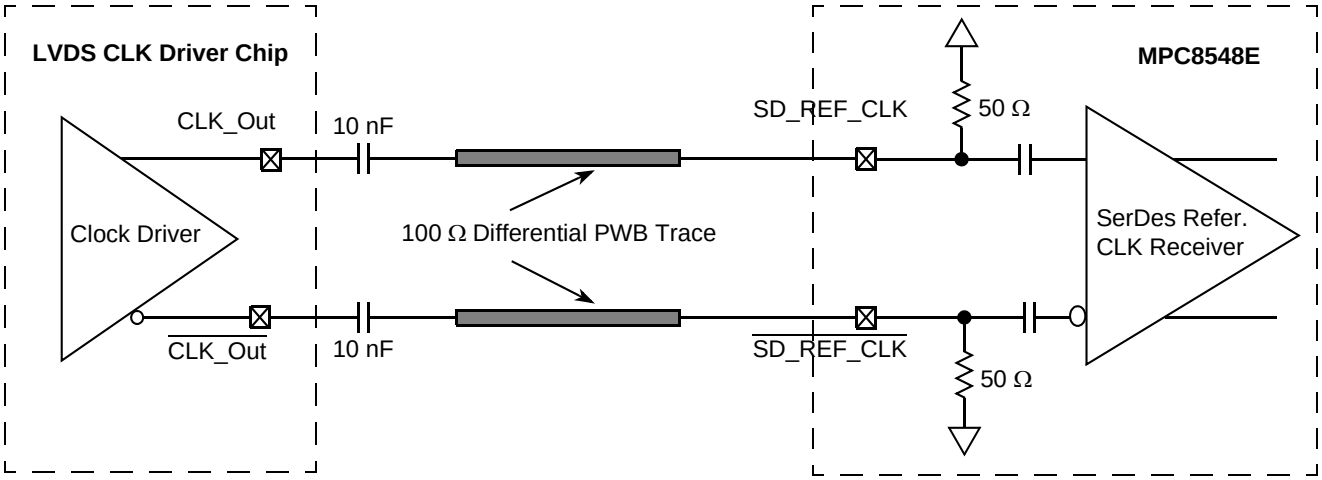

Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-}\rvert$. See Note 2.
$V_{TX-DE-RATIO}$	De- emphasized differential output voltage (ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = RMS(\lvert V_{TXD+} + V_{TXD-}\rvert/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$\lvert V_{TX-CM-DC\ (during\ L0)} + V_{TX-CM-Idle-DC\ (during\ electrical\ idle)}\rvert \le 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D–	0	—	25	mV	$\lvert V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\rvert \le 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\lvert V_{TX-D+}\rvert$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\lvert V_{TX-D-}\rvert$. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\rvert \le 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.

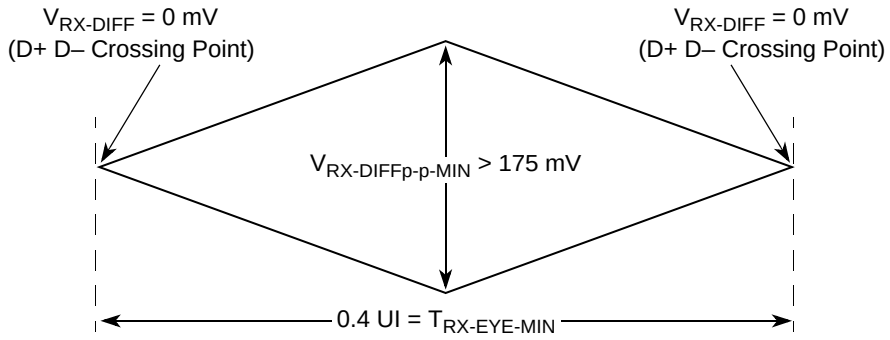

Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

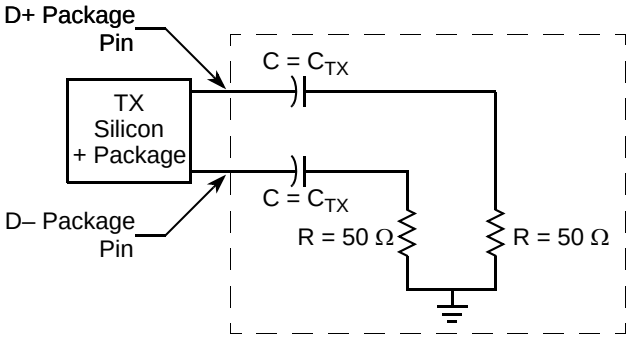

Figure 50. Compliance Test/Measurement Load

components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 66. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	800	800	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	400	400	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
3. A valid clock must be provided at POR if TSEC4_TXD[2] is set = 1.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, “CCB/SYSCLK PLL Ratio.”
8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections must be made to these pins if they are not used.
16. These pins are not connected for any use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI1\_C\_BE}}$[7:4]).
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx flow control.
24. Do not connect.

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FIFO1_RXC2	P5	I	LV_{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV_{DD}	15
cfg_dram_type1	R10	I	LV_{DD}	5
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV_{DD}	—
TSEC3_CRS	AA3	I/O	TV_{DD}	31
TSEC3_TX_ER	AB6	O	TV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:3]	M27, N25, P27, R25	I	XV_{DD}	—
SD_TX[0:3]	M22, N20, P22, R20	O	XV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV_{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
PCI1_REQ0	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
PCI1_DEVSEL	AH11	I/O	OV_{DD}	2
PCI1_FRAME	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
cfg_pci1_width	AF14	I/O	OV_{DD}	112
Reserved	V15	—	—	110
Reserved	AE28	—	—	2
Reserved	AD26	—	—	110
Reserved	AD25	—	—	110
Reserved	AE26	—	—	110
cfg_pci1_clk	AG24	I	OV_{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	110
Reserved	AG25	—	—	110
Reserved	AD24	—	—	110
Reserved	AF24	—	—	110
Reserved	AD27	—	—	110
Reserved	AD28, AE27, W17, AF26	—	—	110
Reserved	AH25	—	—	110
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Table 82. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	25	33.33	41.66	66.66	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500			
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533						
20	333	500							

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

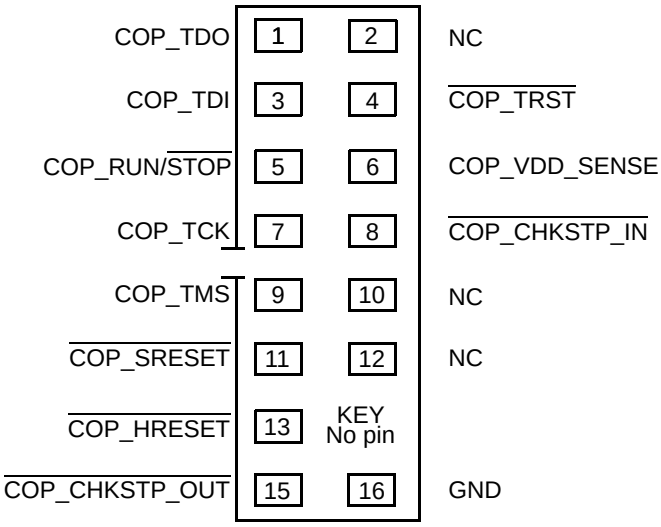

Figure 62. COP Connector Physical Pinout

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 87. Part Numbering Nomenclature

MPC	*nnnn*	*t*	*pp*	*ff*	*c*	*r*
Product Code	**Part Identifier**	**Temperature**	**Package[1, 2, 3]**	**Processor Frequency[4]**	**Core Frequency**	**Silicon Version**
MPC	8548E	Blank = 0 to 105°C C = –40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500[3] AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500[5] G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)