# E·XFL



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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547vjatgd
SATA USB Voltage - I/O Operating Temperature Security Features Package / Case Supplier Device Package Purchase URL	- - 1.8V, 2.5V, 3.3V 0°C ~ 105°C (TA) - 783-BBGA, FCBGA 783-FCPBGA (29x29) https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8547vjatgd

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#### Overview

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL\_2 compatible I/O (1.8-V SSTL\_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high-resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with  $F_2m$  and F(p) modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES

#### Overview

- AESU-Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I<sup>2</sup>C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave  $I^2C$  mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the  $I^2C$  interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I<sup>2</sup>C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT,  $\overline{\text{RTS}}$ ,  $\overline{\text{CTS}}$ )
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the device. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

# 2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

## 2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute	Maximum	Ratings	1
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Characteristic		Symbol	Max Value	Unit	Notes
Core supply vo	bltage	V <sub>DD</sub>	-0.3 to 1.21	V	—
PLL supply vol	tage	AV <sub>DD</sub>	-0.3 to 1.21	V	—
Core power su	pply for SerDes transceivers	SV <sub>DD</sub>	-0.3 to 1.21	V	—
Pad power sup	oply for SerDes transceivers	XV <sub>DD</sub>	-0.3 to 1.21	V	—
DDR and DDR	2 DRAM I/O voltage	GV <sub>DD</sub>	-0.3 to 2.75 -0.3 to 1.98	V	2
Three-speed E	thernet I/O voltage	LV <sub>DD</sub> (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	
		TV <sub>DD</sub> (for eTSEC3 and eTSEC4)	-0.3 to 3.63 -0.3 to 2.75		3
PCI/PCI-X, DUART, system control and power management, I <sup>2</sup> C, Ethernet MII management, and JTAG I/O voltage		OV <sub>DD</sub>	-0.3 to 3.63	V	_
Local bus I/O voltage		BV <sub>DD</sub>	-0.3 to 3.63 -0.3 to 2.75	V	—
Input voltage	DDR/DDR2 DRAM signals	MV <sub>IN</sub>	–0.3 to (GV <sub>DD</sub> + 0.3)	V	4
	DDR/DDR2 DRAM reference	MV <sub>REF</sub>	-0.3 to (GV <sub>DD</sub> /2 + 0.3)	V	—
	Three-speed Ethernet I/O signals	LV <sub>IN</sub> TV <sub>IN</sub>	-0.3 to (LV <sub>DD</sub> + 0.3) -0.3 to (TV <sub>DD</sub> + 0.3)	V	4
	Local bus signals	BV <sub>IN</sub>	-0.3 to (BV <sub>DD</sub> + 0.3)	_	—
	DUART, SYSCLK, system control and power management, I <sup>2</sup> C, Ethernet MII management, and JTAG signals	OV <sub>IN</sub>	-0.3 to (OV <sub>DD</sub> + 0.3)	V	4
	PCI/PCI-X	OV <sub>IN</sub>	-0.3 to (OV <sub>DD</sub> + 0.3)	V	4

# 4 Input Clocks

This section discusses the timing for the input clocks.

# 4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

## Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$ .

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f <sub>SYSCLK</sub>	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t <sub>SYSCLK</sub>	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t <sub>KHK</sub> /t <sub>SYSCLK</sub>	40	—	60	%	3
SYSCLK jitter	_	—	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

# 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{CCB}$ , and minimum clock low time is  $2 \times t_{CCB}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.

# 4.3 eTSEC Gigabit Reference Clock Timing

The following table provides the eTSEC gigabit reference clocks (EC\_GTX\_CLK125) AC timing specifications for the device.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
EC_GTX_CLK125 frequency	f <sub>G125</sub>	—	125	—	MHz	
EC_GTX_CLK125 cycle time	t <sub>G125</sub>	—	8	—	ns	
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t <sub>G125R</sub> , t <sub>G125F</sub>	_	_	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t <sub>G125H</sub> /t <sub>G125</sub>	45 47	_	55 53	%	2, 3

Table 6. EC_	GTX_CLK125	AC Timing	Specifications
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Notes:

1. Rise and fall times for EC\_GTX\_CLK125 are measured from 0.5 and 2.0 V for L/TV<sub>DD</sub> = 2.5 V, and from 0.6 and 2.7 V for L/TV<sub>DD</sub> = 3.3 V.

- 2. Timing is guaranteed by design and characterization.
- 3. EC\_GTX\_CLK125 is used to generate the GTX clock TSEC*n*\_GTX\_CLK for the eTSEC transmitter with 2% degradation. EC\_GTX\_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*\_GTX\_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

# 4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCIn\_CLK. The following table provides the PCI/PCI-X reference clock AC timing specifications for the device.

	Table 7.	PCIn_	CLK AC	Timing	S	pecifications
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At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$ .

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
PCIn_CLK frequency	f <sub>PCICLK</sub>	16	_	133	MHz	—
PCIn_CLK cycle time	t <sub>PCICLK</sub>	7.5	_	60	ns	—
PCIn_CLK rise and fall time	t <sub>PCIKH</sub> , t <sub>PCIKL</sub>	0.6	1.0	2.1	ns	1, 2
PCIn_CLK duty cycle	t <sub>PCIKHKL</sub> /t <sub>PCICLK</sub>	40		60	%	2

Notes:

1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

2. Timing is guaranteed by design and characterization.

# 5 **RESET** Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Parameter/Condition	Min	Мах	Unit	Notes
Required assertion time of HRESET	100	—	μS	—
Minimum assertion time for SRESET	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before HRESET negation	100	—	μS	—
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs	1

Table 8. RESE1	<b>Initialization</b>	Timing	Specifications
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#### Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

### Table 9. PLL Lock Times

Parameter/Condition	Min	Мах	Unit
Core and platform PLL lock times	—	100	μS
Local bus PLL lock time	—	50	μS
PCI/PCI-X bus PLL lock time	—	50	μS

## 5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements.

Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10.	Power	Supply	Ramp	Rate
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Parameter	Min	Мах	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	_	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.

2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, "PLL Power Supply Filtering," the recommended AVDD\_CORE, AVDD\_PLAT, AVDD\_LBIU, AVDD\_PCI1 and AVDD\_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

# 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

## 6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 1.8 \text{ V}$ .

### Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.25	V
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 2.5 \text{ V}$ .

### Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.31	V
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

### Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	<sup>t</sup> ciskew	-300 -365 -390	300 365 390	ps	1, 2

Notes:

1. t<sub>CISKEW</sub> represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t<sub>DISKEW</sub>. This can be determined by the following equation: t<sub>DISKEW</sub> = ± (T/4 – abs(t<sub>CISKEW</sub>)) where T is the clock period and abs(t<sub>CISKEW</sub>) is the absolute value of t<sub>CISKEW</sub>.

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV <sub>DD</sub> /TV <sub>DD</sub>	2.37	2.63	V	1, 2
Output high voltage ( $LV_{DD}/TV_{DD} = Min$ , $I_{OH} = -1.0 \text{ mA}$ )	V <sub>OH</sub> 2.00		LV <sub>DD</sub> /TV <sub>DD</sub> + 0.3	V	
Output low voltage ( $LV_{DD}/TV_{DD} = Min$ , I <sub>OL</sub> = 1.0 mA)	V <sub>OL</sub>	GND –0.3	0.40	V	
Input high voltage	V <sub>IH</sub>	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	
Input low voltage	V <sub>IL</sub>	-0.3	0.90	V	
Input high current ( $V_{IN} = LV_{DD}$ , $V_{IN} = TV_{DD}$ )	Ι <sub>ΙΗ</sub>	_	10	μΑ	1, 2, 3
Input low current (V <sub>IN</sub> = GND)	۱ <sub>IL</sub>	-15	_	μÂ	3

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Notes:

1.  $LV_{DD}$  supports eTSECs 1 and 2.

2.  $\mathsf{TV}_{\mathsf{DD}}$  supports eTSECs 3 and 4.

3. Note that the symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  and  $TV_{IN}$  symbols referenced in Table 1 and Table 2.

# 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

## 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*\_TX\_CLK, while the receive clock must be applied to pin TSEC*n*\_RX\_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*\_GTX\_CLK pin (while transmit data appears on TSEC*n*\_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*\_GTX\_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

#### Enhanced Three-Speed Ethernet (eTSEC)

Figure 10 shows the GMII receive AC timing diagram.



Figure 10. GMII Receive AC Timing Diagram

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

## 8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

fable 2	28.	MII	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t <sub>MTX</sub> <sup>2</sup>	_	400	_	ns
TX_CLK clock period 100 Mbps	t <sub>MTX</sub>		40	_	ns
TX_CLK duty cycle	t <sub>MTXH</sub> /t <sub>MTX</sub>	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t <sub>MTKHDX</sub>	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t <sub>MTXR</sub> <sup>2</sup>	1.0	_	4.0	ns
TX_CLK data clock fall (80%–20%)	t <sub>MTXF</sub> <sup>2</sup>	1.0		4.0	ns

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>MTKHDX</sub> symbolizes MII transmit timing (MT) for the time t<sub>MTX</sub> clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t<sub>MTX</sub> represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

## 8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	<b>AC Timing</b>	Specifications
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t <sub>TRX</sub>	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t <sub>SKTRX</sub>	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t <sub>TRXH</sub> /t <sub>TRX</sub>	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDVKH</sub>	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDXKH</sub>	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t <sub>TRXR</sub> <sup>2</sup>	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t <sub>TRXF</sub> <sup>2</sup>	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).</sub>

2. Guaranteed by design.



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

of a balanced interchange circuit and ground. In this example, for SerDes output,  $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$ , which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V<sub>OD</sub>) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V<sub>OD</sub> is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V<sub>DIFFp</sub>) is 500 mV. The peak-to-peak differential voltage (V<sub>DIFFp</sub>) is 1000 mVp-p.

## 16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD\_REF\_CLK and SD\_REF\_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

## 16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for  $XV_{DD SRDS2}$  are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
V <sub>TX-DIFFp-p</sub>	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times  V_{TX-D+} - V_{TX-D-} $ . See Note 2.
V <sub>TX-DE-RATIO</sub>	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T <sub>TX-EYE</sub>	Minimum TX eye width	0.70	—	_	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
T <sub>TX-EYE-MEDIAN-to-</sub> MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median.	_	_	0.15	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
T <sub>TX-RISE</sub> , T <sub>TX-FALL</sub>	D+/D-TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
V <sub>TX-CM-ACp</sub>	RMS AC peak common mode output voltage	_	_	20	mV	$\begin{split} & V_{TX\text{-}CM\text{-}ACp} = RMS( V_{TXD\text{+}} + V_{TXD\text{-}} /2 - V_{TX\text{-}CM\text{-}DC}) \\ & V_{TX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of }  V_{TX\text{-}D\text{+}} + V_{TX\text{-}D\text{-}} /2. \\ & See Note 2. \end{split}$
V <sub>TX-CM-DC-ACTIVE-</sub> IDLE-DELTA	Absolute delta of dc common mode voltage during L0 and electrical idle	0	_	100	mV	$\begin{split}  V_{TX-CM-DC} & (during \ L0) + V_{TX-CM-Idle-DC} & (during \\ electrical \ idle)  &\leq 100 \ mV \\ V_{TX-CM-DC} &= DC_{(avg)} \ of \  V_{TX-D+} + V_{TX-D-} /2 \ [L0] \\ V_{TX-CM-Idle-DC} &= DC_{(avg)} \ of \  V_{TX-D+} + V_{TX-D-} /2 \\ [electrical \ idle] \\ See \ Note \ 2. \end{split}$
VTX-CM-DC-LINE-DELTA	Absolute delta of DC common mode between D+ and D–	0	_	25	mV	$\begin{split}  V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}  &\leq 25 \text{ mV} \\ V_{TX-CM-DC-D+} &= DC_{(avg)} \text{ of }  V_{TX-D+}  \\ V_{TX-CM-DC-D-} &= DC_{(avg)} \text{ of }  V_{TX-D-} . \\ \text{See Note 2.} \end{split}$
V <sub>TX</sub> -IDLE-DIFFp	Electrical idle differential peak output voltage	0	_	20	mV	$V_{TX-IDLE-DIFFp} =  V_{TX-IDLE-D+} - V_{TX-IDLE-D-}  \le 20 \text{ mV.}$ See Note 2.
V <sub>TX-RCV-DETECT</sub>	The amount of voltage change allowed during receiver detection	_	_	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V <sub>RX-CM-ACp</sub>	AC peak common mode input voltage	_	_	150	mV	$\begin{split} & V_{RX\text{-}CM\text{-}ACp} =  V_{RXD\text{+}} - V_{RXD\text{-}} /2 + V_{RX\text{-}CM\text{-}DC} \\ & V_{RX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of }  V_{RX\text{-}D\text{+}} + V_{RX\text{-}D\text{-}}  \div 2. \\ & See Note 2. \end{split}$
RL <sub>RX-DIFF</sub>	Differential return loss	15	—	_	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4.
RL <sub>RX-CM</sub>	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
Z <sub>RX-DIFF-DC</sub>	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z <sub>RX-DC</sub>	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 $\pm$ 20% tolerance). See Notes 2 and 5.
Z <sub>RX-HIGH-IMP-DC</sub>	Powered down DC input impedance	200 k	—	_	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
V <sub>RX-IDLE-DET-DIFFp-p</sub>	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFF_{p-p}} = 2 \times  V_{RX-D+} - V_{RX-D-} .$ Measured at the package pins of the receiver
T <sub>RX-IDLE-DET-DIFF-</sub> ENTERTIME	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ( $V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$ ) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

## Table 57. Differential Receiver (RX) Input Specifications (continued)

# 18.8 Receiver Eye Diagrams

For each baud rate at which an LP-serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 66, Table 67, and Table 68) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 54 with the parameters specified in Table 69. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a  $100-\Omega \pm 5\%$  differential resistive load.



Figure 54. Receiver Input Compliance Mask

Table 69. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V <sub>DIFF</sub> min (mV)	V <sub>DIFF</sub> max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

## **18.9 Measurement and Test Requirements**

Since the LP-serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE Std. 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE Std.

#### Serial RapidIO

802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

## 18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than  $10^{-12}$ . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be  $100-\Omega$  resistive  $\pm 5\%$  differential to 2.5 GHz.

## 18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

## 18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100  $\Omega$  resistive ± 5% differential to 2.5 GHz.

## 18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 18.7, "Receiver Specifications," and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 54 and Table 69. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 18.7, "Receiver Specifications," is then added to the signal and the test load is replaced by the receiver being tested.

#### **Package Description**

#### Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Package Description

Table 72	. MPC8547E	<b>Pinout Listing</b>	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV <sub>DD</sub>	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_	_	2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV <sub>DD</sub>	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV <sub>DD</sub>	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV <sub>DD</sub>	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV <sub>DD</sub>	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV <sub>DD</sub>	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV <sub>DD</sub>	_
MBA[0:2]	F7, J7, M11	0	GV <sub>DD</sub>	—
MWE	E7	0	GV <sub>DD</sub>	—
MCAS	H7	0	GV <sub>DD</sub>	—
MRAS	L8	0	GV <sub>DD</sub>	—
MCKE[0:3]	F10, C10, J11, H11	0	GV <sub>DD</sub>	11
MCS[0:3]	K8, J8, G8, F8	0	GV <sub>DD</sub>	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV <sub>DD</sub>	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV <sub>DD</sub>	_
MODT[0:3]	E6, K6, L7, M7	0	GV <sub>DD</sub>	—
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36

Signal	Signal Package Pin Number		Power Supply	Notes
TSEC2_TX_ER	R10	0	LV <sub>DD</sub>	5, 9, 33
Three	e-Speed Ethernet Controller (Gigabit Ethe	ernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV <sub>DD</sub>	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV <sub>DD</sub>	_
TSEC3_GTX_CLK	W8	0	TV <sub>DD</sub>	_
TSEC3_RX_CLK	W2	I	TV <sub>DD</sub>	_
TSEC3_RX_DV	W1	I	TV <sub>DD</sub>	—
TSEC3_RX_ER	Y2	I	TV <sub>DD</sub>	_
TSEC3_TX_CLK	V10	I	TV <sub>DD</sub>	_
TSEC3_TX_EN	V9	0	TV <sub>DD</sub>	30
Three	-Speed Ethernet Controller (Gigabit Ethe	ernet 4)	<u> </u>	
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV <sub>DD</sub>	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV <sub>DD</sub>	1
TSEC4_GTX_CLK	AA5	0	TV <sub>DD</sub>	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV <sub>DD</sub>	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV <sub>DD</sub>	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV <sub>DD</sub>	1, 30
· · ·	DUART			
UART_CTS[0:1]	AB3, AC5	I	OV <sub>DD</sub>	—
UART_RTS[0:1]	AC6, AD7	0	OV <sub>DD</sub>	—
UART_SIN[0:1]	AB5, AC7	I	OV <sub>DD</sub>	—
UART_SOUT[0:1]	AB7, AD8	0	OV <sub>DD</sub>	—
· · ·	I <sup>2</sup> C Interface			
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4, 27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4, 27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4, 27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4, 27
· · · · · ·	SerDes	·		
SD_RX[0:3]	M28, N26, P28, R26	I	XV <sub>DD</sub>	—
SD_RX[0:3]	M27, N25, P27, R25	I	XV <sub>DD</sub>	—
SD_TX[0:3]	M22, N20, P22, R20	0	XV <sub>DD</sub>	_
SD_TX[0:3]	M23, N21, P23, R21	0	XV <sub>DD</sub>	—
Reserved	W26, Y28, AA26, AB28	—	— —	40
Reserved	W25, Y27, AA25, AB27	—	-	40

## Table 72. MPC8547E Pinout Listing (continued)

#### System Design Information

level must always be equivalent to  $V_{DD}$ , and preferably these voltages are derived directly from  $V_{DD}$  through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the  $AV_{DD}$  pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific  $AV_{DD}$  pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.



Figure 57. PLL Power Supply Filter Circuit with PLAT Pins



Figure 58. PLL Power Supply Filter Circuit with CORE Pins



Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV<sub>DD</sub>\_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV<sub>DD</sub>\_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the AV<sub>DD</sub>\_SRDS ball. The 0.003- $\mu$ F capacitor is closest to the ball, followed by the two 2.2  $\mu$ F capacitors, and finally the 1  $\Omega$  resistor to the board supply plane. The capacitors are connected from AV<sub>DD</sub>\_SRDS to