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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

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Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8547vtaqgb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

4.5 Platform to FIFO Restrictions

Note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency \leq platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 167 MHz.

4.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

See *MPC8548ERM*, *Rev.* 2, *PowerQUICC III Integrated Processor Family Reference Manual*, Section 18.1.3.2, "Link Width," for PCI Express interface width details.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

 $2 \times (0.80) \times (Serial RapidIO interface frequency) \times (Serial RapidIO link width)$

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See *MPC8548ERM*, *Rev.* 2, *PowerQUICC III Integrated Processor Family Reference Manual*, Section 17.4, "1x/4x LP-Serial Signal Descriptions," for serial RapidIO interface width and frequency details.

4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform see the specific section of this document.

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.37	2.63	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, I _{OH} = -1.0 mA)	V _{OH}	2.00	LV _{DD} /TV _{DD} + 0.3	V	
Output low voltage ($LV_{DD}/TV_{DD} = Min$, I _{OL} = 1.0 mA)	V _{OL}	GND –0.3	0.40	V	
Input high voltage	V _{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	
Input low voltage	V _{IL}	-0.3	0.90	V	
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	Ι _{ΙΗ}	_	10	μΑ	1, 2, 3
Input low current (V _{IN} = GND)	۱ _{IL}	-15	_	μÂ	3

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. $\mathsf{TV}_{\mathsf{DD}}$ supports eTSECs 3 and 4.

3. Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

A summary of the FIFO AC specifications appears in Table 24 and Table 25.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
TX_CLK, GTX_CLK clock period	t _{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t _{FITH} /t _{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}	—	_	250	ps
Rise time TX_CLK (20%–80%)	t _{FITR}	—	_	0.75	ns
Fall time TX_CLK (80%–20%)	t _{FITF}	—	_	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t _{FITDV}	2.0	_	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	_	3.0	ns

Table 24. FIFO Mode Transmit AC Timing Specification

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t _{FIRH} /t _{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t _{FIRJ}	—		250	ps
Rise time RX_CLK (20%-80%)	t _{FIRR}	—	_	0.75	ns
Fall time RX_CLK (80%–20%)	t _{FIRF}	—	_	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{FIRDX}	0.5			ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 4.5, "Platform to FIFO Restrictions."

Timing diagrams for FIFO appear in Figure 6 and Figure 7.



Figure 6. FIFO Transmit AC Timing Diagram







Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII 1	Transmit AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSEC <i>n</i> _TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns

Local Bus



Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).



Figure 34 shows the AC timing diagram for the I^2C bus.



Figure 34. I²C Bus AC Timing Diagram

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

High-Speed Serial Interfaces (HSSI)

- The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DCor AC-coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.



Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

PCI Express

Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{RX-CM-ACp}	AC peak common mode input voltage	_	_	150	mV	$\begin{split} & V_{RX\text{-}CM\text{-}ACp} = V_{RXD\text{+}} - V_{RXD\text{-}} /2 + V_{RX\text{-}CM\text{-}DC} \\ & V_{RX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } V_{RX\text{-}D\text{+}} + V_{RX\text{-}D\text{-}} \div 2. \\ & See Note 2. \end{split}$
RL _{RX-DIFF}	Differential return loss	15	—	_	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4.
RL _{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
Z _{RX-DIFF-DC}	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z _{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 \pm 20% tolerance). See Notes 2 and 5.
Z _{RX-HIGH-IMP-DC}	Powered down DC input impedance	200 k	—	_	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
V _{RX-IDLE-DET-DIFFp-p}	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFF_{p-p}} = 2 \times V_{RX-D+} - V_{RX-D-} .$ Measured at the package pins of the receiver
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	ļ	BV _{DD}	_
LSYNC_OUT	F28	0	BV _{DD}	_
	DMA			
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 102
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	_
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	_
	Programmable Interrupt Controller			
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	_
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	_
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)		
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	Τ7	0	LV _{DD}	—

Table 72.	MPC8547E	Pinout Listing	(continued)
		i mout Listing	(continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DFT			
L1_TSTCLK	AC25	I	OV _{DD}	25
L2_TSTCLK	AE22	I	OV _{DD}	25
LSSD_MODE	AH20	I	OV _{DD}	25
TEST_SEL	AH14	I	OV _{DD}	25
	Thermal Management			
THERMO	AG1			14
THERM1	AH1			14
	Power Management			
ASLEEP	AH18	0	OV_{DD}	9, 19, 29
	Power and Ground Signals			
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 	_	_	_
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}	

Signal	Package Pin Number	Pin Type	Power Supply	Notes						
TDO	AF28	0	OV _{DD}	—						
TMS	AH27	I	OV _{DD}	12						
TRST	AH23	I	OV _{DD}	12						
DFT										
L1_TSTCLK	AC25	I	OV _{DD}	25						
L2_TSTCLK	AE22	I	OV _{DD}	25						
LSSD_MODE	AH20	I	OV_{DD}	25						
TEST_SEL	AH14	I	OV _{DD}	25						
	Thermal Management									
THERM0	AG1	—	_	14						
THERM1	AH1	_	_	14						
	Power Management									
ASLEEP	AH18	0	OV _{DD}	9, 19, 29						
	Power and Ground Signals									
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 									
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}							
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	_						
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}							

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}		
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	_	
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	—	
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	_	
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV _{DD}	_	
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26	
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26	
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26	
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)		26	
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26	
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26	
SENSEVDD	M14	0	V _{DD}	13	
SENSEVSS	M16	—	—	13	
	Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF		

Table 73. MPC8545E Pinout Listing (continued)

20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

Characteristic	Maximum		Processor Core F		Frequency		Unit	Notes
					1333 11172			
	Min	Мах	Min	Мах	Min	Мах		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

 Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)

Notes:

 Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.) The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 76. Processor Core Clocking Specifications (MPC8545E)

Characteristic	Maximum Processor Core Frequency							
	800 MHz		1000 MHz		1200 MHz		Unit	Notes
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-board	N/A	$R_{ extsf{ heta}JB}$	5	°C/W	3
Die junction-to-case	N/A	$R_{ ext{ heta}JC}$	0.8	°C/W	4

Table 85. Package Thermal Characteristics for FC-PBGA (continued)

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed-circuit board is the recommended procedure using a maximum of 10 lbs force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

22 System Design Information

This section provides electrical design recommendations for successful application of the device.

22.1 System Clocking

This device includes five PLLs, as follows:

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 20.2, "CCB/SYSCLK PLL Ratio."
- 2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 20.3, "e500 Core PLL Ratio."
- 3. The PCI PLL generates the clocking for the PCI bus.
- 4. The local bus PLL generates the clock for the local bus.
- 5. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS, respectively). The AV_{DD}

System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

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