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Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548cvjaqgd

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6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t _{DDKHAS}	1.48 1.95 2.40		ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t ddkhax	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCS	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCX	1.48 1.95 2.40		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	^t DDKHDS, ^t DDKLDS	538 700 900	 	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	^t ddkhdx, ^t ddkldx	538 700 900		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5 imes t_{MCK}$ + 0.6	ns	6

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = min$, $I_{OH} = -4.0 mA$)	V _{OH}	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	_
Output low voltage ($LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA$)	V _{OL}	GND	0.50	V	_
Input high voltage	V _{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	_
Input low voltage	V _{IL}	-0.3	0.90	V	_
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IH}	—	40	μΑ	1, 2, 3
Input low current (V _{IN} = GND)	IIL	-600	_	μA	

Table 22.	GMII. MI	I. RMII. a	and TBI DC	Electrical	Characteristics
	O min, mi	.,		Licothour	onaraotoristios

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. TV_DD supports eTSECs 3 and 4.

3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.







Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII 1	Transmit AC	Timing	Specifications
------------------	-------------	--------	----------------

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSEC <i>n</i> _TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the device.

10.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3 \text{ V DC}$.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($V_{IN}^{1} = 0 V \text{ or } V_{IN} = BV_{DD}$)	I _{IN}	_	±5	μΑ
High-level output voltage ($BV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	_	0.4	V

Table 38. Local Bus DC Electrical Characteristics (3.3 V DC)

Note:

1. Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 39 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5 \text{ V DC}$.

Table 39. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = BV_{DD})$	I _{IH}	—	10	μA
	IIL		-15	
High-level output voltage ($BV_{DD} = min, I_{OH} = -1 mA$)	V _{OH}	2.0	—	V
Low-level output voltage ($BV_{DD} = min$, $I_{OL} = 1 mA$)	V _{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	_	150	ps	7, 8
Input setup to local bus clock (except LGTA/UPWAIT)	t _{LBIVKH1}	1.9	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	_	2.1	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}		2.3	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}		2.4	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}		2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}		2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}		2.6	ns	5

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub></sub>

- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.



Figure 22. Local Bus AC Test Load

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.



This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V with PLL disabled.

Table 42. Local Bus Timing	Parameters—PLL Bypassed
----------------------------	-------------------------

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	—	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t _{lbkhkt}	2.3	4.4	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	6.2	—	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.1	—	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	—	ns	4, 5

Local Bus



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

JTAG

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.







Figure 32. Boundary-Scan Timing Diagram

3.	The maximum t _{I2DXKL}	has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal	al.

For the detail of I²C frequency calculation, see Determining the I²C Frequency Divider Ratio for SCL (AN2919). Note that the

200 MHz

390 kHz

0x26

512

133 MHz

346 kHz

0x00

384

4. Guaranteed by design.

FDR bit setting

I²C source clock frequency

Actual FDR divider selected

Actual I²C SCL frequency generated

Figure 33 provides the AC test load for the I^2C .



Figure 33. I²C AC Test Load

57

Table 46. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	—	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (see the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the device acts as the I²C bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as a transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 kHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

266 MHz

378 kHz

0x05

704

333 MHz

0x2A

371 kHz

896

I²C source clock frequency is half of the CCB clock frequency for the device.

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

High-Speed Serial Interfaces (HSSI)







Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

High-Speed Serial Interfaces (HSSI)

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.





Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
------------------------------	-------------------------

Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	_	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

19.2 Mechanical Dimensions of the HiCTE FC-CBGA and FC-PBGA with Full Lid

The following figures show the mechanical dimensions and bottom surface nomenclature for the MPC8548E HiCTE FC-CBGA and FC-PBGA packages.



the HiCTE FC-CBGA and FC-PBGA with Full Lid

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_		2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Table 72	. MPC8547E	Pinout	Listing ((continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes				
Local Bus Controller Interface								
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	_				
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	_				
LA[27]	H21	0	BV _{DD}	5, 9				
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9				
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	_				
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1				
LCS6/DMA_DACK2	G20	0	BV _{DD}	1				
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1				
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9				
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9				
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9				
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9				
LALE	H24	0	BV _{DD}	5, 8, 9				
LBCTL	G27	0	BV _{DD}	5, 8, 9				
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9				
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9				
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9				
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9				
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	—				
LGPL5	E26	0	BV _{DD}	5, 9				
LCKE	E24	0	BV _{DD}	—				
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	—				
LSYNC_IN	F27	I	BV _{DD}	—				
LSYNC_OUT	F28	0	BV _{DD}	_				
	DMA			•				
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 107				
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—				
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	—				
	Programmable Interrupt Controller		•					
UDE	AH16	I	OV _{DD}	—				
MCP	AG19	I	OV _{DD}	—				

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	Ι	OV _{DD}	_
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21		OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)		
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6		LV _{DD}	
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	Τ7	0	LV _{DD}	
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 2)		
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	-	LV _{DD}	_
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	0	LV _{DD}	5, 9, 33
TSEC2_COL	P1	I	LV _{DD}	—
TSEC2_CRS	R6	I/O	LV _{DD}	20
TSEC2_GTX_CLK	P6	0	LV _{DD}	
TSEC2_RX_CLK	N4		LV _{DD}	
TSEC2_RX_DV	P5		LV _{DD}	
TSEC2_RX_ER	R1	I	LV _{DD}	_
TSEC2_TX_CLK	P10	I	LV _{DD}	_
TSEC2_TX_EN	P7	0	LV _{DD}	30

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	0	BV _{DD}	—
	DMA		I	
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 108
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	—
	Programmable Interrupt Controller		I	
UDE	AH16	I	OV _{DD}	_
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
	Three-Speed Ethernet Controller (Gigabit Ether	rnet 1)		
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	Τ7	0	LV _{DD}	
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a $1-\mu F$ ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA_DACK[0:1], and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout