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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548cvtaqgd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

 Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
 - Flexible configuration.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
 - Four inbound windows plus a default window on RapidIO[™]
 - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
 - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface
 - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
 - DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
 - Full ECC support
 - Page mode support
 - Up to 16 simultaneous open pages for DDR

Overview

- AESU-Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

Power Characteristics

Power Characteristics 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Table 4. Device Power Dissipation

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on V_{DD} = 1.1 V, T_i = 65°C.

3. Typical-65 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 65^{\circ}\text{C}$, running Dhrystone. 4. Typical-105 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running Dhrystone. 5. Maximum is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running a smoke test.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 30	. TBI	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	_	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	_	—	ns
GTX_CLK rise (20%–80%)	t _{TTXR} ²		_	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} ²		_	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	AC Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t _{TRX}	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t _{SKTRX}	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t _{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t _{TRDXKH}	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t _{TRXR} ²	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t _{TRXF} ²	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}

2. Guaranteed by design.







Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII 1	Transmit AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSEC <i>n</i> _TX_CLK (20%–80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t _{RMRR}	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMRF}	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	—	0.90	V
Input high current ($OV_{DD} = Max, V_{IN}^{1} = 2.1 V$)	I _{IH}	—	40	μA
Input low current ($OV_{DD} = Max, V_{IN} = 0.5 V$)	I _{IL}	-600	—	μΑ

Table 36. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t _{MDC}	120.5		1389	ns	—
MDC clock pulse width high	width high t _{MDCH} 32 —		—	ns	—	
MDC to MDIO valid	t _{MDKHDV}	$16 \times t_{CCB}$		—	ns	5
MDC to MDIO delay	t _{MDKHDX}	(16 × t _{CCB} × 8) – 3		$(16 \times t_{\rm CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t _{MDDVKH}	5		—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0		—	ns	—
MDC rise time	t _{MDCR}	_	_	10	ns	4

10.2 Local Bus AC Electrical Specifications

This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.3	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}		2.5	ns	5

Table 40. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Parar	Symbol ²	Min	Мах	Unit	Notes	
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	4 2	20 10	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	30 30		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO		t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

 Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.



Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.



Figure 30. JTAG Clock Input Timing Diagram



Figure 34 shows the AC timing diagram for the I^2C bus.



Figure 34. I²C Bus AC Timing Diagram

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
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Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	—	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 50. Compliance Test/Measurement Load

Serial RapidIO

Characteristic	Symbol	Ra	nge	Unit	Netos
Characteristic	Min Max		Unit	Notes	
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	800	1600	mVp-p	_
Deterministic jitter	J _D	—	0.17	UI p-p	_
Total jitter	J _T	—	0.35	UI p-p	_
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 63. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Table 64. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notos
	Symbol	Min	Max	Onic	NOIES
Output voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	800	1600	mVp-p	_
Deterministic jitter	J _D	—	0.17	UI p-p	_
Total jitter	J _T	—	0.35	UI p-p	_
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 52 with the parameters specified in Table 65 when measured at the output pins of the device and the device is driving a $100-\Omega \pm 5\%$ differential resistive load. The output eye pattern of an LP-serial

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4		OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
cfg_pci1_width	AF14	I/O	OV _{DD}	112
Reserved	V15		—	110
Reserved	AE28	_		2
Reserved	AD26		—	110
Reserved	AD25		—	110
Reserved	AE26		—	110
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_	_	101
Reserved	AE25	_		110
Reserved	AG25		—	110
Reserved	AD24	_	—	110
Reserved	AF24	_	—	110
Reserved	AD27	_	_	110
Reserved	AD28, AE27, W17, AF26		—	110
Reserved	AH25		—	110
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	—
MBA[0:2]	F7, J7, M11	0	GV _{DD}	_

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1		_	104
Reserved	R6	—	—	104
Reserved	P6		_	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV _{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	_	105
FIFO1_TXC2	P7	0	LV _{DD}	15
cfg_dram_type1	R10	0	LV _{DD}	5, 9
Thr	ee-Speed Ethernet Controller (Gigabit I	Ethernet 3)		
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_
TSEC3_GTX_CLK	W8	0	TV _{DD}	_
TSEC3_RX_CLK	W2	I	TV _{DD}	_
TSEC3_RX_DV	W1	I	TV _{DD}	_
TSEC3_RX_ER	Y2	I	TV _{DD}	_
TSEC3_TX_CLK	V10	I	TV _{DD}	—
TSEC3_TX_EN	V9	0	TV _{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	_
Reserved	AA5	—	_	15
TSEC3_COL	Y5	I	TV _{DD}	—
TSEC3_CRS	AA3	I/O	TV _{DD}	31
TSEC3_TX_ER	AB6	0	TV _{DD}	—
	DUART	1		
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	_
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	_
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	—
	I ² C interface	I		
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27

Table 74. MPC8543E Pinout Listing (continued)

System Design Information

level must always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.



Figure 57. PLL Power Supply Filter Circuit with PLAT Pins



Figure 58. PLL Power Supply Filter Circuit with CORE Pins



Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD}_SRDS ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout

Rev. Number	Date	Substantive Change(s)
2	04/2008	 Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit.") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	 Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." Added Section 4.4, "PCI/PCL-X Reference Clock Timing." Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified Note 4 of Table 29, "GMII, MII, RMII, and TBI DC Electrical Characteristics." Corrected V_{IL}(max) in Table 22, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. Corrected V_{IH}(min) in Table 36, "MII Management DC Electrical Characteristics." Corrected V_{IH}(min) in Table 37, "MII Management AC Timing Specifications." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKH2}, t_{LBIXKH1}, and t_{LBIXKH2} in Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled" and Table 40, "Local Bus Timing Parameters (BV_{DD} = 3.5 V)—PLL Enabled." Updated parameter descriptions for t_{LBIVKH1}, t_{LBIVKL2}, t_{LBIXKH1}, and t_{LBIXKL2} in Table 42, "Local Bus Timing Parameters —PLL Bypassed." Note that t_{LBIVKL2} and t_{LBIXKL2} in Table 42, "Local Bus Signals (PLL Bypass Mode)." Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." Added LOPWAIT assertion in Figure 26, Figure 27 and Figure 28. Carrified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" Added LOP
0	07/2007	Initial Release

Table 88. Document Revision History (continued)