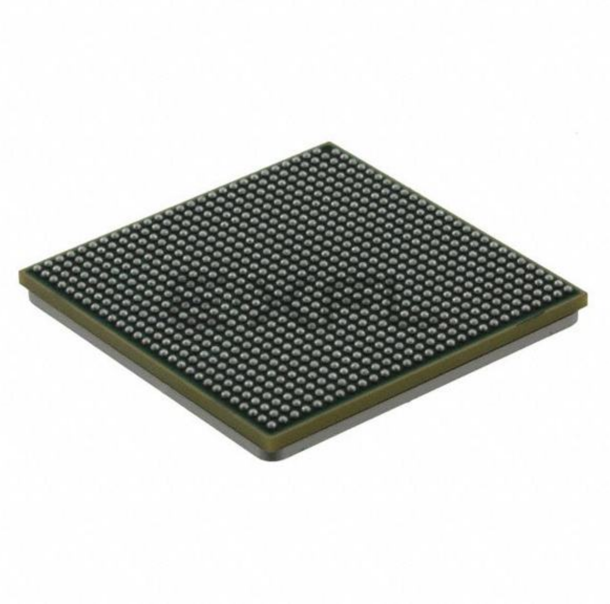

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548echxaqg

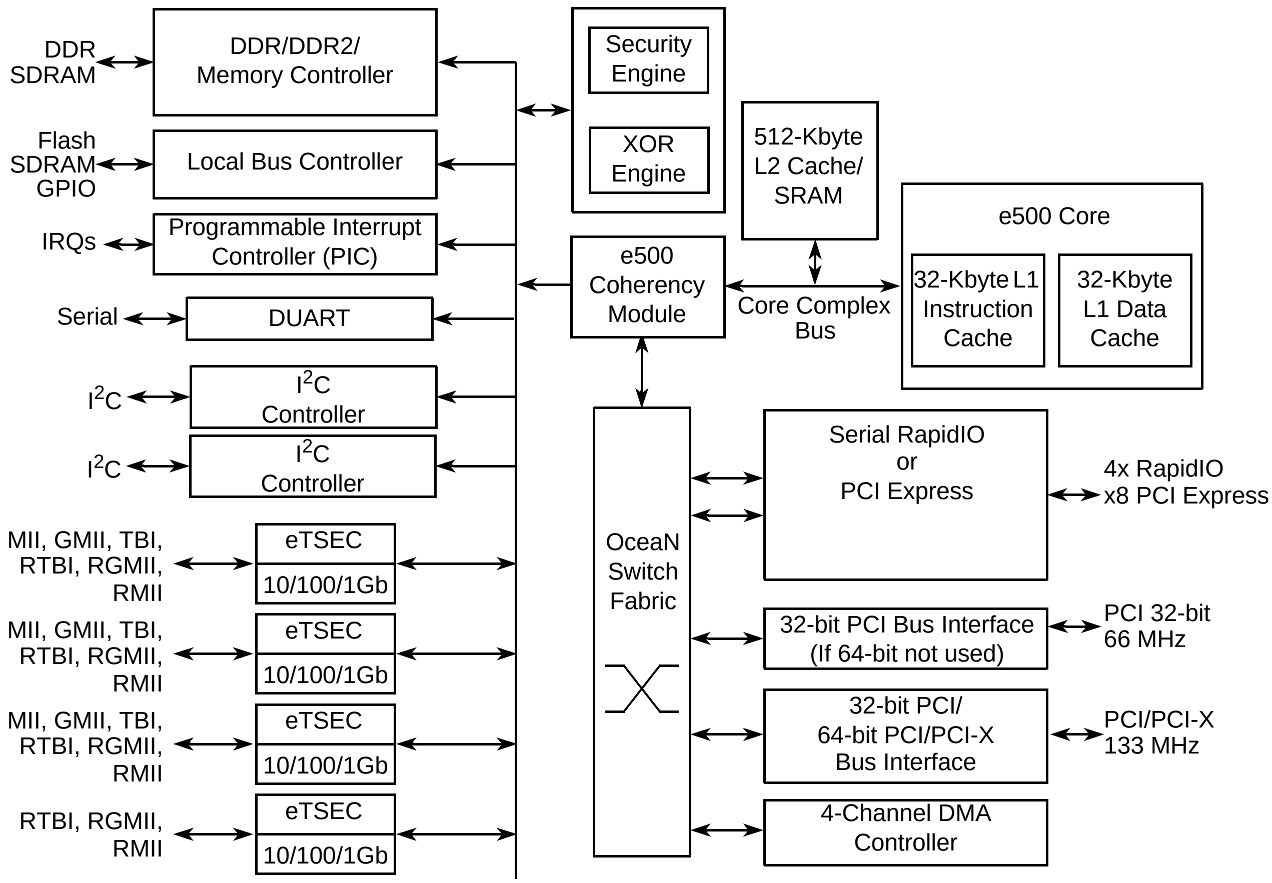

Figure 1. Device Block Diagram

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
  - — 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - — Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
  - — Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - — 36-bit real addressing
  - — Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - — Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
  - — Enhanced hardware and software debug support

— Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
  - Flexible configuration.
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
  - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and Flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be Flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
    - Four inbound windows plus a default window on RapidIO™
    - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
    - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface
  - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
  - DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
  - Full ECC support
  - Page mode support
    - Up to 16 simultaneous open pages for DDR

- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

• Dual I^2C controllers
- Two-wire interface
- Multiple master support
- Master or slave I^2C mode support
- On-chip digital filtering rejects spikes on the bus

• Boot sequencer
- Optionally loads configuration data from serial ROM at reset via the I^2C interface
- Can be used to initialize configuration registers and/or memory
- Supports extended I^2C addressing mode
- Data integrity checked with preamble signature and CRC

• DUART
- Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
- Programming model compatible with the original 16450 UART and the PC16550D

• Local bus controller (LBC)
- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per chip select basis:
  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)

- VRRP and HSRP support for seamless router fail-over
- Up to 16 exact-match MAC addresses supported
- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode

— Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
— RMON statistics support
— 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
— MII management interface for control and status
— Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  — Full crossbar packet switch
  — Reorders packets from a source based on priorities
  — Reorders packets to bypass blocked packets
  — Implements starvation avoidance algorithms
  — Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  — Four-channel controller
  — All channels accessible by both the local and remote masters
  — Extended DMA functions (advanced chaining and striding capability)
  — Support for scatter and gather transfers
  — Misaligned transfer capability
  — Interrupt on completed segment, link, list, and error
  — Supports transfers to or from any local memory or I/O port
  — Selectable hardware-enforced coherency (snoop/no snoop)
  — Ability to start and flow control each DMA channel from external 3-pin interface
  — Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
  — PCI 2.2 and PCI-X 1.0 compatible
  — One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
  — One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
  — Host and agent mode support
  — 64-bit dual address cycle (DAC) support
  — PCI-X supports multiple split transactions
  — Supports PCI-to-memory and memory-to-PCI streaming

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
3. The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
4. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage		AV_{DD}	1.1 V ± 55 mV	V	1
Core power supply for SerDes transceivers		SV_{DD}	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.1 V ± 55 mV	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	—	4
PCI/PCI-X, DUART, system control and power management, I^2C, Ethernet MII management, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, Ethernet MII management, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that GV_{DD}(typ) = 2.5 V for DDR SDRAM, and GV_{DD}(typ) = 1.8 V for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

A timing diagram for TBI receive appears in Figure 16.

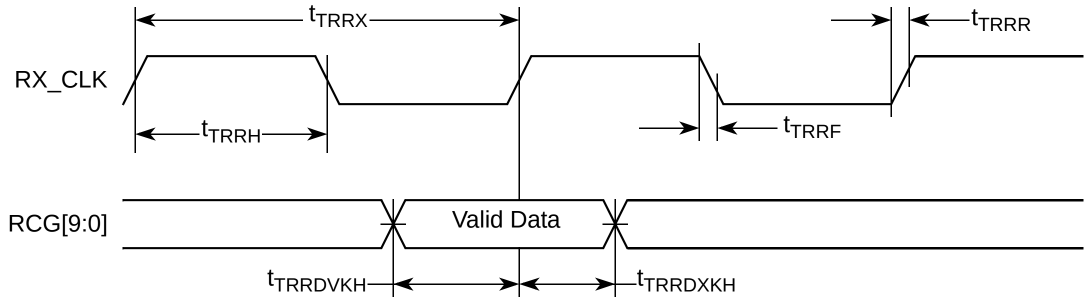

Figure 16. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 33. RGMII and RTBI AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period [3]	t_{RGT}[5]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX[3, 4]	t_{RGTH}/t_{RGT}[5]	45	50	55	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. In rev 1.0 silicon, due to errata, t_{SKRGT} is -650 ps (min) and 650 ps (max). See “eTSEC 10” in the device errata document.

Figure 19 provides the AC test load for eTSEC.

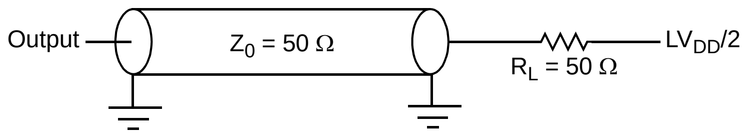

Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.

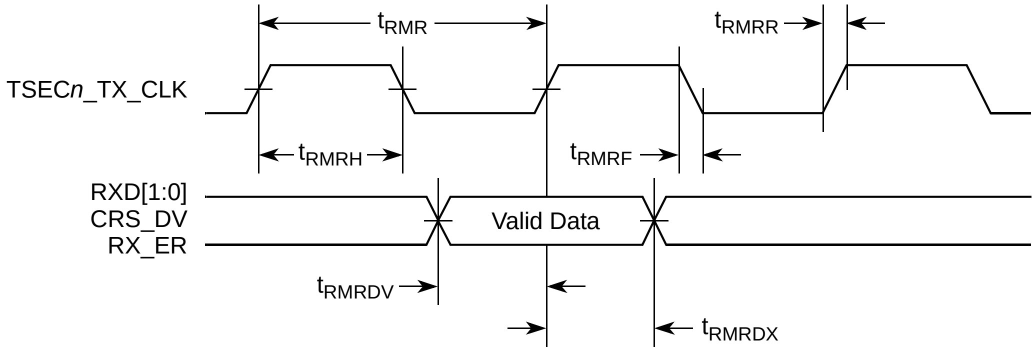

Figure 20. RMII Receive AC Timing Diagram

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—		10	ns	4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB} \div 64$ and minimum $f_{MDC} = f_{CCB} \div 448$. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the *MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual* for more detail.
3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
4. Guaranteed by design.
5. t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.

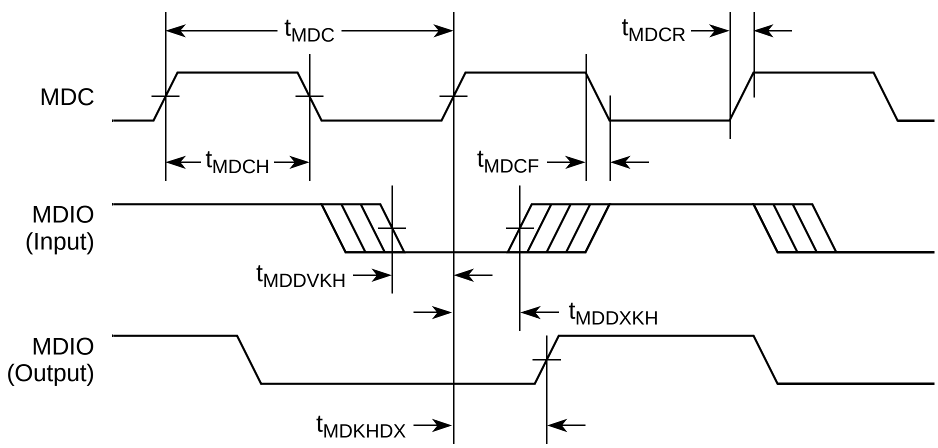

Figure 21. MII Management Interface Timing Diagram

— The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.

— For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode

— The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.

— The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.

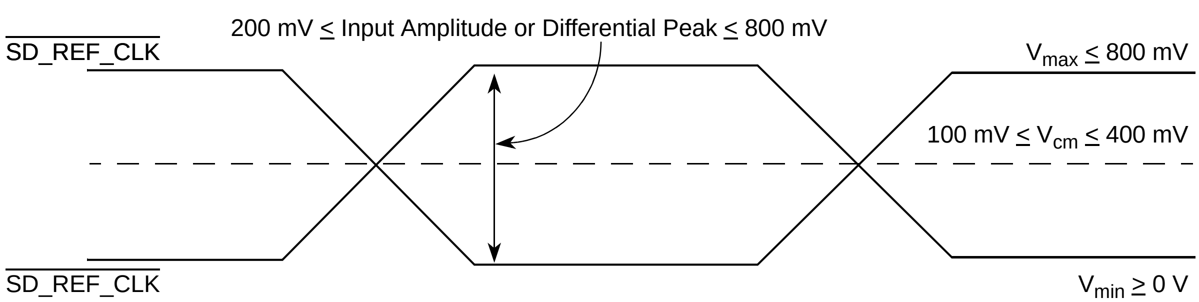

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Table 68. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	320	320	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

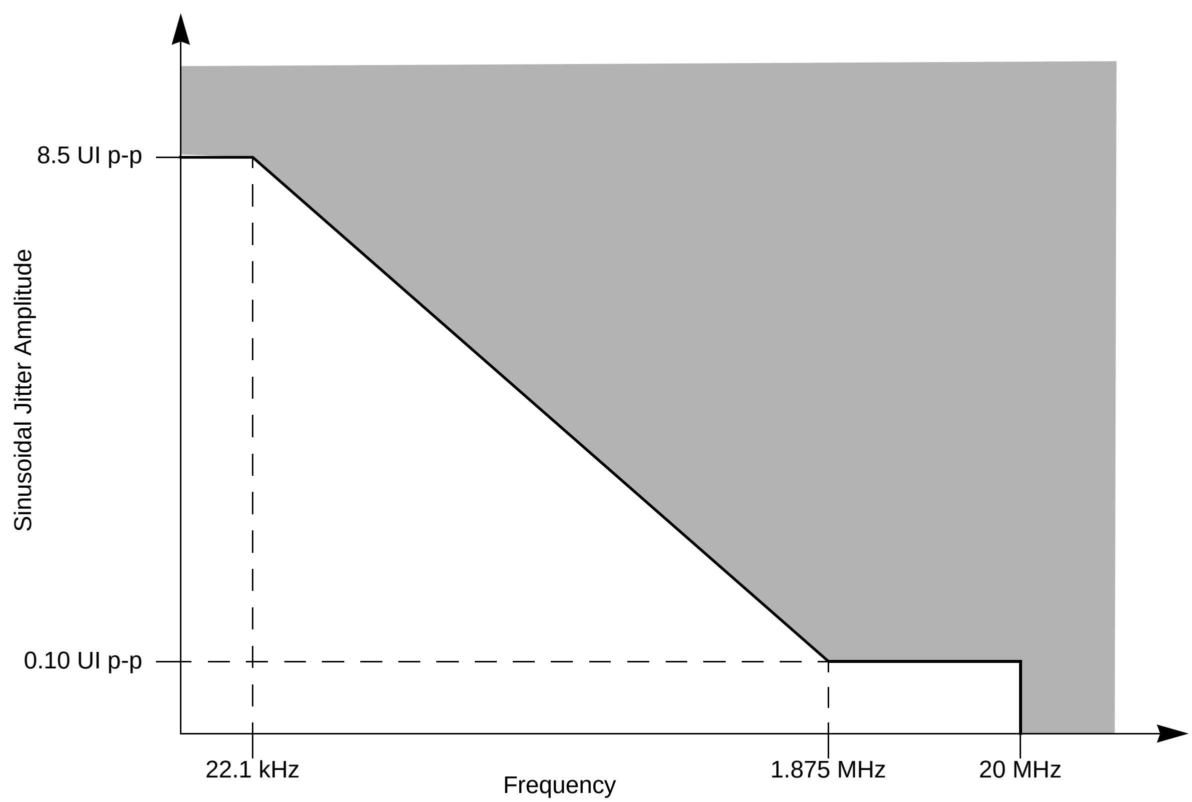

Figure 53. Single Frequency Sinusoidal Jitter Limits

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
				—
				—
				—
				—
PCI1_REQ0	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
PCI1_DEVSEL	AH11	I/O	OV_{DD}	2
PCI1_FRAME	AE11	I/O	OV_{DD}	2
PCI1_IDSEL	AG9	I	OV_{DD}	—
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV_{DD}	2, 5, 10
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV_{DD}	2
PCI2_CLK	AE28	I	OV_{DD}	39
PCI2_IRDY	AD26	I/O	OV_{DD}	2
PCI2_PERR	AD25	I/O	OV_{DD}	2
PCI2_GNT[4:1]	AE26, AG24, AF25, AE25	O	OV_{DD}	5, 9, 35
PCI2_GNT0	AG25	I/O	OV_{DD}	—
PCI2_SERR	AD24	I/O	OV_{DD}	2, 4
PCI2_STOP	AF24	I/O	OV_{DD}	2
PCI2_TRDY	AD27	I/O	OV_{DD}	2
PCI2_REQ[4:1]	AD28, AE27, W17, AF26	I	OV_{DD}	—
PCI2_REQ0	AH25	I/O	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	—
MBA[0:2]	F7, J7, M11	O	GV_{DD}	—

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11
Clock				
RTC	AF16	I	OV_{DD}	—
SYSCLK	AH17	I	OV_{DD}	—
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[7:4]/PCI2_C_$\overline{\text{BE}}$[3:0]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	17
PCI1_C_$\overline{\text{BE}}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV_{DD}	—
$\overline{\text{PCI1\_GNT}}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1\_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1\_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_TRDY}}$	AG11	I/O	OV_{DD}	2
$\overline{\text{PCI1\_REQ}}$[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ0}}$	AH3	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	39
$\overline{\text{PCI1\_DEVSEL}}$	AH11	I/O	OV_{DD}	2

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD\_TX}}$[0:3]	M23, N21, P23, R21	O	XV_{DD}	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11
Clock				
RTC	AF16	I	OV_{DD}	—
SYSCLK	AH17	I	OV_{DD}	—
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{TRST}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{LSSD\_MODE}$	AH20	I	OV_{DD}	25
TEST_SEL	AH14	I	OV_{DD}	109
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	O	AVDD_SRDS	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

Table 82. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

20.4 Frequency Options

Table 83This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	25	33.33	41.66	66.66	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500			
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533						
20	333	500							

Note: Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

NOTE

> It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK